1 INTRODUCTION

The TMP68HC11E9 is an advanced 8-bit microcontroller (MCU) with highly sophisticated on-chip peripheral capabilities. New design techniques were used to achieve a nominal bus speed of 2.1MHz (@Ta = −40~+85°C)*. In addition, the fully static design allows operation at frequencies down to dc, further reducing power consumption.

* : With the TMP68HC11E9, the 3MHz nominal bus speed is also guaranteed (@Ta = 0 to +70°C). The electrical specifications under 3MHz operation is similar to that of the TMP68HC11E0T-3/E1T-3. Refer to "1. Electrical Specifications" in "2.5 TMP68HC11E0T-3/E1T-3".

1.1 FEATURES

The following are some of the hardware and software highlights.

HARDWARE FEATURES

- 12K Bytes of ROM
- 512 Bytes of EEPROM
- 512 Bytes of RAM (All Saved During Standby) Relocatable to Any 4K Boundary
- Enhanced 16-Bit Timer System:
  Four Stage Programmable Prescaler
  Three Input Capture/Five Output Compare Functions or
  Four Input Capture/Four Output Compare Functions
- 8-Bit Pulse Accumulator Circuit
- Enhanced NRZ Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- Eight Channel, 8-Bit Analog-to-Digital Converter
- Real Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Available in Plastic Shrink Dual-In-Line Packages, and Plastic Leaded chip Carrier Packages.
- Under development Quad Flat Package

SOFTWARE FEATURES

- Enhanced M6800/M6801 Instruction Set
- 16×16 Integer and Fractional Divide Features
- Bit Manipulation
- WAIT Mode
- STOP Mode

1.2 GENERAL DESCRIPTION

The high-density CMOS technology used on the TMP68HC11E9 combines smaller size and higher speeds with the low power and high noise immunity of CMOS. On-chip memory systems include 12K bytes of ROM, 512 bytes of electrically eraseable

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programmable ROM (EEPROM), and 512 bytes of static RAM.

Major peripheral functions are provided on-chip. An eight channel analog-to-digital (A/D) converter is included with eight bits of resolution. An asynchronous serial communications interface (SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit free-running timer system has three input capture lines, five output compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected.

Two software controlled operating modes, WAIT and STOP, are available to conserve additional power.

A block diagram of the TMP68HC11E9 is shown in Figure 1.1

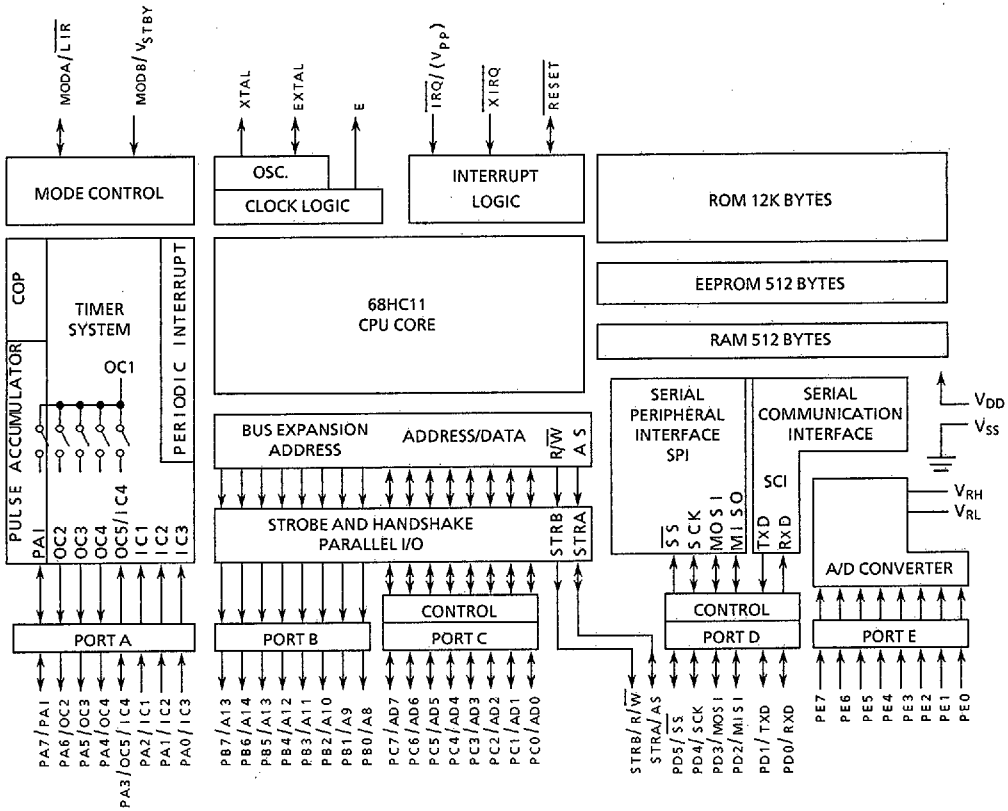

Figure 1.1 TMP68HC11E9 Block Diagram

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1.3 PROGRAMMER'S MODEL

In addition to being able to execute all M6800 and M6801 instructions, the TMP68HC11E9 allows execution of 91 new opcodes. Figure 1.2 shows the seven CPU registers which are available to the programmer.

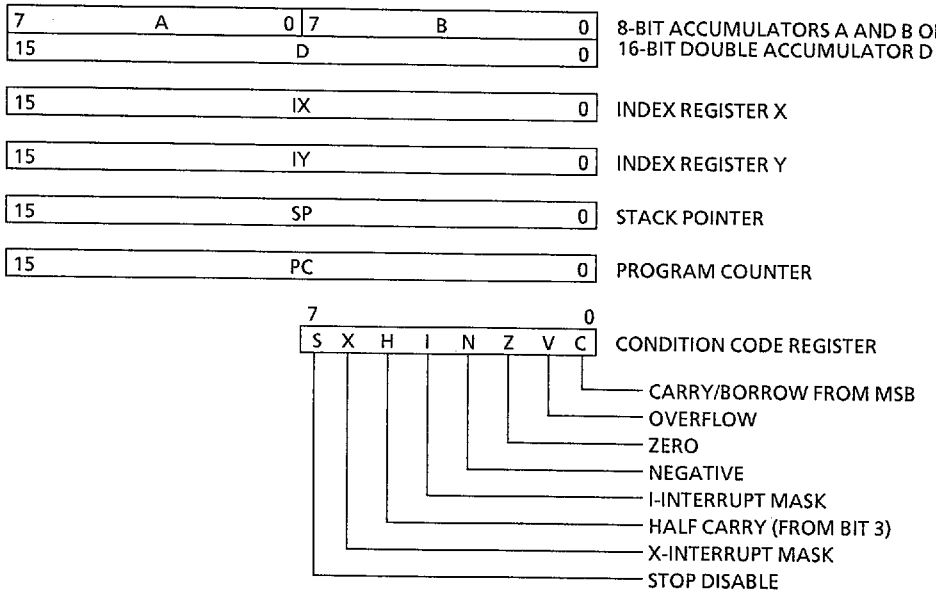

Figure 1.2 Programming Model

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2. SIGNAL DESCRIPTIONS AND OPERATING MODES

The signal descriptions and operating modes are presented in this section. When the microcontroller is in an expanded multiplexed operating mode, 18 pins change function to support a multiplexed address/data bus.

2.1 SIGNAL PIN DESCRIPTIONS

The following paragraphs provide a description of the input/output signals. Reference is made, where applicable, to other sections that contain more detail about the function being performed.

2.1.1 Input Power (V_{DD}) and Ground (V_{SS})

Power is supplied to the microcontroller using these pins. V_{DD} is the positive power input and V_{SS} is ground. Although the TMP68HC11E9 is a CMOS device, very fast signal transitions are present on many of its pins. Short rise and fall times are present even when the microcontroller is operating at slow clock rates. Special care must be taken to provide good power supply bypassing at the MCU. Recommended bypassing would include a 0.1 μF ceramic capacitor between the V_{DD} and V_{SS} pins and physically adjacent to one of the two pins. A bulk capacitance, whose size depends on the other circuity in the system, should also be present on the circuit board.

2.1.2 Reset ($\overline{\text{RESET}}$)

This active low bidirectional control signal is used as an input to initialize the TMP68HC11E9 to a known startup state, and as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit. This reset signal is significantly different from the reset signal used on other Motorola MCUs. Please refer to SECTION 9 RESETS, INTERRUPTS, AND LOW POWER MODES before designing circuitry to generate or monitor this signal.

2.1.3 Crystal Driver and External Clock Input (XTAL, EXTAL)

These two pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. The frequency applied to these pins shall be four times higher than the desired E clock rate. The XTAL pin is normally left unterminated when using an external CMOS compatible clock input to the EXTAL pin. The XTAL output is normally intended to drive only a crystal.

The XTAL output may be buffered with a high input impedance buffer such as the 74HC04, or it may be used to drive the EXTAL input of another TMP68HC11.

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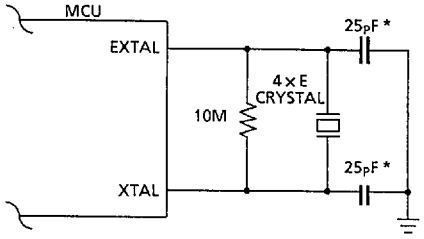
In all cases take extra care in the circuit board layout around the oscillator pins. Load capacitances shown in the oscillator circuits include all stray layout capacitances. Refer to Figures 2.1, 2.2, and 2.3 for diagrams of oscillator circuits.



* This value includes all stray capacitances.

Figure 2.1 Common Crystal Connections

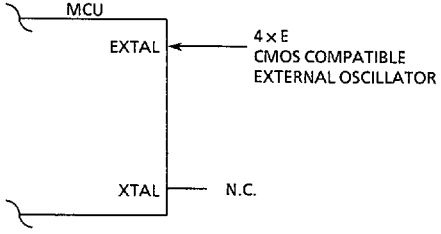
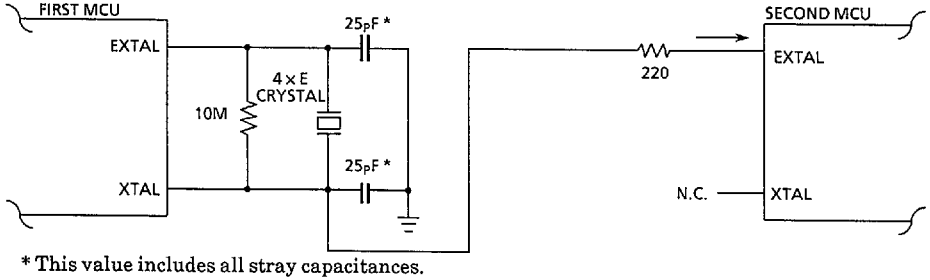


Figure 2.2 External Oscillator Connections



* This value includes all stray capacitances.

Figure 2.3 One Crystal Driving 2 MCUs

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2.1.4 E Clock Output (E)

This is the output connection for the internally generated E clock which can be used as a timing reference. The frequency of the E clock output is actually one fourth that of the input frequency at the XTAL and EXTAL pins. When the E clock output is low an internal process is taking place and, when high, data is being accessed. The E clock signal is halted when the MCU is in STOP mode.

2.1.5 Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ input provides a means for requesting asynchronous interrupts to the TMP68HC11E9. It is program selectable (OPTION register) with a choice of either negative edge-sensitive or level-sensitive triggering, and is always configured to level-sensitive triggering by reset. The $\overline{IRQ}$ pin requires an external pullup resistor to V_{DD} (typically 4.7K ohm).

During factory testing, this pin is also used as a bulk V_{PP} power supply-input. This allows for parallel programming of as many as half of the bytes in the EEPROM in a single programming operation.

2.1.6 Non-Maskable Interrupt ($\overline{XIRQ}$)

This input provides a means for requesting a non-maskable interrupt, after reset initialization. During reset, the X bit in the condition code register is set and any interrupt is masked until MCU software enables it. The $\overline{XIRQ}$ input is level sensitive and requires an external pullup resistor to V_{DD}.

2.1.7 Mode A/Load Instruction Register and Mode B/Standby Voltage (MODA/$\overline{LIR}$, MODB/V_{STBY})

During reset, MODA and MODB are used to select one of the four operating modes. Refer to Table 2.1 Paragraph 2.2 OPERATING MODES provides additional information.

After the operating mode has been selected, the $\overline{LIR}$ pin provides an open-drain output to indicate that an instruction is starting. All instructions are made up of a series of E clock cycles. The $\overline{LIR}$ signal goes low during the first E clock cycle of each instruction (opcode fetch). This output is provided as an aid in program debugging.

Table 2.1 Operating Modes versus MODA and MODB

MODB	MODA	Mode Selected
1	0	Single Chip
1	1	Expanded Multiplexed
0	0	Special Bootstrap
0	1	Special Test

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The V_{STBY} signal is used as the input for RAM standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the V_{DD} voltage, the internal 512-byte RAM and part of the reset logic are powered from this signal rather than the V_{DD} input. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

2.1.8 A/D Converter Reference Voltages (V_{RL}, V_{RH})

These two inputs provide the reference voltages for the analog-to-digital converter circuitry.

2.1.9 Strobe B and Read/Write (STRB/R/$\overline{W}$)

This signal acts as a strobe B output or as a data bus direction indicator depending on the operating mode.

In single-chip operating mode, the STRB output acts as a programmable strobe for handshake with other parallel I/O devices. Refer to SECTION 4 PARALLEL I/O for additional information.

In expanded multiplexed operating mode, R/$\overline{W}$ is used to control the direction of transfers on the external data bus. A low on the R/$\overline{W}$ signal indicates data is being written to the external data bus. A high on this signal indicates that a read cycle is in progress. R/$\overline{W}$ will stay low during consecutive data bus write cycles, such as in a double-byte store. The NAND of inverted R/$\overline{W}$ with the E clock should be used as the write enable signal for an external static RAM.

2.1.10 Strobe A and Address Strobe (STRA/AS)

This signal acts as an edge detecting strobe A input or as an address strobe bus control output depending on the operating mode.

In single-chip operating mode, the STRA input acts as a programmable strobe for handshake with other parallel I/O devices. Refer to SECTION 4 PARALLEL I/O for additional information.

In expanded multiplexed operating mode, the AS output is used to demultiplex the address and data signals at port C. Refer to 2.2.2 Expanded Multiplexed Operating Mode for additional information.

2.1.11 Port Signals

Ports A, D, and E signals are independent of the operating mode. Port B provides eight general purpose output signals in single-chip operating modes and provides eight high-order address signals when the microcontroller is in expanded multiplexed operating modes. Port C provides eight general purpose input/output signals when the microcontroller is in single-chip operating modes. When the microcontroller is in

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expanded multiplexed operating modes, port C is used for a multiplexed address/data bus. Table 2.2 shows a summary of the 40 port signals as they relate to the operating modes. Unused inputs and I/O pins configured as inputs should be terminated high or low.

Table 2.2 Port Signal Summary

Port-Bit	Single-Chip and Bootstrap Mode	Expanded Multiplexed and Special Test Mode
A-0	PA0/IC3	PA0/IC3
A-1	PA1/IC2	PA1/IC2
A-2	PA2/IC1	PA2/IC1
A-3	PA3/OC5/IC4/and-or OC1	PA3/OC5/IC4/and-or OC1
A-4	PA4/OC4/and-or OC1	PA4/OC4/and-or OC1
A-5	PA5/OC3/and-or OC1	PA5/OC3/and-or OC1
A-6	PA6/OC2/and-or OC1	PA6/OC2/and-or OC1
A-7	PA7/PAI/and-or OC1	PA7/PAI/and-or OC1
B-0	PB0	A8
B-1	PB1	A9
B-2	PB2	A10
B-3	PB3	A11
B-4	PB4	A12
B-5	PB5	A13
B-6	PB6	A14
B-7	PB7	A15
C-0	PC0	A0/D0
C-1	PC1	A1/D1
C-2	PC2	A2/D2
C-3	PC3	A3/D3
C-4	PC4	A4/D4
C-5	PC5	A5/D5
C-6	PC6	A6/D6
C-7	PC7	A7/D7
D-0	PD0/RxD	PD0/RxD
D-1	PD1/TxD	PD1/TxD
D-2	PD2/MISO	PD2/MISO
D-3	PD3/MOSI	PD3/MOSI
D-4	PD4/SCK	PD4/SCK
D-5	PD5/$\overline{SS}$	PD5/$\overline{SS}$
D-6	STRA	AS
D-7	STRB	R/$\overline{W}$
E-0	PE0/AN0	PE0/AN0
E-1	PE1/AN1	PE1/AN1
E-2	PE2/AN2	PE2/AN2
E-3	PE3/AN3	PE3/AN3
E-4	PE4/AN4	PE4/AN4
E-5	PE5/AN5	PE5/AN5
E-6	PE6/AN6	PE6/AN6
E-7	PE7/AN7	PE7/AN7

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2.1.11.1 Port A.

Port A may be configured for: four input capture functions (IC1, IC2, IC3, IC4) and three output compare functions (OC2, OC3, OC4), or three input capture functions (IC1, IC2, IC3) and four output compare functions (OC2, OC3, OC4, OC5) , and either a pulse accumulator input (PAI) or a fifth output compare function (OC1) . Refer to 8.1 PROGRAMMABLE TIMER for additional information.

Any port A pin that is not used for its alternate timer function may be used as a general-purpose input or output line.

2.1.11.2 Port B.

While in single-chip operating modes, all of the port B pins are general-purpose output pins. During MCU reads of this port, the level sensed at the input side of the port B output drivers is read. Port B may also be use in a simple strobed output mode where an output pulse appears at the STRB signal each time data is written to port B.

When in expanded multiplexed operating modes, all of the port B pins act as high order address output signals. During each MCU cycle, bits 8 through 15 of the address are output on the PB0-PB7 lines respectively.

2.1.11.3 Port C.

While in single-chip operating modes, all port C pins are general-purpose input/output pins. Port C inputs can be latched by providing an input transition to the STRA signal. Port C may also be used in full handshake modes of parallel I/O where the STRA input and STRB output act as handshake control lines.

When in expanded multiplexed operating modes, all port C pins are configured as multiplexed address/data signals. During the address portion of each MCU cycle, bits 0 through 7 of the address are output on the PC0-PC7 lines. During the data portion of each MCU cycle (E high), pins 0 through 7 are bidirectional data signals (D0-D7). The direction of data at the port C pins is indicated by the R/$\overline{W}$ signal.

2.1.11.4 Port D.

Port D pins 0-5 may be used for general purpose I/O signals. Port D pins alternately serve as the serial communications interface (SCI) and serial peripheral interface (SPI) signals when those subsystems are enabled.

Pin PD0 is the receive data input (RxD) signal for the serial communication interface (SCI).

Pin PD1 is the transmit data output (TxD) signal for the SCI.

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Pins PD2 through PD5 are dedicated to the SPI. PD2 is the master-in-slave-out (MISO) signal. PD3 is the master-out-slave in (MOSI) signal. PD4 is the serial clock (SCK) signal and PD5 is the slave select ($\overline{SS}$) input.

2.1.11.5 Port E.

Port E is used for general-purpose inputs and/or analog-to-digital (A/D) input channels. Reading port E during the sampling portion of an A/D conversion could cause very small disturbances and affect the accuracy of that result. If very high accuracy is required, avoid reading port E during conversions.

2.2 OPERATING MODES

There are four operating modes for the TMP68HC11E9:single-chip operating mode, expanded multiplexed operating mode, special bootstrap operating mode, and special test operating mode.

Table 2.1 shows how the operating mode is selected. The following paragraphs describe these operating modes.

2.2.1 Single-Chip Operating Mode

In single-chip operating mode, the TMP68HC11E9 functions as a monolithic microcontroller without external address or data buses. Port B, port C, strobe A, and strobe B function as general purpose I/O and handshake signals. Refer to SECTION 4 PARALLEL I/O for additional information.

2.2.2 Expanded Multiplexed Operating Mode

In expanded multiplexed operating mode, the TMP68HC11E9 has the capability of accessing a 64K byte address space. This total address space includes the same on-chip memory addresses used for single-chip operating mode plus external peripheral and memory devices. The expansion bus is made up of port B and port C, and control signals AS and R/$\overline{W}$. Figure 2.4 shows a recommended way of demultiplexing low order addresses from data at port C. The address, R/$\overline{W}$, and AS signals are active and valid for all bus cycles including accesses to internal memory locations.

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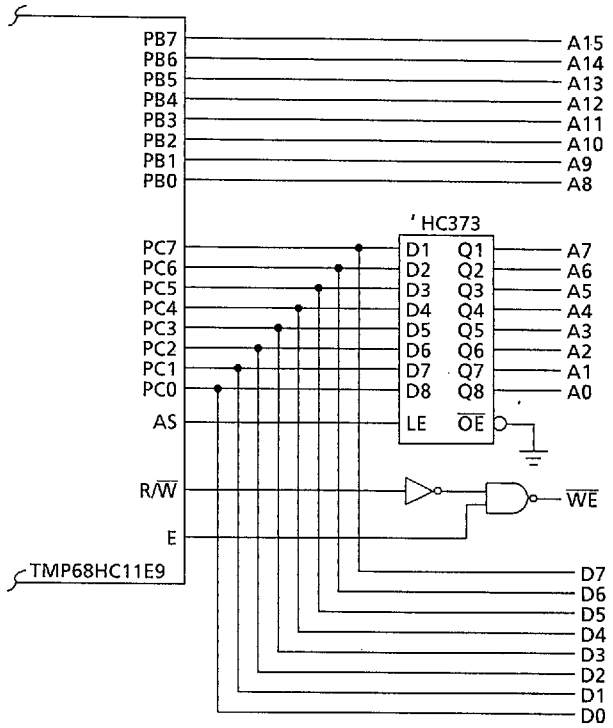

Figure 2.4. Address/Data Demultiplexing

2.2.3 Special Bootstrap Operating Mode

The bootstrap mode is considered a special operating mode as distinguished from the normal single-chip operating mode. This is a very versatile operating mode since there are essentially no limitations on the special purpose program that can be loaded into the internal RAM. The boot loader program is contained in the 192 byte bootstrap ROM. This ROM is enabled only if the MCU is reset in special bootstrap operating mode, and appears as internal memory space at locations $BF40-$BFFF. The boot loader program will use the SCI to read a 512 byte program into on-chip RAM at locations $0000-$01FF. After the final byte is received, control is automatically passed to that program at location $0000.

The TMP68HC11E9 communicates through the SCI port. After reset in special bootstrap operating mode, the SCI is running at E clock/16 (7812 baud for E clock equal 2 MHz). If the security feature was specified and the security bit is set, $FF is output by the SCI transmitter. The EEPROM is then erased. If erasure is unsuccessful, $FF is

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output again and erasure is attempted again. Upon successful erasure of the EEPROM, all internal RAM is written over with $FF. The CONFIG register is then erased. The boot loader program now proceeds as though the part had not been in security mode.

If the part is not in security mode (or has completed the above erase sequence), a break character is output by the SCI transmitter. For normal use of the boot loader program, the user sends $FF to the SCI receiver at either E clock/16 (7812 baud for E clock = 2MHz) or E clock/104 (1200 baud for E clock = 2MHz).

Note : This $FF is not echoed through the SCI transmitter.

Next the user must download 512 bytes of program data to be put into RAM starting at location $0000. These characters are echoed through the transmitter. When loading is complete, the program jumps to location $0000 and begins executing that code.

If the SCI transmitter pin is to be used, an external pullup resistor is required because port D pins are configured for wire-OR operation.

In special bootstrap operating mode the interrupt vectors are directed to RAM as shown in Table 2.1. This allows the user to use interrupts by way of a jump table. For example: to use the SWI interrupt, a jump instruction would be placed in RAM at locations $00F4, $00F5, and $00F6. When an SWI is encountered, the vector (which is in the boot loader ROM program) will direct program control to location $00F4 in RAM which in turn contains a JUMP instruction to the interrupt service routine.

Table 2.1 Bootstrap Mode Jump Table

Address	Jump Table
00C4	SCI
00C7	SPI
00CA	Pulse Accumulator Input Edge
00CD	Pulse Accumulator Overflow
00D0	Timer Overflow
00D3	Timer Output Compare 5/Input Capture 4
00D6	Timer Output Compare 4
00D9	Timer Output Compare 3
00DC	Timer Output Compare 2
00DF	Timer Output Compare 1
00E2	Timer Input Capture 3
00E5	Timer Input Capture 2
00E8	Timer Input Capture 1
00EB	Real Time Interrupt
00EE	$\overline{\text{IRQ}}$
00F1	$\overline{\text{XIRQ}}$
00F4	SWI
00F7	Illegal Opcode
00FA	COP Fail
00FD	Clock Monitor
Start of Boot Code	Reset

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2.2.4 Additional Boot Loader Program Options

The user may tie the receiver to the transmitter (with an external pull-up resistor). This will cause the program to jump directly to the beginning of EEPROM ($B600). Another way to cause the program to jump directly to EEPROM is to transmit either a break or $00 as the first character rather than the normal $FF.

Note that none of these options bypass the security check and so do not compromise those customers using security.

Keep in mind that upon entry to the downloaded program at location $0000, some registers have been changed from their reset states. The SCI transmitter and receiver are enabled which cause port D pins 0 and 1 to be dedicated to SCI use. Also port D is configured for wired-OR operation. It may be necessary for the user to write to the SCCR2 and SPCR registers to disable the SCI and/or port D wire-OR operation.

2.2.5 Special Test Operating Mode

The test mode is a special operating mode intended primarily for factory testing. This mode is very similar to the expanded multiplexed operating mode. In special test operating mode, the reset and interrupt vectors are fetched from external memory locations $BFC0-BFFF rather than $FFC0-$FFFF. There are no time limits for protection of the TMSK2, OPTION, and INIT registers, so these registers may be written repeatedly. Also a special TEST1 register is enabled which allows several factory test functions to be invoked.

The special test operating mode is not recommended for use by an end user because of the reduced system security;however, an end user may wish to come out of reset in special test operating mode. Then, after some initialization, the SMOD and MDA bits could be rewritten to select a normal operating mode to re-enable the protection features.

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3. ON-CHIP MEMORIES

This section describes the on-chip ROM, RAM, and EEPROM memories. The memory maps for each mode of operation are shown and the RAM and I/O mapping register (INIT) is described. The INIT register allows the on-chip RAM and the 64 control registers to be moved to suit the needs of a particular application.

3.1 MEMORY MAPS

Composite memory maps for each mode of operation are shown in Figure 3.1. Memory locations are shown in the shaded areas and the contents of these shaded areas are shown to the right. These modes include single-chip, expanded multiplexed, special bootstrap, and special test.

Single-chip operating modes do not generate external addresses. Refer to Table 3.1 for a full list of the registers.

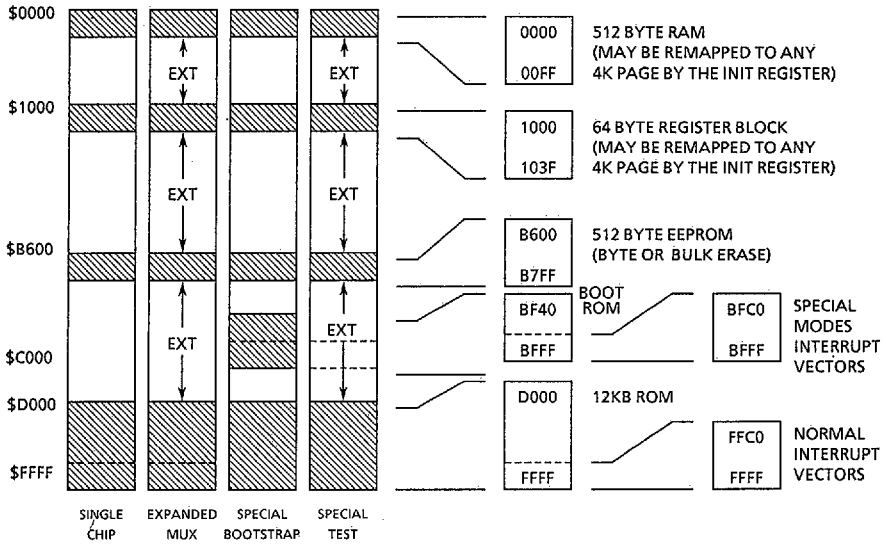

Figure 3.1 Memory Maps

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Table 3.1 Register and Control Bit Assignments (Sheet 1 of 3)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	–	–	–	–	–	–	Bit 0	PORTA	I/O Port A
$1001									Reserved	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control Register
	0	0	0	0	0	U	1	1		
$1003	Bit 7	–	–	–	–	–	–	Bit 0	PORTC	I/O Port C
$1004	Bit 7	–	–	–	–	–	–	Bit 0	PORTB	Output Port B
	0	0	0	0	0	0	0	0		
$1005	Bit 7	–	–	–	–	–	–	Bit 0	PORTCL	Alternate Latched Port C
$1006									Reserved	
$1007	Bit 7	–	–	–	–	–	–	Bit 0	DDRC	Data Direction for Port C
	0	0	0	0	0	0	0	0		
$1008			Bit 5	–	–	–	–	Bit 0	PORTD	I/O Port D
$1009			Bit 5	–	–	–	–	Bit 0	DDRD	Data Direction for Port D
			0	0	0	0	0	0		
$100A	Bit 7	–	–	–	–	–	–	Bit 0	PORTE	Input Port E
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Compare Force Register
	0	0	0	0	0					
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1 Action Mask Register
	0	0	0	0	0					
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1 Action Data Register
	0	0	0	0	0					
$100E	Bit 15	–	–	–	–	–	–	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	–	–	–	–	–	–	Bit 0		
$1010	Bit 15	–	–	–	–	–	–	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	–	–	–	–	–	–	Bit 0		
$1012	Bit 15	–	–	–	–	–	–	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	–	–	–	–	–	–	Bit 0		
$1014	Bit 15	–	–	–	–	–	–	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	–	–	–	–	–	–	Bit 0		

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Table 3.1 Register and Control Bit Assignments (Sheet 2 of 3)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1016	Bit 15	–	–	–	–	–	–	Bit 8	TOC1	Output Compare 1 Register
$1017	Bit 7	–	–	–	–	–	–	Bit 0		
$1018	Bit 15	–	–	–	–	–	–	Bit 8	TOC2	Output Compare 2 Register
$1019	Bit 7	–	–	–	–	–	–	Bit 0		
$101A	Bit 15	–	–	–	–	–	–	Bit 8	TOC3	Output Compare 3 Register
$101B	Bit 7	–	–	–	–	–	–	Bit 0		
$101C	Bit 15	–	–	–	–	–	–	Bit 8	TOC4	Output Compare 4 Register
$101D	Bit 7	–	–	–	–	–	–	Bit 0		
$101E	Bit 15	–	–	–	–	–	–	Bit 8	TOC5	Output Compare 5 Register
$101F	Bit 7	–	–	–	–	–	–	Bit 0		
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
	0	0	0	0	0	0	0	0		
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2
	0	0	0	0	0	0	0	0		
$1022	OC1I	OC2I	OC3I	OC4I	I4OC5I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Register 1
	0	0	0	0	0	0	0	0		
$1023	OC1F	OC2F	OC3F	OC4F	I4OC5F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Register 1
	0	0	0	0	0	0	0	0		
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Timer Interrupt Mask Register 2
	0	0	0	0						
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Timer Interrupt Flag Register 2
	0	0	0	0						
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL	Pulse Accumulator Control Register
	0	0	0	0	0	0	0	0		
$1027	Bit 7	–	–	–	–	–	–	Bit 0	PACNT	Pulse Accumulator Count Register
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
	0	0	0	0	0	1	U	U		
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
	0	0	0	0	0	0	0	0		
$102A	Bit 7	–	–	–	–	–	–	Bit 0	SPDR	SPI Data Register
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
	0	0	0	0	0	0	U	U		
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1
	U	U	0	0	0	0	0	0		
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register 2
	0	0	0	0	0	0	0	0		
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCSR	SCI Status Register
	1	1	0	0	0	0	0	0		
$102F	Bit 7	–	–	–	–	–	–	Bit 0	SCDR	SCI Data (Read RDR, Write TDR)

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Table 3.1 Register and Control Bit Assignments (Sheet 3 of 3)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
	0	0	U	U	U	U	U	U		
$1031	Bit 7	–	–	–	–	–	–	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	–	–	–	–	–	–	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	–	–	–	–	–	–	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	–	–	–	–	–	–	Bit	ADR4	A/D Result Register 4
$1035				PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT	EEPROM Block Protect Reg.
	0	0	0	1	1	1	1	1		
$1036 Thru $103B									Reserved	
$1039	ADPU	CSEL	IRQE	DLY	CME		CR1	CR0	OPTION	System Configuration Options
	0	0	0	1	0	0	0	0		
$103A	Bit 7	–	–	–	–	–	–	Bit 0	COPRST	Am/Reset COP Timer Circuity
	0	0	0	0	0	0	0	0		
$103B	ODD	EVEN		BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	EEPROM Programming Control
	0	0	0	0	0	0	0	0		
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Priorly 1-Bit Int and Misc
	–	–	–	–	0	1	0	1		
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping Register
	0	0	0	0	0	0	0	1		
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Register
$103F					NOSEC	NOCOP	ROMON	EEON	CONFIG	COP, ROM and EEPROM Enables
	0	0	0	0	*	*	*	*		

Initial state (Control bit only)

0 : Clear
1 : Set
U : Undefined
– : Effected by a pin status
* : Fixed depending on products
□ : Bits changed only within 64E clock cycles after reset

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In expanded multiplexed operating modes, memory locations are basically the same as the single-chip operating modes; however, the locations between the shaded areas (designated EXT) are for externally addressed memory and I/O. If an external memory or I/O device is located to overlap an enabled internal resource, the internal resource will take priority. For reads of such an address the data (if any) driving the port C data inputs is ignored and will not result in any harmful conflict with the internal read. For writes to such an address data is driven out of the port C data pins as well as to the internal location. No external devices should drive port C during write accesses to internal locations; however, there is normally no conflict since the external address decode and/or data direction control should incorporate the R/$\overline{W}$ signal in their development. The R/$\overline{W}$, AS, address, and write data signals are valid for all accesses including accesses to internal memory and registers.

The special bootstrap operating mode memory locations are similar to the single-chip operating mode memory locations except that a bootstrap program at memory locations $BF40 through $BFFF is enabled. The reset and interrupt vectors are addressed at $BFC0-$BFFF while in the special bootstrap operating mode. These vector addresses are within the 192 byte memory used for the bootstrap program.

The special test operating mode memory map is the same as the expanded multiplexed operating mode memory map except that the reset and interrupt vectors are located at external memory locations $BFC0-$BFFF.

3.2 RAM AND I/O MAPPING REGISTER (INIT)

There are 64 internal registers which are used to control the operation of the MCU. These registers can be relocated on 4K boundaries within the memory space, using the INIT register. Refer to Table 3.1 (found on a foldout page at the back of this document) for a complete list of the registers. The registers and control bits are explained throughout this document.

The INIT register is a special-purpose 8-bit register which may be used during initialization to change the default locations of RAM and control registers within the MCU memory map. It may be written to only once within the initial 64E clock cycles after a reset and thereafter becomes a read-only register.

	7	6	5	4	3	2	1	0	
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
RESET	0	0	0	0	0	0	0	1	

The default starting address for internal RAM is $0000 and the default starting address for the 64 control registers is $1000 (the INIT register is set to $01 by reset). The upper four bits of the INIT register specify the starting address for the 512 byte RAM

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and the lower four bits of INIT specify the starting address for the 64 control registers. These four bits are matched to the upper four bits of the 16-bit address.

This convention indecates that the register block may be relocated to any 4K memory page, but that its default location is $1000.

RAM and the control and status registers can be relocated independently. If the control and status registers are relocated in such a way as to conflict with ROM, then the register block takes priority, and the ROM at those locations becomes inaccessible. No harmful conflicts result. Lower priority resources simply become inaccessible. Similarly, if an internal resource conflicts with an external device, no harmful conflict results, since data from the external device is not applied to the internal data bus. Thus, it cannot interfere with the internal read.

Note : There are unused register locations in the 64 byte control and status register block. Reads of these unused registers return data from the undriven internal data bus, not from another source that happens to be located at the same address.

3.3 ROM

The internal 12K ROM occupies the highest 12K of the memory map ($D000-$FFFF). This ROM is disabled when the ROMON bit in the CONFIG register is clear. The ROMON bit is implemented with an EEPROM cell and is programmed using the same procedures for programming the on-chip EEPROM. For further information refer to 3.5.3 System Configuration Register (CONFIG).

In the single-chip operating mode, internal ROM is enabled regardless of the state of the ROMON bit.

There is also a 192 byte mask programmed boot ROM in the TMP68HC11E9. This bootstrap program ROM controls the operation of the special bootstrap operating mode and is only enabled following reset in the special bootstrap operating mode. For more information refer to 2.2.3 Special Bootstrap Operating Mode.

3.4 RAM

The 512 byte internal RAM may be relocated during initialization by writing to the INIT register. The reset default position is $0000 through $01FF. This RAM is implemented with static cells and retains its contents during the WAIT and STOP modes.

The contents of the 512 byte RAM can also be retained by supplying a low current backup power source to the MODB/V_{STBY} pin. When using a standby power source, V_{DD} may be removed;however, reset must go low before V_{DD} is removed and remain low until V_{DD} has been restored.

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3.5 EEPROM

The 512 bytes of EEPROM are located at $B600 through $B7FF and have the same read cycle time as the internal ROM. The write (or programming) mechanism for the EEPROM is controlled by the PPROG register. The EEPROM is disabled when the EEON bit in the CONFIG register is zero. The EEON bit is implemented with an EEPROM cell.

The erased state of an EEPROM byte is $FF. Programming changes ones to zeros. If any bit in a location needs to be changed from a zero to a one, the byte must be erased in a separate operation before it is reprogrammed. If a new data byte has no ones in bit positions which were already programmed to zero, it is acceptable to program the new data without erasing the EEPROM byte first. For example, programming $50 to a location which was already $55 would change the location to $50.

Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz the efficiency of this charge pump decreases which increases the time required to program or erase a location. The recommended program and erase time is 10 milliseconds when the E clock is 2 MHz and should be increased to as much as 20 milliseconds when E is between 1 MHz and 2MHz. When the E clock is below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. Note that the CSEL bit also controls a clock to the analog to digital converter subsystem.

3.5.1 EEPROM Programming Control Register (PPROG)

This 8-bit register is used to control programming and erasure of the 512-byte EEPROM. Reset clears this register so the EEPROM is configured for normal reads.

	7	6	5	4	3	2	1	0	
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
RESET	0	0	0	0	0	0	0	0	

ODD - Program Odd Rows (TEST)

EVEN - Program Even Rows (TEST)

Bit5 - Not implemented.

This bit always reads zero.

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BYTE - Byte Erase Select

This bit overrides the ROW bit.

0 = Row or Bulk Erase

1 = Erase Only One Byte

ROW - Row Erase Select

If the BYTE bit is 1, ROW has no meaning.

0 = Bulk Erase

1 = Row Erase

ERASE - Erase Mode Select

0 = Normal Read or Program

1 = Erase Mode

EELAT - EEPROM Latch Control

0 = EEPROM Address and Data Configured for Read Mode

1 = EEPROM Address and Data Configured for Programming/Erasing

EEPGM - EEPROM Programming Voltage Enable

0 = Programming Voltage Switched Off

1 = Programming Voltage Turned On

If an attempt is made to set both the EELAT and EEPGM bits in the same write cycle, neither will be set. If a write to an EEPROM address is performed while the EEPGM bit is set, the write is ignored and the programming operation currently in progress is not disturbed. These two safe-guards were included to prevent accidental EEPROM changes in cases of program runaway.

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3.5.2 EEPROM Block Protect Register (BPROT)

This register prevents inadvertent writes to the CONFIG register and to the 512 bytes of EEPROM. The bits in this registers may only be written to zero during the first 64 E clock cycles after reset in the normal modes. Once the bits are set to zero, the associated EEPROM section and/or the CONFIG register may be programmed or erased in the normal manner. The EEPROM is only visible if the EEON bit in the CONFIG register is set to "one". The bits in the BPROT register may be written back to one (in any mode) to protect the EEPROM and/or the CONFIG register, but can only be cleared again if operating in the test or bootstrap modes.

	7	6	5	4	3	2	1	0	
$1035				PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
RESET	0	0	0	1	1	1	1	1	

Bits 7-5 - Not Implemented

These bits always read as zero

PTCON - Protect CONFIG Register

1 = Programming/erasure of the CONFIG register disabled

0 = Programming/erasure of the CONFIG register allowed

BPRT3-BPRT0 - Block Protect

When set, these bits protect a block of EEPROM from programming and erasure, and when cleared allow programming and erase of the associated block.

Bit	Block Protected	Size
BPRT0	$B600-$B61F	32 Bytes
BPRT1	$B620-$B65F	64 Bytes
BPRT2	$B660-$B6DF	128 Bytes
BPRT3	$B6E0-$B7FF	288 Bytes

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3.5.3 Programming/Erasing Internal EEPROM

The EEPROM programming and erasure process is controlled by the PPROG register. The following paragraphs describe the various operations performed on the EEPROM and include example program segments to demonstrate programming and erase operations.

These program segments are intended to be simple straightforward examples of the sequences needed for basic program and erase operations. There are no special restrictions on the address modes used and bit manipulation instructions may be used. Other MCU operations can continue to be peformed during EEPROM programming and erasure provided these operations do not include reads of data from EEPROM (the EEPROM is disconnected from the read data bus during EEPROM program and erase operations). The subroutine DLY10 used in these program segments is not shown but can be any set of instructions which takes ten milliseconds.

3.5.3.1 Read.

For the read operation the EELAT bit in the PPROG register must be clear. When this bit is cleared, the remaining bits in the PPROG register have no meaning or effect, and the EEPROM may be read as if it were a normal ROM.

3.5.3.2 Programming.

During EEPROM programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Recall that in this EEPROM, zeros must be erased by a separate erase operation before programming. The following program segment demonstrates how to program an EEPROM byte.

*On entry, A = data to be programmed and X = an EEPROM address

```
        •
        •
        •
PROG    LDAB    #$02
        STAB    $103B     Set EELAT Bit (EEPGM = 0)
        STAA    0, X      Store Data to EEPROM Address
        LDAB    #$03
        STAB    $103B     Set EEPGM Bit (EELAT = 1)
        JSR     DLY10     Delay 10 ms
        CLR     $103B     Turn Off High Voltage and Set to READ Mode
        •
        •
        •
```


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3.5.3.3 Bulk Erase.

The following program segment demonstrates how to bulk erase the 512-byte EEPROM. The CONFIG register is not affected in this example.

```
        •
        •
        •
BULKE   LDAB    #$06
        STAB    #103B   Set to Bulk Erase Mode
        STAB    $B600   Write any Data to any EEPROM Address
        LDAB    #$07
        STAB    $103B   Turn On Programming Voltage
        JSR     DLY10   Delay 10 ms
        CLR     $103B   Turn Off High Voltage and Set to READ Mode
        •
        •
        •
```

3.5.3.4 Row Erase.

The following program segment demonstrates the row erase function. A 'row' is sixteen bytes ($B600-$B60F, $B610-$B61F...$B7F0-$B7FF). This type of erase operation saves time compared to byte erase when large sections of EEPROM are to be erased.

*On entry X = any address in the row to be erased

```
        •
        •
        •
ROWE    LDAB    #$0E
        STAB    $103B   Set to Row Erase Mode
        STAB    0, X    Write any Data to any Address in Row
        LDAB    #$0F
        STAB    $103B   Turn on High Voltage
        JSR     DLY10   Delay 10 ms
        CLR     $103B   Turn Off High Voltage and Set to Read Mode
        •
        •
        •
```


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3.5.3.5 Byte Erase.

The following program segment shows the byte erase function.

*On entry, X = address of byte to be erased

```
        •
        •
        •
BYTEE   LDAB    #$16
        STAB    $103B     Set to Byte Erase Mode
        STAB    0, X      Write any Data to the Address to Erase
        LDAB    #$17
        STAB    $103B     Turn on High Voltage
        JSR     DLY10     Delay 10 ms
        CLR     $103B     Turn Off High Voltage and Set to Read Mode
        •
        •
        •
```

3.5.4 System Configuration Register (CONFIG)

The TMP68HC11E9 can be configured to specific system requirements through the use of hardwired options such as the mode select pins, semi-permanent EEPROM control bit specifications (CONFIG register), or by use of control registers. The configuration control register (CONFIG) is implemented in EEPROM cells and controls the presence of ROM and EEPROM in the memory map, as well as enabling the COP watchdog system. A security feature to protect data in the EEPROM and RAM is also available on mask programmed TMP68HC11E9s.

	7	6	5	4	3	2	1	0	
$103F	0	0	0	0	NOSEC	NOCOP	ROMON	EEON	CONFIG
RESET	(see 3.5.4.2 OPERATION OF THE CONFIG MECHANISM)								

Bits 7, 6, 5, and 4-Not Implemented

These bits are always read as zero.

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NOSEC - Security Mode Disable Bit

This bit is only implemented if it is specifically requested at the time mask ROM information is requested. When this bit is not implemented it always reads one.

When RAM and EEPROM security are required, the NOSEC bit can be programmed to zero to enable a software anti-theft mechanism. When clear, the NOSEC bit prevents the selection of expanded multiplexed operating modes. If the MCU is reset in the special bootstrap operating mode while NOSEC is zero, EEPROM, RAM, and CONFIG are erased before the loading process continues.

0 = Enable Security Mode

1 = Disable Security Mode

NOCOP - COP System Disable

0 = COP Watchdog System Enabled

1 = COP Watchdog System Disabled

ROMON - Enable On-Chip ROM

When this bit is clear, the 12K ROM is disabled, and that memory space becomes externally accessed space. In the single-chip operating mode, the internal 12K ROM is enabled regardless of the state of the ROMON bit.

EEON - Enable On-Chip EEPROM

When this bit is clear, the 512-byte EEPROM is disabled, and that memory space becomes externally accessed space.

3.5.4.1 Programming and Erasure of the Config Register.

Since the CONFIG register is implemented with EEPROM cells, special provisions must be made to erase and program this register. The normal EEPROM control bits in the PPROG register are used for this purpose. Programming follows the same procedure as programming a byte in the 512-byte EEPROM except the CONFIG register address is used. Erase also follows the same procedure as that used for the EEPROM.

The CONFIG register may only be programmed or erased while the MCU is operating in the test mode or the bootstrap mode.

The following program segment demonstrates how to program the CONFIG register. This program assumes that the CONFIG register was previously erased and the PTCON bit in the BPROT register is clear.

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*On entry, A = data to be programmed into CONFIG

```
        •
        •
        •
PROGC   LDAB    #$02
        STAB    $103B    Set EELAT Bit (EEPGM = 0)
        STAA    $103F    Store Data to CONFIG Address
        LDAB    #$03
        STAB    $103B    Turn on Programming Voltage
        JSR     DLY10    Delay 10 ms
        CLR     $103B    Turn Off High Voltage and Set to READ Mode
        •
        •
        •
```

The following program segment demonstrates the byte erase procedure for the CONFIG register.

```
        •
        •
        •
BYTEC   LDAB    #$16
        STAB    $103B    Set Byte Erase Mode
        STAB    $103F    Write any Data to CONFIG
        LDAB    #$17
        STAB    $103B    Turn on Programming Voltage
        JSR     DLY10    Delay 10 ms
        CLR     $103B    Turn Off High Voltage and Set to READ Mode
        •
        •
        •
```


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3.5.4.2 Operation of the Configuration Mechanism.

The CONFIG register consists of an EEPROM byte and static working latches. This register controls the startup configuration of the MCU. The contents of the EEPROM CONFIG byte are transferred into static working latches during any reset sequence. The operation of the MCU is controlled directly by these latches and not the actual EEPROM byte. Changes to the EEPROM byte do not affect operation of the MCU until after the next reset sequence. When programming the CONFIG register, the EEPROM byte is being accessed. When the CONFIG register is being read, the static latches are being accessed.

To change the value in the CONFIG register proceed as follows:

1) Erase the CONFIG register.

Note : Do not issue a reset at this time.

2) Program the new value to the CONFIG register.

3) Issue a reset so the new configuration will take effect.

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4 PARALLEL I/O

Please refer to SECTION 4. PARALLEL I/O in TMP68HC11A8

5 SERIAL COMMUNICATIONS INTERFACE (SCI)

Please refer to SECTION 5. SERIAL COMMUNICATIONS INTERFACE (SCI) in TMP68HC11A8

6 SERIAL PERIPHERAL INTERFACE (SPI)

Please refer to SECTION 6. SERIAL PERIPHERAL INTERFACE (SPI) in TMP68HC11A8

7 ANALOG-TO-DIGITAL CONVERTER

Please refer to SECTION 7. ANALOG-TO-DIGITAL CONVERTER in TMP68HC11A8

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8. PROGRAMMABLE TIMER, REAL TIME INTERRUPT, AND PULSE ACCUMULATOR

This section describes the 16-bit programmable timer, the real time interrupt, and the pulse accumulator system.

8.1 PROGRAMMABLE TIMER

The timer has a single 16-bit free-running counter which is clocked by the output of a four-stage prescaler (divide by 1, 4, 8, or 16), which is in turn driven by the MCU E clock. Input functions are called input captures. These input captures record the count form the free-running counter in response to a detected edge on an input line. Output functions, called output compares, cause an output action when there is a match between a 16-bit output-compare register and the free-running counter. This timer system has four input capture registers and five output compare registers, one register is selectable whether input capture or output compare.

8.1.1 Counter

The key element in the timer system is a 16-bit free-running counter, or timer counter register. After reset, the MCU is configured to use the E clock as the input to the free-running counter. Initialization software may optionally reconfigure the system to use one of the three prescaler values. The prescaler control bits can only be written once during the first 64 cycles after a reset. Software can read the counter at any time without affecting its value because it is clocked and read during opposite phases of the E clock.

A counter read should first address the most significant byte. An MPU read of this address causes the least significant byte to be transferred to a buffer. This buffer is not affected by reset and is accessed when reading the least significant byte of the counter. For double byte read instructions, the two accesses occur on consecutive bus cycles.

The counter is cleared to $0000 during reset and is a read-only register with one exception. In test modes only, any MPU write to the most significant byte presets the counter to $FFF8 regardless of the value involved in the write.

When the count changes from $FFFF to $0000, the timer overflow flag (TOF) bit is set in timer interrupt flag register 2 (TFLG2). An interrupt can be enabled by setting the interrupt enable bit (TOI) in timer interrupt mask register 2 (TMSK2).

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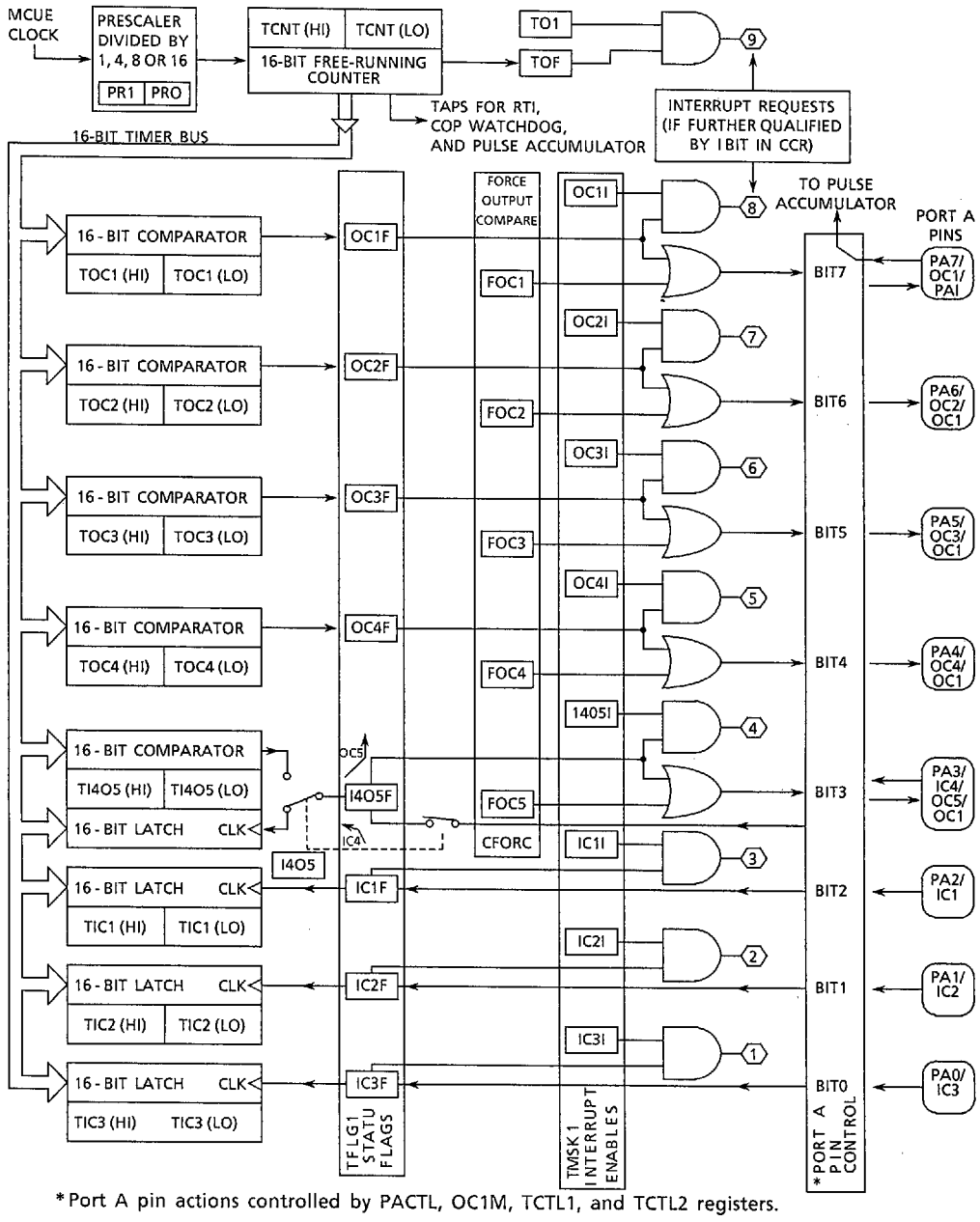

*Port A pin actions controlled by PACTL, OC1M, TCTL1, and TCTL2 registers.

Figure 8.1 Timer Block Diagram

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8.1.2 Input Capture

The input capture registers are 16-bit read-only registers which are not affected by reset and are used to latch the value of the counter when a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers counter transfer is defined by the corresponding input edge bits (EDGxB, EDGxA) in TCTL2.

The result obtained by an input capture corresponds to the value of the counter one E clock cycle after the transition which triggered the edge-detection logic. The selected edge transition sets the ICxF bit in timer interrupt flag register 1 (TFLG1) and can cause an interrupt if the corresponding ICxI bit(s) is (are) set in the timer interrupt mask register 1 (TMSK1). A read of the input capture register's most significant byte inhibits captures for one E cycle to allow a double-byte read of the full 16-bit register.

8.1.2.1 Input Capture 4

Port A pin 3 serves multiple functions. After reset, data direction bit 3 (DDRA3), in the PACTL register is cleared to zero configuring Port A pin 3 as an input. Port A pin 3 can then be used as an input capture 4 (IC4), by setting I4/O5 to "one" in the PACTL register. The I4/O5 bit is configured to OC5 (cleared to zero) on reset. If DDA3 is configured as an output (set to one) and IC4 is enabled, writes to Port A bit 3 causes edges on the PA3 pin to result in input captures. All other aspects of using IC4 remain the same as the other input captures, with the exception that the 16-bit timer output compare 5 register now also server as the 16-bit timer input capture 4 register. When the TI4O5 register is acting as the IC4 capture register it cannot be written to. Upon reset, I4/O5 is configured as OC5. The OC5 function overrides DDRA3 to force the Port A pin 3 to be an output whenever OM5:OL5 bit are not 0:0. In all other aspects, OC5 works the same as the other output compares.

8.1.3 Output Compare

All output compare registers are 16-bit read/write registers which are initialized to $FFFF by reset. They can be used as output waveform controls or as elapsed time indicators. If an output compare register is not used, it may be used as a storage location.

All output compare registers have a separate dedicated comparator for comparing against the free-running counter. If a match is found, the corresponding output compare flag (OCxF) bit in TFLG1 is set and a specified action is automatically taken. For output compare functions two through five the automatic action is controlled by pairs of bits (OMx and OLx) in the timer control register 1 (TCTL1). Each pair of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. The output action is taken on each succesful compare regardless of wheather or not the OCxF flag was previously clear.

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An interrupt can also accompany a successful output compare, provided that the corresponding interrupt enable bit (OCx1) is set in TMSK1.

After an MPU write cycle to the most significant byte, output compares are inhibited for one E cycle in order to allow writing two consecutive bytes before making the next comparison. If both bytes of the register are to be changed, a double-byte write instruction should be used in order to take advantage of the compare inhibit feature.

MPU write can be made to either byte of the output compare register without affecting the other byte.

A write-only register, timer compare force (CFORC), allows forced compares. Five of the bit positions in the CFORC register correspond to the five output compares. To force a compare, or compares, a write is done to CFORC register withe the associated bits set for each output compare that is to be forced. The action taken as a result of a forced compare is the same as if there was a match between the OCx register and the free-running counter, except that the corresponding interrupt status flag bits are not set. Output actions are synchronized to the prescaled timer clock so there could be as much as 16 E clock cycles of delay between the write to CFORC and the output action.

8.1.4 Output Compare 1 I/O Pin Control

Unlike the other four output compares, output compare 1 can automatically affect any or all of the five output pins (bits 3-7) in port A as a result of a successful compare between the OC1 register and the 16-bit free-running counter. The two 5-bit registers used in conjunction with this function are the output compare 1 mask register (OC1M) and the output compare 1 data register (OC1D).

Register OC1M is used to specify the bits of port A (I/O and timer port) which are to be affected as a result of a successful OC1 compare. Register OC1D is used to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare. If an OC1 compare and another output compare occur during the same E cycle and both attempt to alter the same port A line, the OC1 compare prevails.

This function allows control of multiple I/O pins automatically with a single output compare.

Another intended use for the special I/O pin control on output compare 1 is to allow more than one output compare to control a single I/O pin. This allows pulses as short as one E clock cycle to be generated.

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8.1.5 Timer Compare Force Register (CFORC)

The timer compare force register is used to force early output compare actions. The CFORC register is an 8-bit write-only register. Reads of this location have no meaning and always return logic zeros. Note that the compare force function is not generally recommended for use with the output toggle function because a normal compare occuring immediately before or after the force may result in undesirable operation.

	7	6	5	4	3	2	1	0	
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC
RESET	0	0	0	0	0	0	0	0	

FOC1-FOC5 - Force Output Compare x Action

0= Has no meaning

1= Causes action programmed for output compare x, except the OCxF flag bit is not set.

Bits 2-0 - Not Implemented

These bits always read zero.

8.1.6 Output Compare 1 Mask Register (OC1M)

This register is used in conjunction with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M
RESET	0	0	0	0	0	0	0	0	

The bit of the OC1M register correspond bit-for-bit with the lines of port A (lines 7 through 3 only). For each bit that is affected by the successful compare, the corresponding bit in OC1M should be set to one.

Note that the pulse accumulator function shares line 7 of port A. If the DDRA7 bit in the pulse accumulator control register (PACTL) is set, then port A line 7 is configured as an output and OC1 can obtain access by setting OC1M bit 7. In this condition if the PAEN bit in the PACTL register is set, enabling the pulse accumulator input, then OC1 compares cause a write of OC1D bit 7 to an internal latch, and the output of that latch drives the pin and the pulse accumulator input. This action can then cause the pulse accumulator to take the appropriate action (pulse count or gate modes).

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8.1.7 Output Compare 1 Data Register (OC1D)

This register is used in conjunction with output compare 1 to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D
RESET	0	0	0	0	0	0	0	0	

The bits of the OC1D register correspond bit-for-bit with the lines of port A (lines 7 thru 3 only) . When a successful OC1 compare occurs, for each bit that is set in OC1M, the corresponding data bit in OC1D is stored in the corresponding bit of port A. If there is a conflicting situation where an OC1 compare and another output compare function occur during the same E cycle with both attempting to alter the same port A line, the OC1 action prevails.

8.1.8 Timer Control Register 1 (TCTL1)

	7	6	5	4	3	2	1	0	
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
RESET	0	0	0	0	0	0	0	0	

OM2, OM3, OM4, and OM5 - Output Mode

OL2, OL3, OL4, and OL5 - Output Level

These two control bits (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx compare.

OMx	OLx	Action Taken Upon Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

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8.1.9 Timer Control Register 2 (TCTL2)

	7	6	5	4	3	2	1	0	
$1021	EDG4B	EDG4B	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
RESET	0	0	0	0	0	0	0	0	

EDGxB and EDGxA - Input Caputre x Edge Control.

These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x as follow:

EDGxB	EDBxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any (rising or falling)edge

8.1.10 Timer Interrupt Mask Register 1 (TMSK1)

	7	6	5	4	3	2	1	0	
$1022	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I	TMSK1
RESET	0	0	0	0	0	0	0	0	

OCxI - Output compare x Interrupt

If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

ICxI - Input Capture x Interrupt

If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

Note : When the I4/O5 bit in the PACTL register is one, the I4O5I bit behaves as the Input Capture 4 Interrupt bit, and when I4/O5 is zero, the I4O5I bit acts as the Output Compare 5 Interrupt control bit.

8.1.11 Timer Interrupt Flag Register 1 (TFLG1)

Timer interrupt flag register 1 is used to indicate the occurrence of timer system events, and together with the TMSK1 register allows the timer subsystem to operate in a polled or interrupt driven system. For each bit in TFLG1, there is a corresponding bit in TMSK1 in the same bit position. If the mask bit is set, each time the condition for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

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These timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

	7	6	5	4	3	2	1	0	
$1023	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F	TFLG1
RESET	0	0	0	0	0	0	0	0	

OCxF - Output Compare xFlag

This flag bit is set each time the timer counter matches the output compare register x value. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

ICxF - Input Capture x Flag

This flag is set each time a selected active edge is detected on the ICx input line. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

Note : When the I4/O5 bit in the PACTL register is one, the I4O5F bit behaves as the Input Capture 4 Flag bit, and when I4/O5 is zero, the I4O5I bit acts as the Output Compare 5 Flag.

8.1.12 Timer Interrupt Mask Register 2 (TMSK2)

Timer interrupt mask register 2 is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in timer interrupt flag register 2. In addition, two timer prescaler bits are included in this register. For each of the four most significant bits in timer flag register 2, (TFLG2), there is a correponding bit in the timer mask register 2 (TMSK2) in the same bit position.

	7	6	5	4	3	2	1	0	
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2
RESET	0	0	0	0	0	0	0	0	

TOI - Timer Overflow Interrupt Enable

0 = TOF interrupts disabled

1 = Interrupt requested when TOF = 1

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RTII - RTI Interrupt Enable

0 = RTIF interrupts disabled

1 = Interrupt requested when RTIF = 1

PAOVI - Pulse Accumulator Overflow Interrupt Enable

0 = PAOVF interrupts disabled

1 = Interrupt requested when PAOVF = 1

PAII - Pulse Accumulator Input Interrupt Enable

0 = PAIF interrupts disabled

1 = Interrupt requested when PAIF = 1

Bits3 and 2 - Not Implemented

These bits always read zero.

PR1 and PR0 - Timer Prescaler Selects

These two bits may be read at any time but may only be written during initalization. Writes are disabled after the first write or after 64 E cycles out of reset. If the MCU is in special test or special bootstrap mode, then these two bits may be written any time.

These two bits specify the timer prescaler divide factor.

PR1	PR0	Divide-by-Factor
0	0	1
0	1	4
1	0	8
1	1	16

8.1.13 Timer Interrupt Flag Register 2 (TFLG2)

Timer interrupt flag register 2 is used to indicate the occurrence of timer system events, and together with the TMSK2 register, allows the timer subsystems to operate in a polled or interrupt driven system. For each bit in timer flag register 2 (TFLG2), there is a corresponding bit in timer mask register 2 (TMSK2) in the same bit position. If the enable bit is set each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

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The timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

	7	6	5	4	3	2	1	0	
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2
RESET	0	0	0	0	0	0	0	0	

TOF - Timer Overflow

This bit is cleared by reset. It is set to one each time the 16-bit free-running counter advances from a value of $FFFF to $0000. This bit is cleared by a write to the TFLG2 register with bit 7 set.

RTIF - Real Time Interrupt Flag

This bit is set at each rising edge of the selected tap point. This bit is cleared by a write to the TFLG2 register with bit 6 set.

PAOVF - Pulse Accumulator Overflow Interrupt Flag

This bit is set when the count in the pulse accumulator rolls over from $FF to $00. This bit is cleared by a write to the TFLG2 register with bit 5 set.

PAIF - Pulse Accumulator Input Edge Interrupt Flag

This bit is set when an active edge is detected on the PAI input pin. This bit is cleared by a write to the TFLG2 register with bit 4 set.

Bits 3-0 - Not Implemented

These bits always read zero.

8.2 REAL TIME INTERRUPT

The real time interrupt feature on the MCU is configured and controlled by using two bits (RTR1 and RTR0) in the PACTL register to select one of four interrupt rates. The RTII bit in the TMSK2 register enables the interrupt capability. Every timeout causes the RTIF bit in TFLG2 to be set, and if RTII is set, and interrupt request is generated. After reset, one entire real time interrupt period elapses before the RTIF flag is set for the first time.

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8.3 PULSE ACCUMULATOR

The pulse accumulator is an 8-bit read/write counter which can operate in either of two modes (external event counting or gated time accumulation) depending on the state of the PAMOD control bit in the PACTL register. In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is E clock divided by two. In the gated time accumulation mode, a free-running E clock/64 signal drives the 8-bit counter, but only while the external PAI input pin is activated.

The pulse accumulator uses port A bit 7 as its PAI input, but this pin also shares function as a general purpose I/O pin and as a timer output compare pin. Normally port A bit 7 would be configure as a input when being used for the pulse accumulator. Note that even when port A bit 7 is configured for output, this pin still drives the input to the pulse accumulator.

8.3.1 Pulse Accumulator Control Register (PACTL)

Four bits in this register are used to control an 8-bit pulse accumulator system and two other bits are used to select the rate for the real time interrupt system.

	7	6	5	4	3	2	1	0	
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL
RESET	0	0	0	0	0	0	0	0	

DDRA7 - Data Direction for Port A Bit 7

0 = Input only

1 = Output

PAEN - Pulse Accumulator System Enable

0 = Pulse accumulator off

1 = Pulse accumulator on

PAMOD - Pulse Accumulator Mode

0 = External event counting

1 = Gated time accumulation

PEDGE - Pulse Accumulator Edge Control

This bit has different meanings depending on the state of the PAMOD bit.

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PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A '0' on PAI Inhibits Counting
1	1	A '1' on PAI Inhibits Counting

DDRA3 - Data Direction for Port A bit 3

0 = Input only

1 = Output

I4/O5 - Input Capture 4/Output Compare 5

0 = Output compare 5 function enable (No IC4)

1 = Input capture 4 function enable (No OC5)

RTR1 and RTR0 - RTI Interrupt Rate Selects

These two bits select one of four rates for the real rime periodic interrupt circuit (see Table 8.1, 8.2). Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

Table 8.1 Real Time Interrupt Rate versus RTR1 and RTR0 (Part1)

RTR1	RTR0	Divide E By	XTAL = 2^{23} Hz	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	2^{13}	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	2^{14}	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	2^{15}	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	2^{16}	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E clock	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 KHz

Table 8.2 Real Time Interrupt Rate versus RTR1 and RTR0 (Part2)

RTR1	RTR0	Divide E By	XTAL = 12.6 MHz	XTAL = 12.0 MHz	XTAL = 9.8304 MHz	XTAL = 7.3728 MHz
0	0	2^{13}	2.60 ms	2.73 ms	3.33 ms	4.44 ms
0	1	2^{14}	5.20 ms	5.46 ms	6.67 ms	8.89 ms
1	0	2^{15}	10.4 ms	10.9 ms	13.3 ms	17.8 ms
1	1	2^{16}	20.8 ms	21.8 ms	26.7 ms	35.6 ms
		E clock	3.15 MHz	3.0 MHz	2.4576 MHz	1.8432 MHz

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9. RESETS, INTERRUPTS, AND LOW POWER MODES

This section provides a description of the resets, interrupts, and low power modes. The computer operating properly (COP) watchdog system and clock monitor are described as part of the reset system. The interrupt description includes a flowchart to illustrate how interrupts are executed.

9.1 RESETS

Please refer to SECTION 9.1 RESETS in TMP68HC11A8.

9.2 INTERRUPTS

When an external or internal (hardware) interrupt occurs, the interrupt is not serviced until the current instruction being executed is completed. Until the current instruction is complete, the interrupt is considered pending. After completion of current instruction execution, unmasked interrupts may be serviced in accordance with an

established fixed hardware priority circuit; however, one I-bit related interrupt source may be dynamically elevated to the highest I bit priority position in the heirarchy (see 9.2.5 Highest Priority I Interrupt Register (HPRIO)).

Seventeen hardware interrupts and one software interrupt (excluding reset type interrupts) can be generated from all of the possible sources. The interrupts can be divided into two basic categories, maskable and non-maskable. In the TMP68HC11E9 fifteen of the interrupts can be masked using the condition code register I bit. In addition to being maskable by the I bit in the condition code register, all of the on-chip interrupt sources are individually maskable by local control bits.

The software interrupt (SWI instruction) is a non-maskable instruction rather than a maskable interrupt source. The illegal opcode interrupt is a non-maskable interrupt. The last interrupt source, external input to the $\overline{\text{XIRQ}}$ pin, is considered a non-maskable interrupt because once enabled, it cannot be masked by software;however, it is masked during reset and upon receipt of an interrupt at the $\overline{\text{XIRQ}}$ pin. Tables 9.2 provide a list of each interrupt, its vector location in memory, and the actual condition code and control bits that mask it. A discussion of the various interrupts is provided below. Figure 9.2 shows the interrupt stacking order.

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Table 9.2 Interrupt Vector Masks and Assignments

Vector Address	Interrupt Source	Condition Code Register Mask	Local Mask
FFC0, FFC1	Reserved	–	–
*	*		
*	*		
FFD4, FFD5	Reserved	–	–
FFD6, FFD7	SCI Serial System	I Bit	–
	Receive Data Register Full	–	RIE
	Receive Overrun	–	RIE
	Idle Line Detect	–	ILIE
	Transmit Data Register Empty	–	TIE
	Transmit Complete	–	TCIE
FFD8, FFD9	SPI Serial Transfer Complete	I Bit	SPIE
FFDA, FFDB	Pulse Accumulator Input Edge	I Bit	PAII
FFDC, FFDD	Pulse Accumulator Overflow	I Bit	PAOVI
FFDE, FFDF	Timer Overflow	I Bit	TOI
FFE0, FFE1	Timer Output Compare 5/Input capture 4	I Bit	I4O5I
FFE2, FFE3	Timer Output Compare 4	I Bit	OC4I
FFE4, FFE5	Timer Output Compare 3	I Bit	OC3I
FFE6, FFE7	Timer Output Compare 2	I Bit	OC2I
FFE8, FFE9	Timer Output Compare 1	I Bit	OC1I
FFEA, FFEB	Timer Input Capture 3	I Bit	IC3I
FFEC, FFED	Timer Input Capture 2	I Bit	IC2I
FFEE, FFEF	Timer Input Capture 1	I Bit	IC1I
FFF0, FFF1	Real-Time Interrupt	I Bit	RTII
FFF2, FFF3	$\overline{IRQ}$-External Pin	I Bit	–
	External Pin	–	None
	Parallel I/O Handshake	–	STAI
FFF4, FFF5	$\overline{XIRQ}$ Pin (Pesudo-Nonmaskable)	X Bit	None
FFF6, FFF7	SWI	None	None
FFF8, FFF9	Illegal Opcode Trap	None	None
FFFA, FFFB	COP Failure (Reset)	None	NOCOP
FFFC, FFFD	Clock Monitor Fail (Reset)	None	CME
FFFE, FFFF	$\overline{RESET}$	None	None

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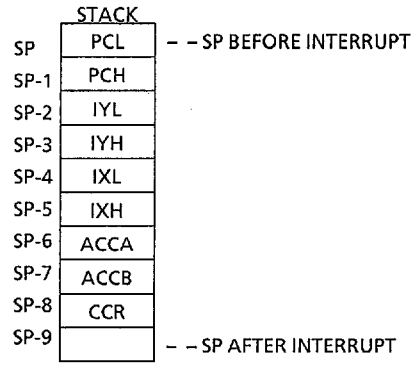

Figure 9.2 Interrupt Stacking Order

9.2.1 Software Interrupt (SWI)

The software interrupt is executed in the same manner as any other instruction and will take precedence over interrupts only if the orher interrupts are masked (I and X bits in the condition code register set). The SWI instruction is executed in a manner simslar to other maskable interrupts in that it sets the I bit, CPU registers are stacked, etc.

Note : The SWI instruction will not be fetched if another interrupt os pending. However, once an SWI instruction has begun, no other interrupt can be honored until the SWI vector has been fetched.

9.2.2 Illegal Opcode Trap

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included. When an illegal opcode is detected, an interrupt is requested to the illegal opcode vector. The illegal opcode vector should never be left unitialized. It is a good idea to reinitialize the stack pointer as a result of an illegal opcode interrupt so repeated execution of illegal opcodes does not cause stack overruns.

9.2.3 Interrupt Mask Bits in Condition Code Register

Upon reset, both the X bit and the I bit are set to inhibit all maskable interrupts and $\overline{\text{XIRQ}}$. After minimum system initialization, software may clear the X bit by a TAP instruction, thus enabling $\overline{\text{XIRQ}}$ interrupts. Thereafter software cannot set the X bit so an $\overline{\text{XIRQ}}$ interrupt is effectively a nonmaskable interrupt. Since the operation of the I bit related interrupt structure has no effect on the X bit, the external $\overline{\text{XIRQ}}$ pin remains effectively non-masked. In the interrupt priority logic, the $\overline{\text{XIRQ}}$ interrupt is a higher priority than any source that is maskable by the I bit. All I bit reated interrupts operate normally with their own priority relationship. When an I bit related interrupt occurs, the I bit is automatically set by hardware after stacking the condition code register byte, but the X bit is not affected.

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When an X bit related interrupt occurs, both the X bit and the I bit are automatically set by hardware after stacking the condition code register. An RTI (return from interrupt) instruction restores the X and I bits to their pre-interrupt request state.

9.2.4 Priority Structure

Interrupts obey a fixed hardware priority circuit to resolve simultaneous requests; however, one I bit related interrupt source may be elevated to the highest I bit priority position in the resolution circuit. The first six interrupt sources are not masked by the I bit in the condition code register and have the fixed priority interrupt relationship of: reset, clock monitor fail, COP fail, illegal opcode, and $\overline{\text{XIRQ}}$. (SWI is actually an instruction and has highest priority other than reset in the sense that once the SWI opcode is fetched, no other interrupt can be honored until the SWI vector has been fetched). Each of these sources is an input to the priority resolution circuit. The highest 1bit masked priority input to the resolution circuit is assigned under software control (of the HPRIO register) to be connected to any one of the remaining I bit related interrupt sources. In order to avoid timing races, the HPRIO register may only be written while the I bit related interrupts are inhibited (I bit in condition code register is a logic one). An interrupt that is assigned to this high priority position is still subject to masking by any associated control bits or the I bit in the condition code register. The interrupt vector address is not affected by assigning a source to this higher priority position.

Figures 9.3, 9.4, and 9.5 illustrate the interrupt process as it relates to normal processing. Figure 9.3 shows how the CPU begins from a reset and how interrupt detection relates to normal opcode fetches. Figure 9.4 is an expansion of a block in Figure 9.3 and shows how interrupt priority is resolved. Figure 9.5 is an expansion of the SCI interrupt block in Figure 9.5 shows the resolution of interrupt sources within the SCI subsystem.

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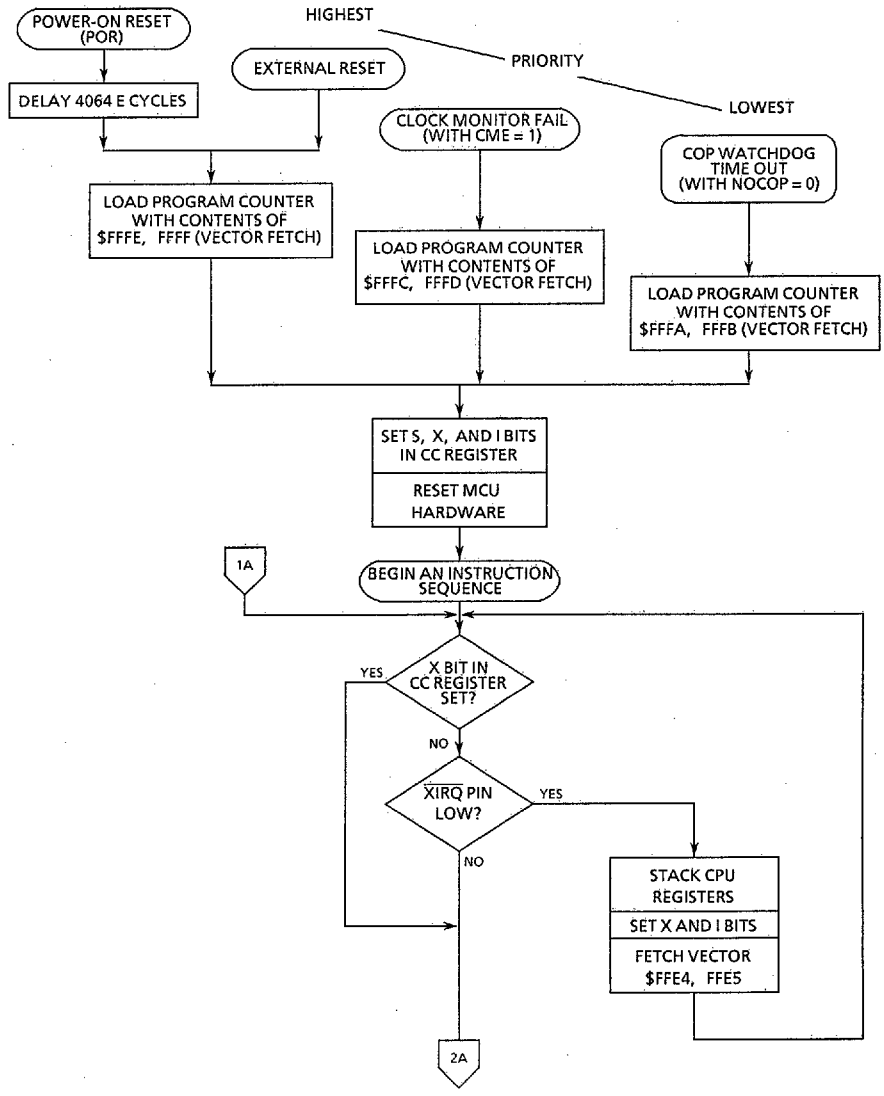

Figure 9.3 Processing Flow Out of Resets (Sheet 1of 2)

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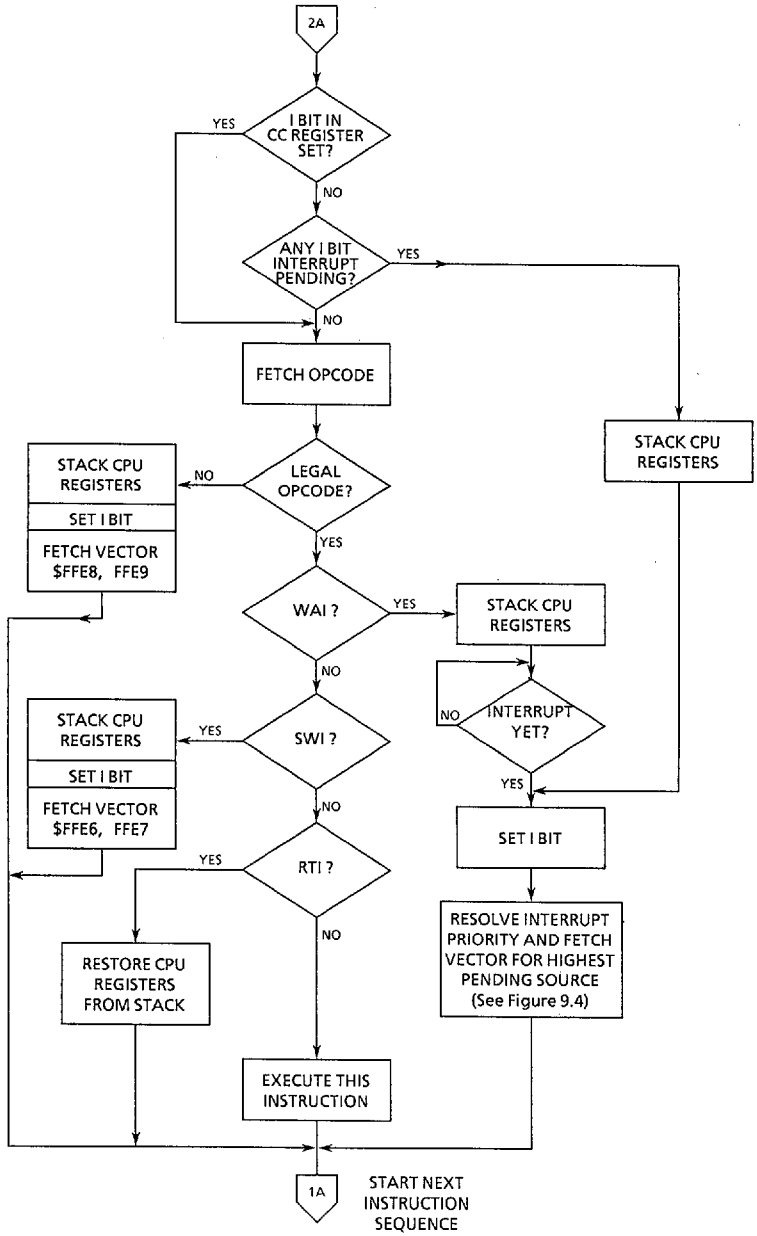

Figure 9.3 Processing Flow Out of Resets (Sheet 2 of 2)

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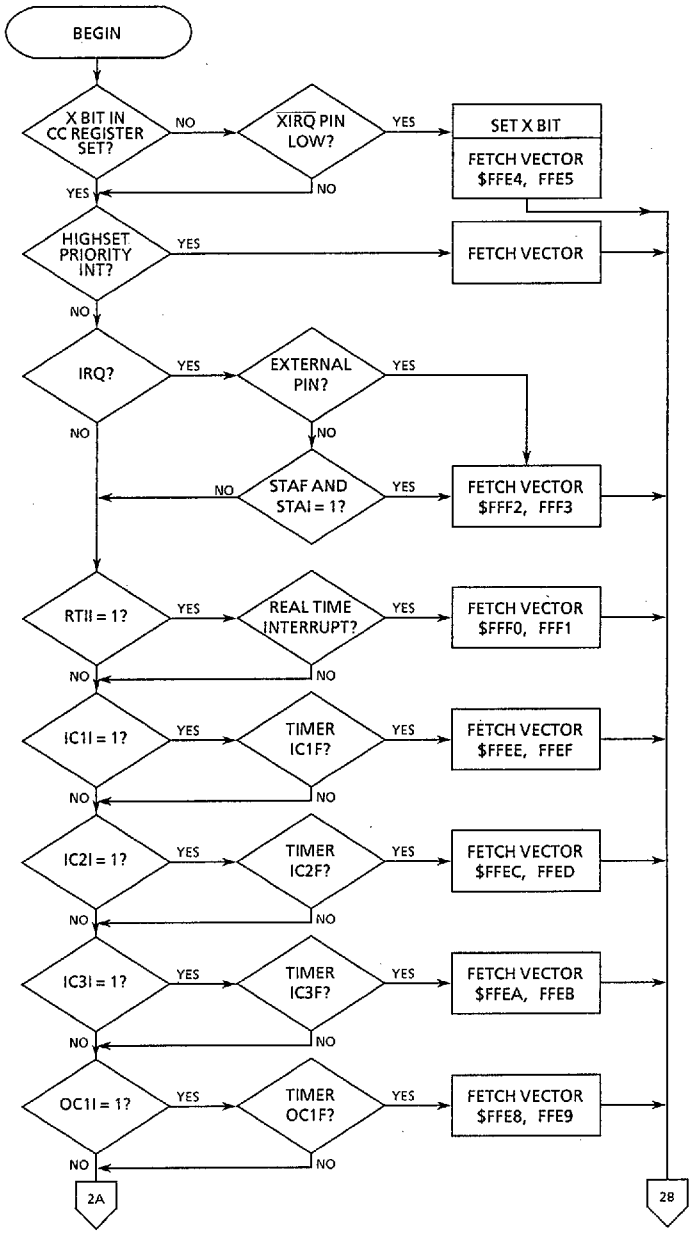

Figure 9.4 Interrupt Priority Resolution (Sheet 1 of 2)

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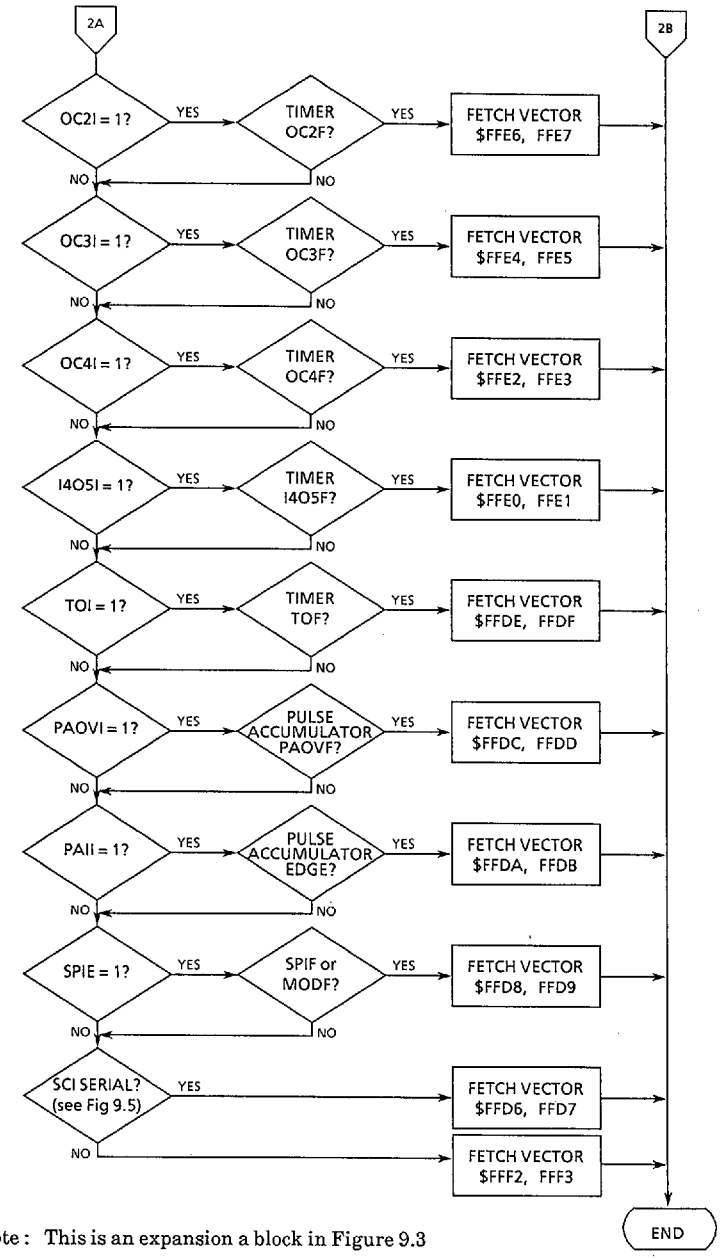

Note : This is an expansion a block in Figure 9.3

Figure 9.4 Interrupt Priority Resolution (Sheet 2 of 2)

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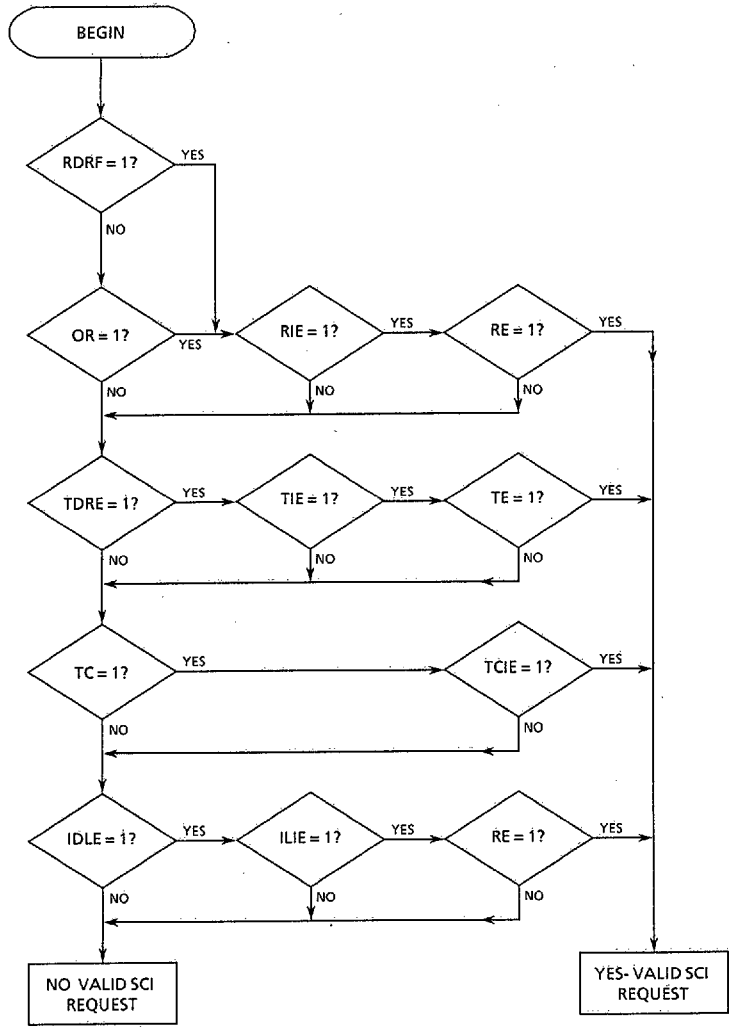

Note : This is an expansion a block in Figure 9.4

Figure 9.5 Interrupt Source Resolution Within SCI

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9.2.5 Highest Priority I Interrupt Register (HPRIO)

This register is used to select one of the I bit related interrupt sources to be elevated to the highest I bit masked position in the priority resolution circuit. In addition, four miscelleneous system control bits are included in this register.

	7	6	5	4	3	2	1	0	
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
RESET	–	–	–	–	0	1	0	1	

RBOOT - Read Bootstrap ROM

The read bootstrap ROM bit only has meaning when the SMOD bit is a one (special bootstrap mode or special test mode). At all other times, this bit is clear and may not be written. When set, upon reset in bootstrap mode only, the small bootstrap loader program is enabled. When clear, by reset in the other three modes, this ROM is disabled and accesses to this area are treated as external accesses.

SMOD - Special Mode

The special mode bit reflects the inverse of the MODB input pin at the rising edge of reset. It is set if the MODB pin is low during reset. If MODB is high during reset, it is cleared. This bit may be cleared under software control from the special modes, thus, changing the operating mode of the MCU, but may never be set by software.

MDA - Mode Select A

The mode select A bit reflects the status of the MODA input pin at the rising edge of reset. While the SMOD bit is set (special bootstrap or special test mode in effect), the MDA bit may be written, thus, changing the operating mode of the MCU. When the SMOD bit is clear, the MODA bit is a read-only bit and the operating mode cannot be changed without going through a reset sequence. Table 9.3 summarizes the relationship between the SMOD and MDA bits and the MODB and MODA input pins at the rising edge of reset.

Table 9.3 Mode Bits Relationship

Inputs		Mode Description	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single Chip	0	0
1	1	Expanded Multiplexed	0	1
0	0	Special Bootstrap	1	0
0	1	Special Test	1	1

1=Logic High 0=Logic Low

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IRV - Internal Read Visibility

The internal read visibility bit is used in the special modes (SMOD = 1) to affect visibility of internal reads on the expansion data bus. IRV is writeable only if SMOD = 1 and returns to zero if SMOD = 0. If IRV is clear, visibility of internal reads is blocked. If the bit is set, internal reads are visible on the external bus.

PSEL3, PSEL2, PSEL1, and PSEL0 - Priority Select

These four priority select bits are used to specify one I bit related interrupt source which becomes the highest priority I bit related source (Table 9.4). These bits may be written only while the I bit in CCR = 1 (interrupts masked).

Table 9.4 Highest Priority I Interrupt versus PSEL3-PSEL0

PSEL3	PSEL2	PSEL1	PSEL0	Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Serial Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{IRQ}$)
0	1	1	0	$\overline{IRQ}$ (External Pin or Parallel I / O)
0	1	1	1	Real Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5/Input Capture 4

Note: During reset, PSEL3, PSEL2, PSEL1, and PSEL0 are initialized to 0:1:0:1 which corresponds to "Reserved (default to $\overline{IRQ}$)" being the highest priority I bit related interupt source.

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9.3 LOW POWER MODES

The MCU contains two programmable low power consumption modes;WAIT and STOP. These two instructions are discussed below. Table 9.5 summarizes the activity on all pins of the MCU for all operating conditions.

9.3.1 WAIT Instruction

The WAI instruction puts the MCU in a low power consumption mode, keeping the oscillator running. Upon execution of a WAI instruction, the machine state is stacked and program execution stops. The wait state can be exited only by an unmasked interrupt or $\overline{\text{RESET}}$. If the I bit is set (interrupts masked) and the COP is disabled, the timer system will be turned off to additionally reduce power consumption. The amount of power savings is application dependent and depends upon circuitry connected to the MCU pins as well as which subsystems (i.e., timer, SPI, SCI) are active when the WAIT mode is entered. Turning off the A/D subsystem by clearing ADPU further reduces WAIT mode current.

9.3.2 STOP Instruction

The STOP instruction places the MCU in its lowest power consumption mode provided the S bit in the condition code register is clear. If the S bit is set, the STOP mode is disabled and STOP instructions are treated as NOPs (no operation). In the STOP mode, all clocks including the internal oscillator are stopped causing all internal processing to be halted. Recovery from the STOP mode may be accomplished by $\overline{\text{RESET}}$, $\overline{\text{XIRQ}}$, or an unmasked $\overline{\text{IRQ}}$. When the $\overline{\text{XIRQ}}$ is used, the MCU exits from the STOP mode regardless of the state of the X bit in the condition code register;however, the actual recovery sequence differs depending on the state of the X bit. If the X bit is clear, the MCU starts up with the stacking sequence leading to normal service of the $\overline{\text{XIRQ}}$ request. if the X bit is set, then processing will continue with the instruction immediately following the STOP instruction and no $\overline{\text{XIRQ}}$ interrupt service routine is requested. A $\overline{\text{RESET}}$ will always result in an exit from the STOP mode, and the start of MCU operation is determined by the reset vector.

Since the oscillator is stopped in the STOP mode, a restart delay of 4064 clock cycle times may be required to allow oscillator stabilization. If the internal oscillator is being used, this delay is required;however, if a stable external oscillator is being used, a control bit in the OPTION register may be used (DLY = 0) to give a delay of four cycles.

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Table 9.5 Pin State Summary for RESET, STOP, and WAIT

Pins	Single-chip mode Special Bootstrap mod			Exanded Multiplexed Special Test mode		
	RESET	WAIT	STOP	RESET	WAIT	STOP
Output Only						
E	Active E	Active E	0	Active E	Active E	0
XTAL!!!	Active	Active	1	Active	Active	1
STRB/R/$\overline{W}$	0	SS	SS	1	1	1
PA4-PA6	0	SS	SS	0	SS	SS
PB0-PB7	0	SS	SS	HI ADD	HI ADD	HI ADD
Input/Output						
RESET	I (0)	I	I	I (0)	I	I
MODA/$\overline{LIR}$	I (0)	OD (1)	OD (1)	I (1)	OD (1)	OD (1)
MODB/V_{STBY}	I (MODB)	I (V_{STBY})	I (V_{STBY})	I (MODES)	I (V_{STBY})	I (V_{STBY})
STRA/AS	I (STRA)	I (STRA)	I (STRA)	Active AS	Active AS	0
PA3, PA7	I	I/O	I/O	I	I/O	I/O
PC0-PC7	I	I/O	I/O	ADD/DATA	SP-8/DATA	I
PD0-PD5	I	I/O	I/O	I	I/O	I/O
Input Only						
EXTAL	Input Clock or Connect to Crystal with XTAL					
$\overline{IRQ}$	Terminate Unused Inputs to V_{DD}					
$\overline{XIRQ}$	Terminate Unused Inputs to V_{DD}					
PA0-PA2	Terminate Unused Inputs to V_{DD} or V_{SS}					
PE0-PE7	If Not Used, External Drive Not Required					
V_{RH}-V_{RL}	If Not Used, External Drive Not Required					

Symbols :

DATA	=	Current data present.
I	=	Input pin, if ( ) associated then this is required input state.
I/O	=	Input/output pin, state determined by data direction register.
HI ADD	=	High byte of the address.
ADD/DATA	=	Low byte of the address multiplexed with data.
OD	=	Open drain output, ( ) current output state.
SS	=	Steady state, output pin stays in current state.
SP-8	=	Address output during WAI period following WAI instruction, stack pointer value, at time of WAI, minus 8.
!!!	=	XTAL is output but not normally usable for any output function beyond crystal drive.

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10 CPU, ADDRESSING MODES, AND INSTRUCTION SET

Please refer to SECTION 10. CPU, ADDRESSING MODES, AND INSTRUCTION SET in TMP68HC11A8

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11. ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the TMP68HC11E9 MCU.

11.1 MAXIMUM RATINGS

Raing	Symbol	Value	Unit
Supply Voltage	V_{DD}	− 0.3 to + 7.0	V
Input Voltage	V_{in}	− 0.3 to + 7.0	V
Operating Temperature Range TMP68HC11E9	T_a	T_L to T_H − 40 to 85	℃
Storage Temperature Range	T_{stg}	− 55 to 150	℃
Current Drain per Pin* Excluding V_{DD}, V_{SS}, V_{RH}, and V_{RL}	I_D	25	mA

* One pin at a time, observing maximum power dissipation limits.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields;however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

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11.2 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Output Voltage I_{Load} = ± 10.0 μA (see Note 1)	All Outputs All Outputs Except $\overline{RESET}$ and MODA	VOL VOH	– V_{DD} – 0.1	0.1 –	V
Output High Voltage ILoad = -0.8mA, VDD = 4.5V (see Note 1)	All Outputs Except RESET, XTAL, and MODA	V_{OH}	V_{DD} – 0.8	–	V
Output Low Voltage I_{Load} = 1.6mA	All Outputs Except XTAL	V_{OL}	–	0.4	V
Input High Voltage	All Inputs Except $\overline{RESET}$ $\overline{RESET}$	V_{IH}	0.7 × V_{DD} 0.8 × V_{DD}	V_{DD} V_{DD}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS}	0.2 × V_{DD}	V
I/O Ports, Three-State Leakage $V_{in} = V_{IH}$ or V_{IL}	PA7, PA3, PC0-PC7, PD0-PD5, STRA/AS, MODA/$\overline{LIR}$, $\overline{RESET}$	I_{OZ}	–	± 10	μA
Input Current (see Note 2) $V_{in} = V_{DD}$ or V_{SS} $V_{in} = V_{DD}$ or V_{SS}	 PA0-PA2, $\overline{IRQ}$ $\overline{XIRQ}$ MODB/V_{STBY}	I_{in}	 – –	 ± 1 ± 10	μA
RAM Standby Voltage	Powerdown	V_{SB}	4.0	V_{DD}	V
RAM Standby Current	Powerdown	I_{SB}	–	20	μA
Total Supply Current(see Note 3) RUN: Single-Chip Mode Expanded Multiplexed Mode WAIT: All Peripheral Functions Shut Down Single-Chip Mode Expanded Multiplexed Mode STOP: No Clocks, Single-Chip Mode		I_{DD} W_{IDD} S_{IDD}	 – – – – –	 15 27 6 15 100	 mA mA mA mA μA
Input Capacitance PA7, PA3, PC0-PC7, PD0-PD5, STRA/AS, MODA/$\overline{LIR}$, $\overline{RESET}$	PA0-PA2, PE0-PE7, $\overline{IRQ}$, $\overline{XIRQ}$, EXTAL	C_{in}	– –	8 12	pF
Power Dissipation	Single Chip Mode Expanded Multiplexed Mode	P_D	– –	85 150	mW

Notes :

1. V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wire-OR mode.
2. See A/D specification for leakage current for port E.
3. All ports configured as inputs,
   $V_{IH} \geqq V_{DD} - 0.2$ V, $V_{IL} \leqq 0.2$ V, No DC loads
   EXTAL is driven with a square wave, and t_{cyc} = 476.5 ns.

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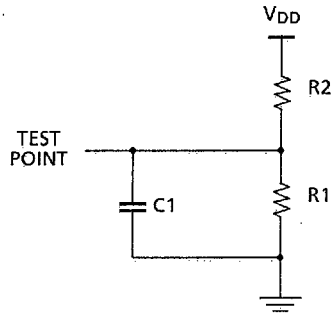
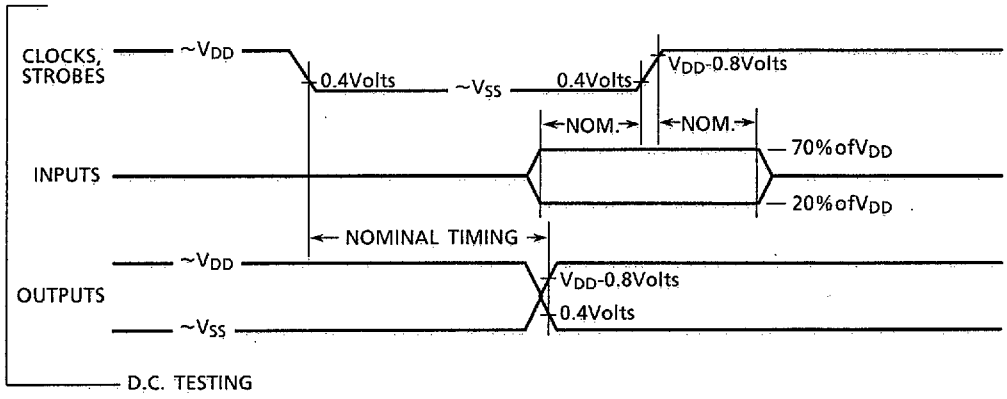
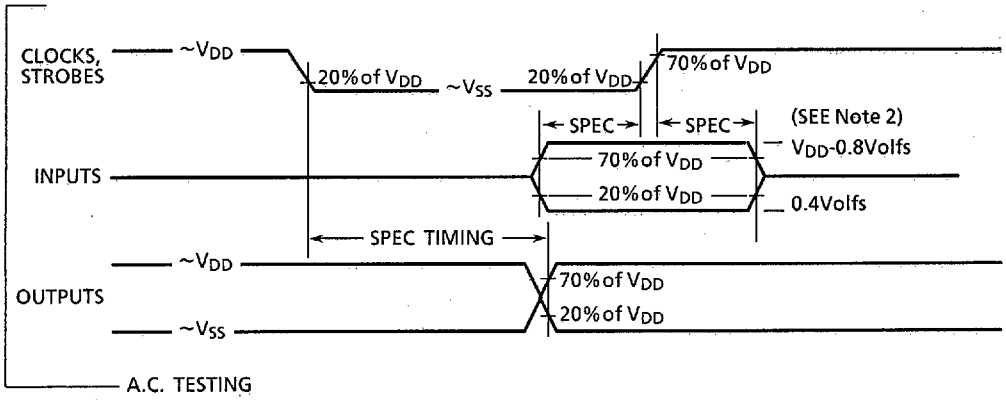


Equivalent Test Load[1]

Pins	R1	R2	C
PA3-PA7 PB0-PB7 PC0-PC7 PD0, PD5 E, AS, R/$\overline{W}$	3.26kΩ	2.38kΩ	90pF
PD1-PD4	3.26kΩ	2.38kΩ	200pF





Notes :
1. Full test loads are applied during all DC electrical and AC timing measurements.
2. During ac timing measurements, inputs are driven to 0.4 volts and V_{DD}-0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

Figure 11.1 Test Methods

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11.3 CONTROL TIMING (V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H)

Characteristic	Symbol	1.0MHz		2.0MHz		2.1MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f_O	dc	1.0	dc	2.0	dc	2.1	MHz
E Clock Period	t_{cyc}	1000	–	500	–	476	–	ns
Crystal Frequency	f_{XTAL}	–	4.0	–	8.0	–	8.4	MHz
External Oscillator Frequency	$4f_O$	dc	4.0	dc	8.0	dc	8.4	MHz
Processor Control Setup Time (see Figures 11.3, 11.5, and 11.6) $t_{PCS} = 1/4\ t_{cyc} - 50$ ns	t_{PCS}	200	–	75	–	69	–	ns
Reset Input Pulse Width (see Note 1 and Figure 11.3) (To Guarantee External Reset Vector)	PW_{RSTL}	8	–	8	–	8	–	t_{cyc}
(Minimum Input Time; May be Preempted by Internal Reset)		1	–	1	–	1	–	
Mode Programming Setup Time (see Figure 11.3)	t_{MPS}	2	–	2	–	2	–	tcyc
Mode Programming Hold Time (see Figure 11.3)	t_{MPH}	0	–	0	–	0	–	ns
Interrupt Pulse Width, IRQ Edge Sensitive Mode (see Figures 11.4 and 11.6) $PW_{IRQ} = t_{cyc} + 20$ ns	PW_{IRQ}	1020	–	520	–	496	–	ns
Wait Recovery Startup Time (See Figure 11.5)	t_{WRS}	–	4	–	4	–	4	tcyc
Timer Pulse Width Input Capture, Pulse Accumulator Input (see Figure 11.2) $PW_{TIM} = t_{cyc} + 20$ ns	PW_{TIM}	1020	–	520	–	496	–	ns

Note : 1. $\overline{\text{RESET}}$ will be recognized during the first clock cycle it is held low. Internal circuity then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to detemine the source of the interrupt. See SECTION9 RESETS, INTERRUPT, AND LOW POWER MODES for details.

2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.

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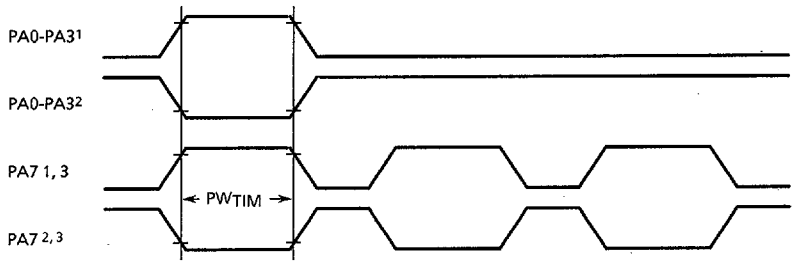
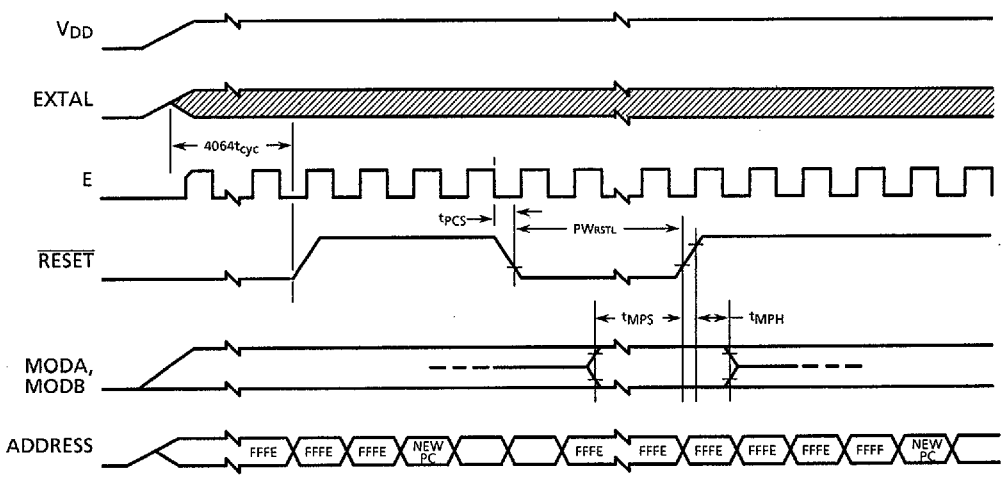


Notes :
1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E frequency divided by 2.

Figure 11.2 Timer Inputs Timing Diagram



Note : Refer to Table 9.5 for pin states during $\overline{\text{RESET}}$

Figure 11.3 POR and External Reset Timing Diagram

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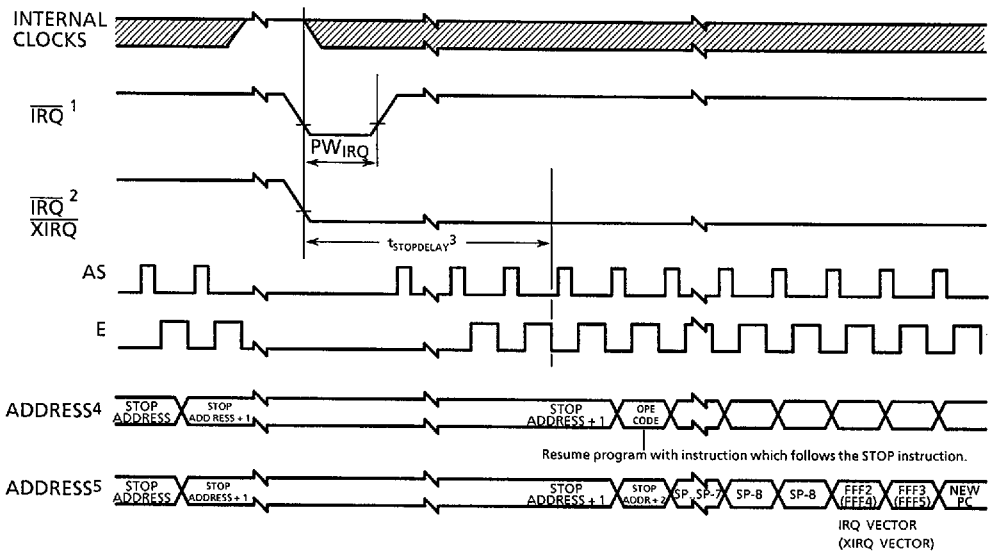
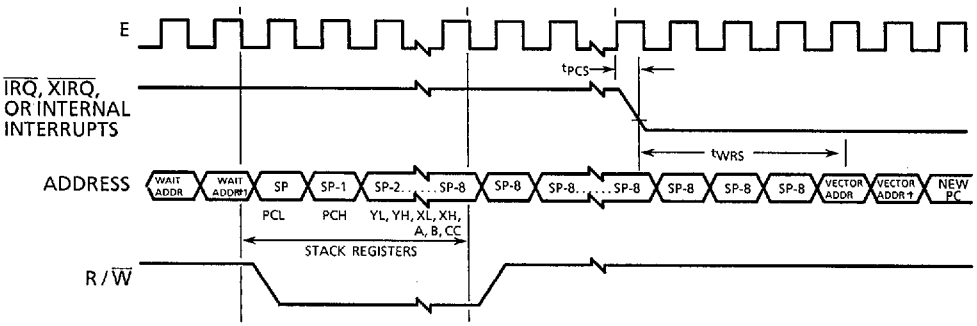


Notes :
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY} = 4064t_{cyc}$ if DLY bit = 1 or $4t_{cyc}$ if DLY = 0.
4. $\overline{XIRQ}$ with X bit CCR = 1 .
5. $\overline{IRQ}$, or ($\overline{XIRQ}$ with X bit in CCR = 0) .
6. Refer to Table 9.5 for pin states during STOP.

Figure 11.4 STOP Recovery Diagram



Notes :
1 Refer to Table 9.5 for pin states during WAIT.
2 $\overline{RESET}$ will also cause recovery from WAIT.

Figure 11.5 WAIT Recovery from Interrupt Timing Diagram

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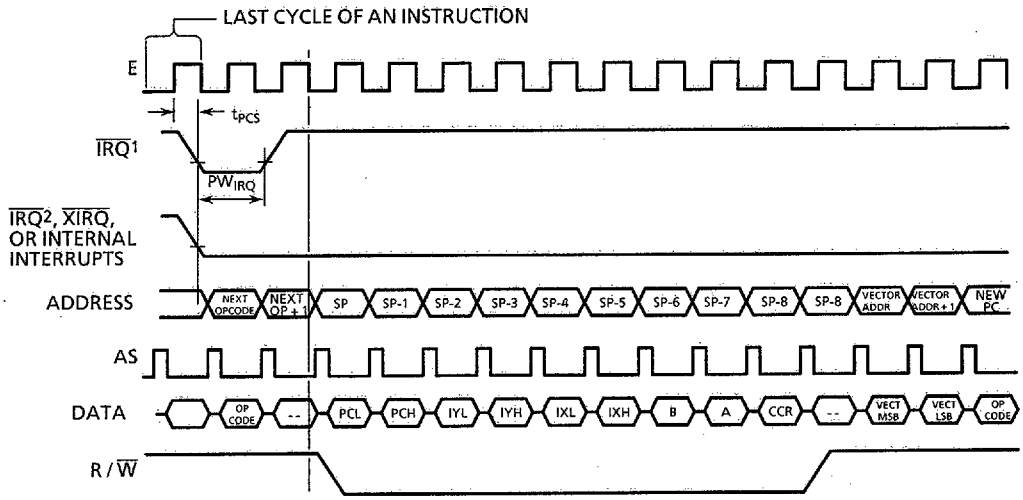

Notes :
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1).
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0).

Figure 11.6 Interrupt Timing Diagram

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11.4 PERIPHERAL PORT TIMING (V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H)

Characteristic	Symbol	1.0MHz		2.0MHz		2.1MHz		Unit
		Min	Max	Min	Max	Min	Max	
E Clock Period	t_{cyc}	1000	–	500	–	476	–	ns
Peripheral Data Setup Time (MCU Read of Ports A,C,D, and E) (see Figure 11.8)	t_{PDSU}	100	–	100	–	100	–	ns
Peripheral Data Hole Time (MCU Read of Ports A,C,D, and E) (see Figure 11.8)	t_{PDH}	50	–	50	–	50	–	ns
Delay Time, Peripheral Data Write (see Figures 11.7,11.9,11.12, and 11.13)	t_{PWD}							ns
MCU Write to Port A		–	150	–	150	–	150	
MCU Writes to Ports B,C, and D $t_{PWD} = 1/4t_{cyc} + 90$ ns		–	340	–	215	–	209	
Input Data Setup Time(Port C) (see Figure 11.10 and 11.11)	t_{IS}	60	–	60	–	60	–	ns
Input Data Hold Time(Port C) (see Figure 11.10 and 11.11)	t_{IH}	100	–	100	–	100	–	ns
Delay Time, E Fall to STRB $t_{DEB} = 1.4t_{cyc} + 100$ ns (see Figures 11.9,11.11,11.12,and 11.13)	t_{DEB}	–	350	–	225	–	219	ns
Setup Time, STRA Asserted to E Fall(see Note 1) (see Figures 11.11,11.12,and 11.13)	t_{AES}	0	–	0	–	0	–	ns
Delay Time, STRA Asserted to Port C Data Output Valid (see Figure 11-13)	t_{PCD}	–	100	–	100	–	100	ns
Hold Time, STRA Negated to Port C Data (see Figure 11.13)	t_{PCH}	10	–	10	–	10	–	ns
Three-State Hold Time (see Figure 11.13)	t_{PCZ}	–	150	–	150	–	150	ns

Notes:

1. If this setup time is met, STRB will acknowledge in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.

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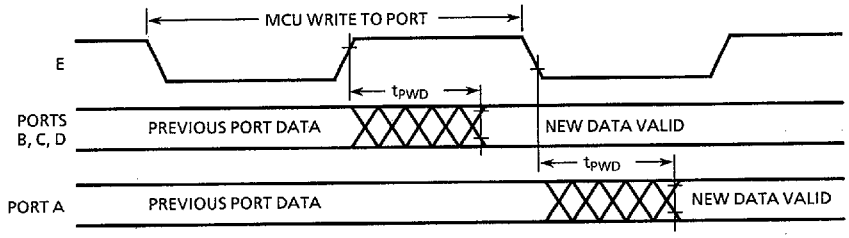
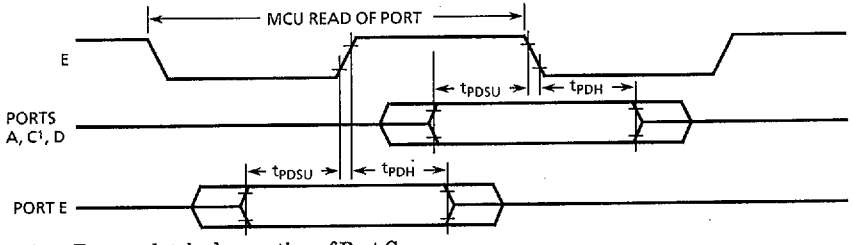


Figure 11.7 Port Write Timing Diagram



Note1 : For non-latched operation of Port C.

Figure 11.8 Port Read Timing Diagram

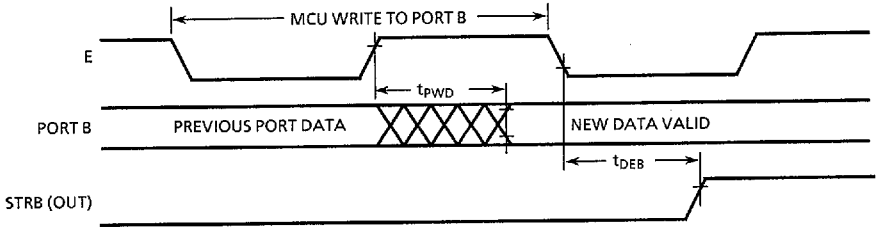


Figure 11.9 Simple Output Strobe Timing Diagram

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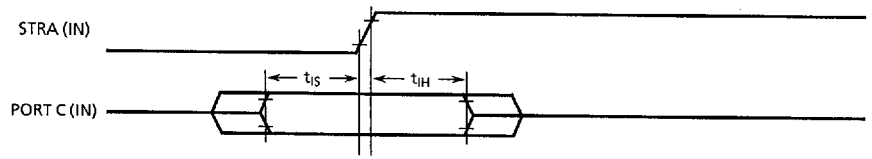
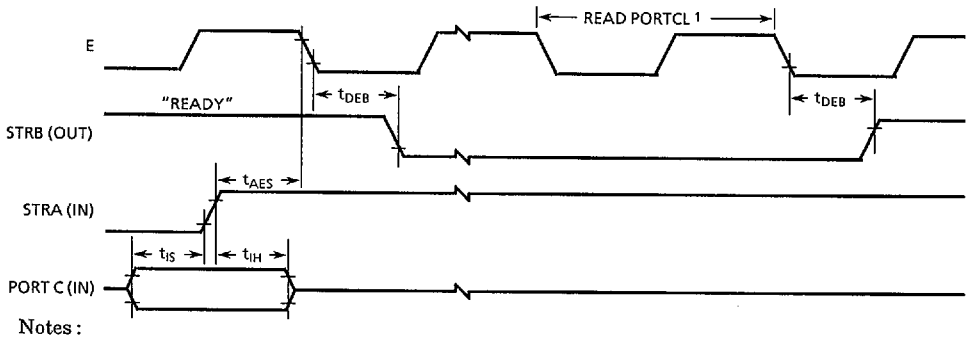
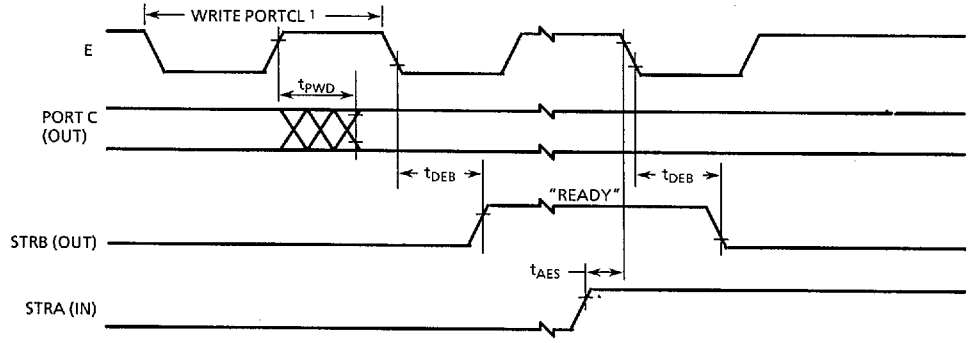


Figure 11.10 Simple Input Strobe Timing Diagram



Notes :
1. After reading PIOC with STAF set.
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 11.11 Port C Input Handshake Timing Diagram



Notes :
1. After reading PIOC with STAF set.
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 11.12 Port C Output Handshake Timing Diagram

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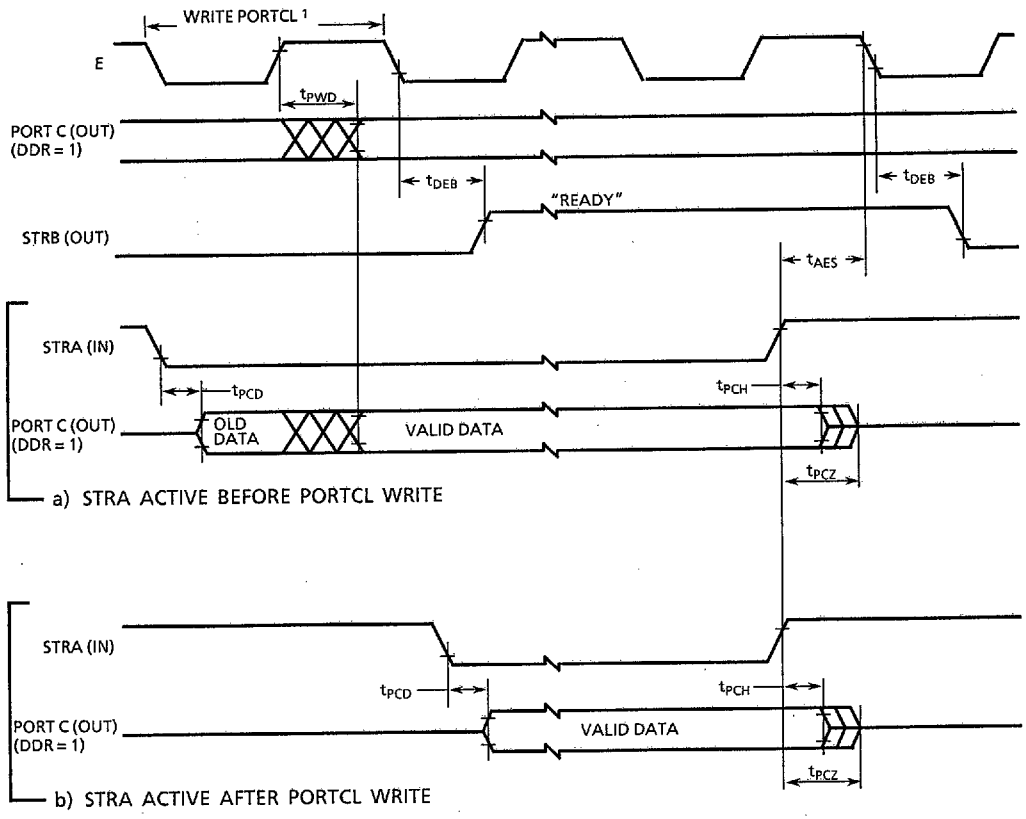

Notes :
1. After reading PIOC with STAF set.
2. Figure shows edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 11.13 Three-State Variation of Output Handshake Timing Diagram (STRA Enables Output Buffer)

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11.5 A/D CONVERTER CHARACTERISTICS(VDD = 5.0 Vdc ± 10%, VSS = 0Vdc, Ta = TL to TH, 750kHz ≦ E ≦ 2.1MHz, unless otherwise noted)

Characteristic	Parameter	Min	Absolute	Max	Unit
Resolution	Number of Bits Resolved by the A/D	8	–	–	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	–	–	± 1/2	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual A/D for Zero Input Voltage	–	–	± 1/2	LSB
Full Scale Error	Difference Between the Output of an Ideal an Actual A/D for Full-Scale Input Voltage	–	–	± 1/2	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	–	–	± 1/2	LSB
Quantization Error	Uncertainty Due to Converter Resolution	–	–	± 1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	–	–	± 1	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	–	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage (see Note 2)	V_{RL}	–	V_{DD} + 0.1	V
V_{RL}	Minimum Analog Reference Voltage (see Note 2)	V_{SS} – 0.1	–	V_{RH}	V
ΔV_R	Minimum Difference between V_{RH} and V_{RL} (see Note 2)	3	–	–	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion: a. E Clock b. Internal RC Oscillator	 – –	 32 –	 – tcyc + 32	 tcyc μs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes		Guaranteed		
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	–	–	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	–	–	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time: a. E Clock b. Internal RC Oscillator	 – –	 12 –	 – 12	 tcyc μs
Sample/Hold Capacitance	Input Capacitance during Sample PE0-PE7	–	20 (Typ)	–	pF
Input Leakage	Input Leakage on A/D Pins PE0-PE7 V_{RL}, V_{RH}	– –	– –	400 1.0	nA μA

Notes:

1. Source impedances greater than 10KΩ will adversely affect accuracy, due mainly to input leakage.
2. Performance verified down to 2.5V ΔV_R, but accuracy is tested and guaranteed at $\Delta V_R = 5V \pm 10\%$.

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11.6 EXPANSION BUS TIMING

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H, see Figure 11.14)

Num	Characteristic	Symbol	1.05MHz		2.0MHz		2.1MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1000	–	500	–	476	–	ns
2	PUlse Width, E Low $PW_{EL} = 1/2t_{cyc}$-23 ns	PW_{EL}	477	–	227	–	215	–	ns
3	PUlse Width, E High $PW_{EH} = 1/2t_{cyc}$-28 ns	PW_{EH}	472	–	222	–	210	–	ns
4	E and AS Rise and Fall Time	t_r, t_f	–	20	–	20	–	20	ns
9	Address Hold Time $t_{AV} = 1/8t_{cyc}$-29.5ns see Note 1(a)	t_{AH}	95.5	–	33	–	30	–	ns
12	Non-Muxed Address Valid Time to E Rise $t_{AV} = PW_{EL}-(t_{ASD} + 80$ ns) see Note 1(b)	t_{AV}	281.5	–	94	–	85	–	ns
17	Read Data Setup Time	t_{DSR}	30	–	30	–	30	–	ns
18	Read Data Hold Time(Max = t_{MAD})	t_{DHR}	10	145.5	10	83	10	80	ns
19	Write Data Delay Time $t_{DDW} = 1/8t_{cyc} + 65.5$ ns see Note 1(a)	t_{DDW}	–	190.5	–	128	–	125	ns
21	Write Data Hold Time $t_{DHW} = 1/8t_{cyc}$-29.5 ns see Note 1(a)	t_{DHW}	95.5	–	33	–	30	–	ns
22	Muxed Address Valid Time to E Rise $t_{AVM} = PW_{EL}-(t_{ASD} + 90$ ns) see Note 1(b)	t_{AVM}	271.5	–	84	–	75	–	ns
24	Muxed Address Valid Time to As Fall $t_{ASL} = PW_{ASH}$-70 ns	t_{ASL}	151	–	26	–	20	–	ns
25	Muxed Address Hold Time $t_{AHL} = 1/8\ t_{cyc}$-29.5 ns see Note 1(b)	t_{AHL}	95.5	–	33	–	30	–	ns
26	Delay Time,E to AS Rise $t_{ASD} = 1/8\ t_{cyc}$-9.5 ns see Note 1(a)	t_{ASD}	115.5	–	53	–	50	–	ns
27	Pulse Width, AS High $PW_{ASH} = 1/4t_{cyc}$-29 ns	PW_{ASH}	221	–	96	–	90	–	ns
28	Delay Time, AS to E Rise $t_{ASED} = 1/8t_{cyc}$-9.5 ns see Note 1(b)	t_{ASED}	115.5	–	53	–	50	–	ns
29	MPU Address Access Time $t_{ACCA} = t_{AVM} + t_r + PW_{EH}-t_{DSR}$ see note 1(b)	t_{ACCA}	733.5	–	296	–	275	–	ns
35	MPU Access Time $t_{ACCE} = PW_{EH}-t_{DSR}$	t_{ACCE}	–	442	–	192	–	180	ns
36	Muxed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30$ ns see Note 1(a)	t_{MAD}	145.5	–	83	–	80	–	ns

Notes :

1. Input clocks with duty cycles other than 50% will affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the follwing expressions in place of 1/8 t_{cyc} in the above formulas where applicable:
   (a) (1-DC) × 1/4tcyc
   (b) DC × 1/4tcyc
   Where :
   DC is the decimal value of duty cycle percentage (high time)
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless othewise noted.

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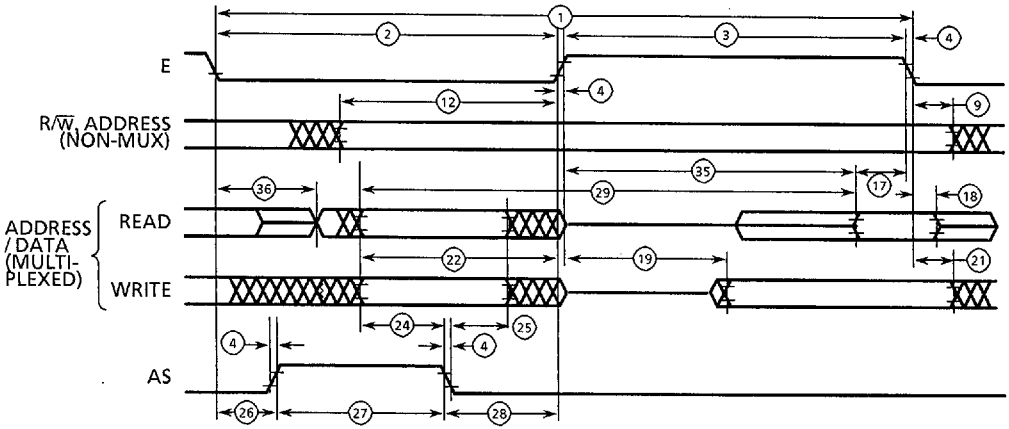

Note : Measurement point shown are 20% and 70% V_{DD}.

Figure 11.14 Expansion Bus Timing Diagram

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11.7 SERIAL PERIPHERAL INTERFACE (SPI) TIMING

(V_{DD}=5.0 Vdc±10%, V_{SS}=0 Vdc, T_a=T_L to T_H, see Figure 11.15)

Num.	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 f_{OP} (m) f_{OP} (s)	 dc dc	 1.05 2.1	 MHz MHz
1	Cycle Time Master Slave	 f_{cyc} (m) f_{cyc} (s)	 2.0 480	 – –	t_{cyc} ns
2	Enable Lead Time Master Slave	 t_{lead} (m) t_{lead} (s)	 * 240	 – –	 ns ns
3	Enable Lag Time Master Slave	 t_{lag} (m) t_{lag} (s)	 * 240	 – –	 ns ns
4	Clock (SCK) High Time Master Slave	 t_w (SCKH) $_m$ t_w (SCKH) $_s$	 340 190	 – –	 ns ns
5	Clock (SCK) Low Time Master Slave	 t_w (SCKL) $_m$ t_w (SCKL) $_s$	 340 190	 – –	 ns ns
6	Data Setup Time (Inputs) Master Slave	 t_{su} (m) t_{su} (s)	 100 100	 – –	 ns ns
7	Data Hold Time (Inputs) Master Slave	 t_h (m) t_h (s)	 100 100	 – –	 ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	 t_a	 0	 120	 ns
9	Disable Time (Hold Time to High-Impedance State) Slave	 t_{dis}	 –	 240	 ns
10	Data Valid (After Enable Edge)**	t_v (S)	–	240	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	–	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200pF) SPI Outputs(SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{rm} t_{rs}	 – –	 100 2.0	 ns μs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200pF) SPI outputs(SCK, MOSI, and MISO) SPI Inputs(SCK, MOSI, MISO, and $\overline{SS}$)	 t_{fm} t_{fs}	 – –	 100 2.0	 ns μs

*Signal production depends on software.

**Assumes 200 pF load on all SPI pins.

Note : All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

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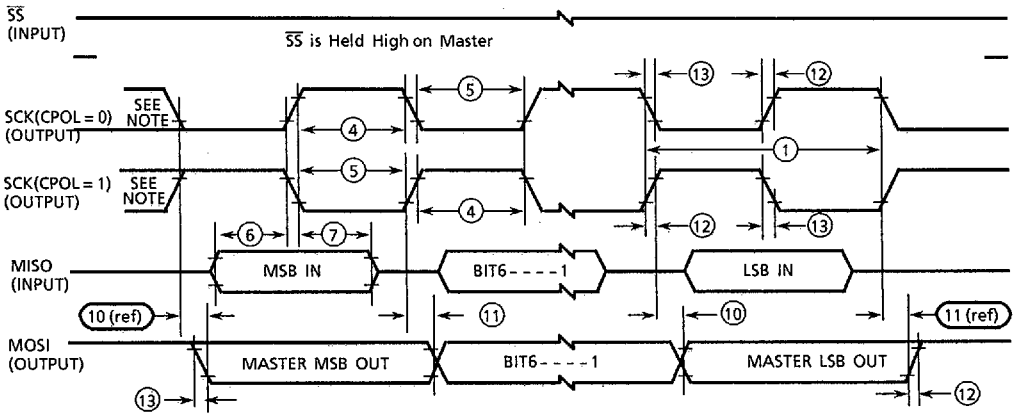
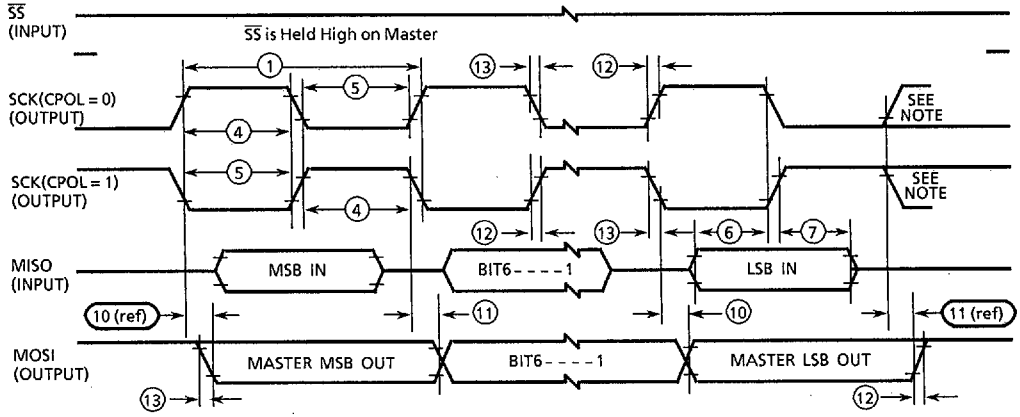


Note : This first clock edge is generated internally but is not seen at the SCK pin.

a) SPI MASTER TIMING (CPHA = 0)



Note : This last clock edge is generated internally but is not seen at the SCK pin.

b) SPI MASTER TIMING (CPHA = 1)

Figure 11.15 SPI Timing Diagrams (Sheet 1 of 2)

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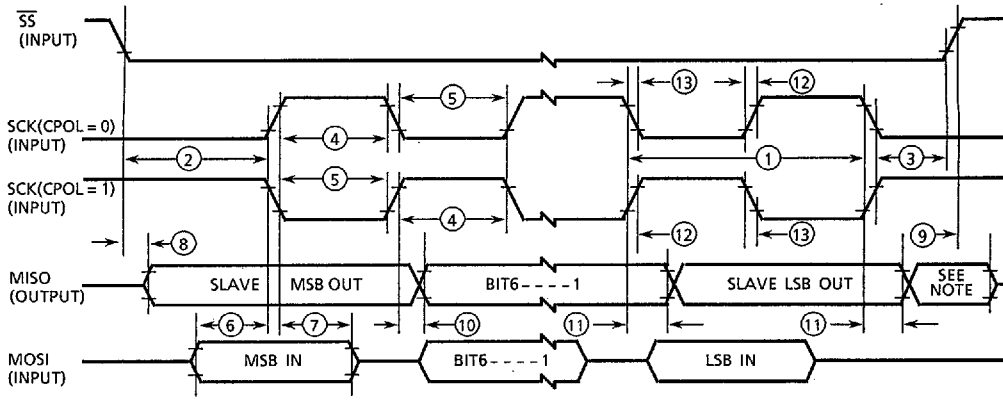
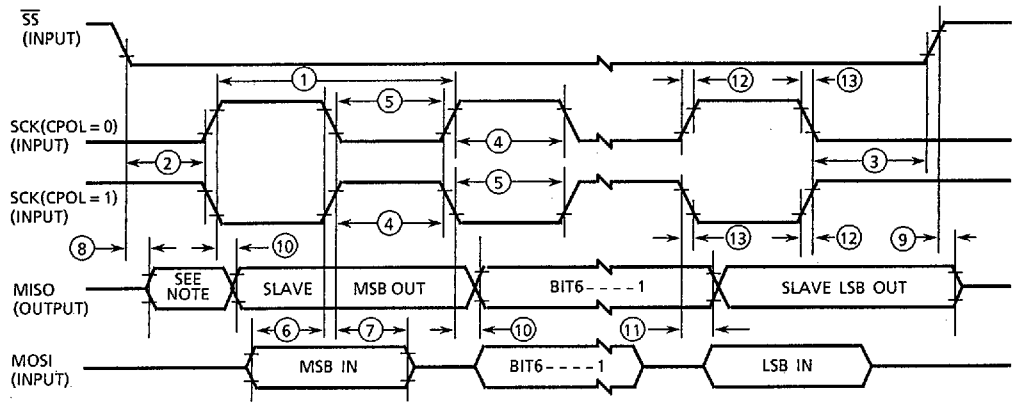


Note : Not defined but normally MSB of character just received.

c) SPI SLAVE TIMING (CPHA = 0)



Note : Not defined but normally LSB of character previously transmitted.

d) SPI SLAVE TIMING (CPHA = 1)

Figure 11.15 SPI Timing Diagrams (Sheet 2 of 2)

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11.8 EEPROM CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H)

Characteristic	Temperature Range – 40 to 85°C	Unit
Programming Time (See Note 1) Under 1.0 MHz with RC Oscillator Enable 1.0 to 2.0 MHz with RC Oscillator Disabled 2.0 MHz (or Anytime RC Oscillator Enabled)	 10 20 10	ms
Erase Time (see Note 1) Byte, Row, and Bulk	10	ms
Write/Erase Endurance	10, 000	Cycles
Data Retention	10	Years

Notes:

1. The RC oscillator must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0MHz.

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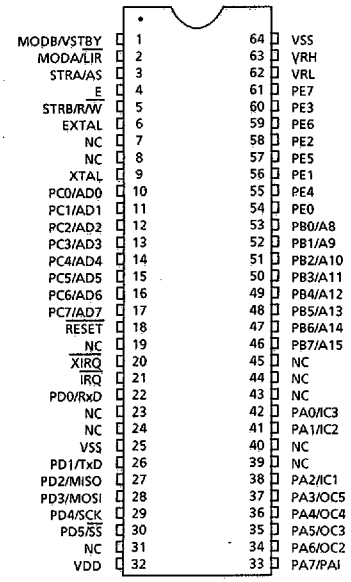
12. PIN ASSIGNMENTS

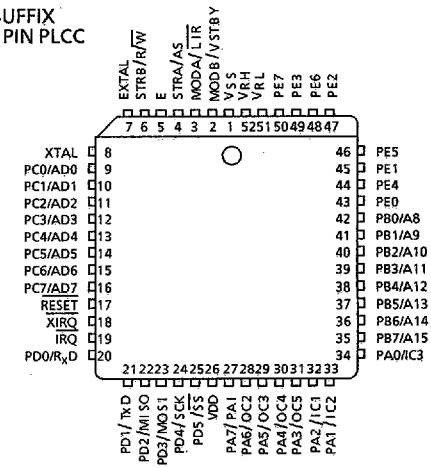
12.1 PIN ASSIGNMENTS

The TMP68HC11E9 is available in a 64-pin plastic shrink dual-in-line package (SDIP) and a 52-pin plastic lead chip carrier (PLCC) package. The following paragraphs provide pin assignments for each package versions.

N SUFFIX
64 PIN SDIP



T SUFFIX
52 PIN PLCC



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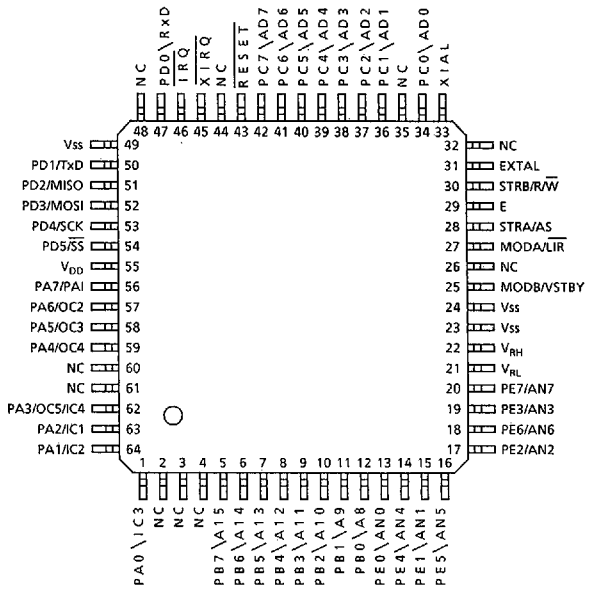
F SUFFIX
64 PIN QFP



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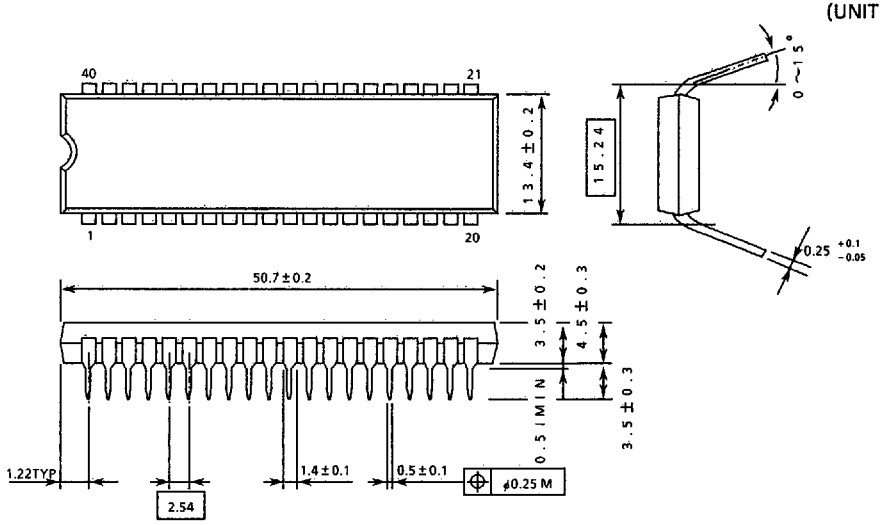
DIP40-P-600

P SUFFIX : 40PIN DIP (Dual Inline Package)

(UNIT : mm)



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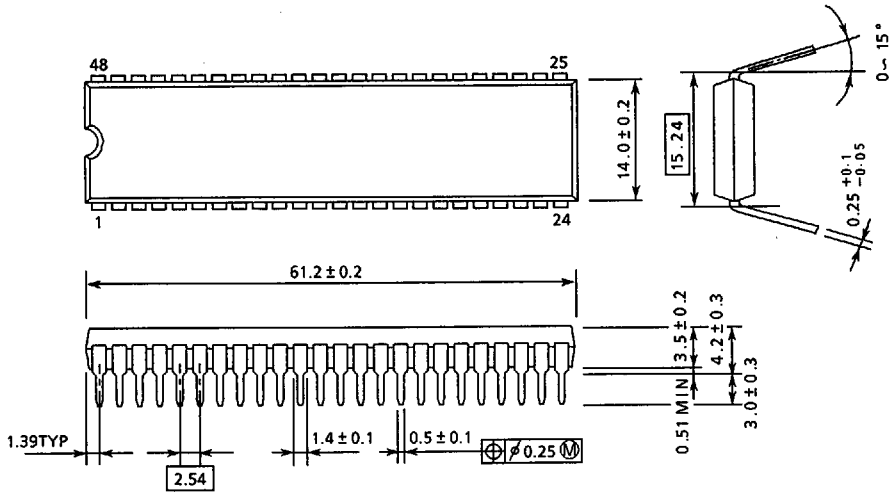
DIP48-P-600

(UNIT : mm)

P SUFFIX : 48PIN DIP (Dual Inline Package)



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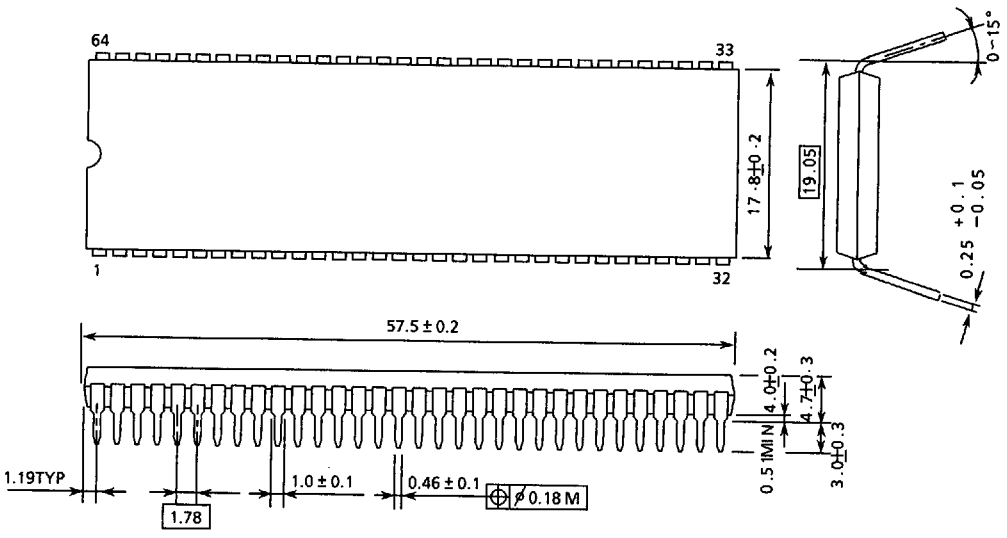
SDIP64-P-750

N SUFFIX : 64PIN SDIP (Shrink Dual Inline Package) (UNIT : mm)



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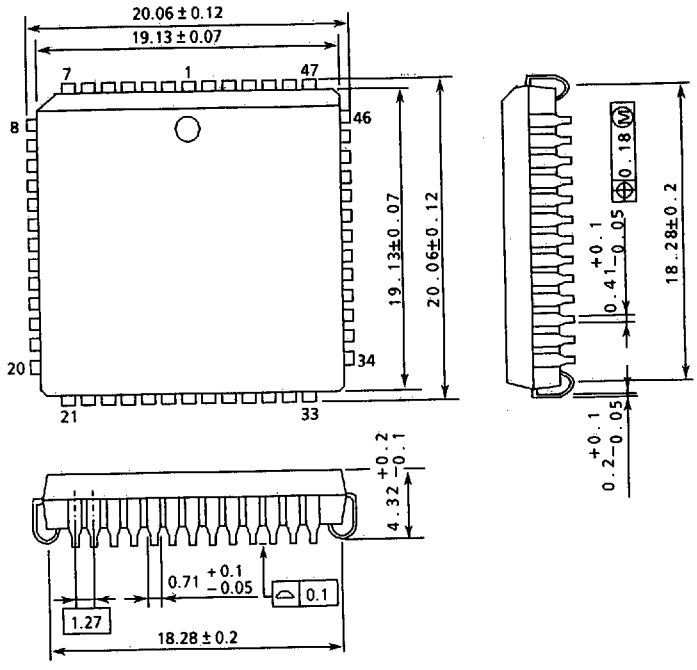
QFJ52-P-S750

T SUFFIX : 52PIN QFJ (Quad Flat J-leaded Package) (PLCC)

(UNIT : mm)



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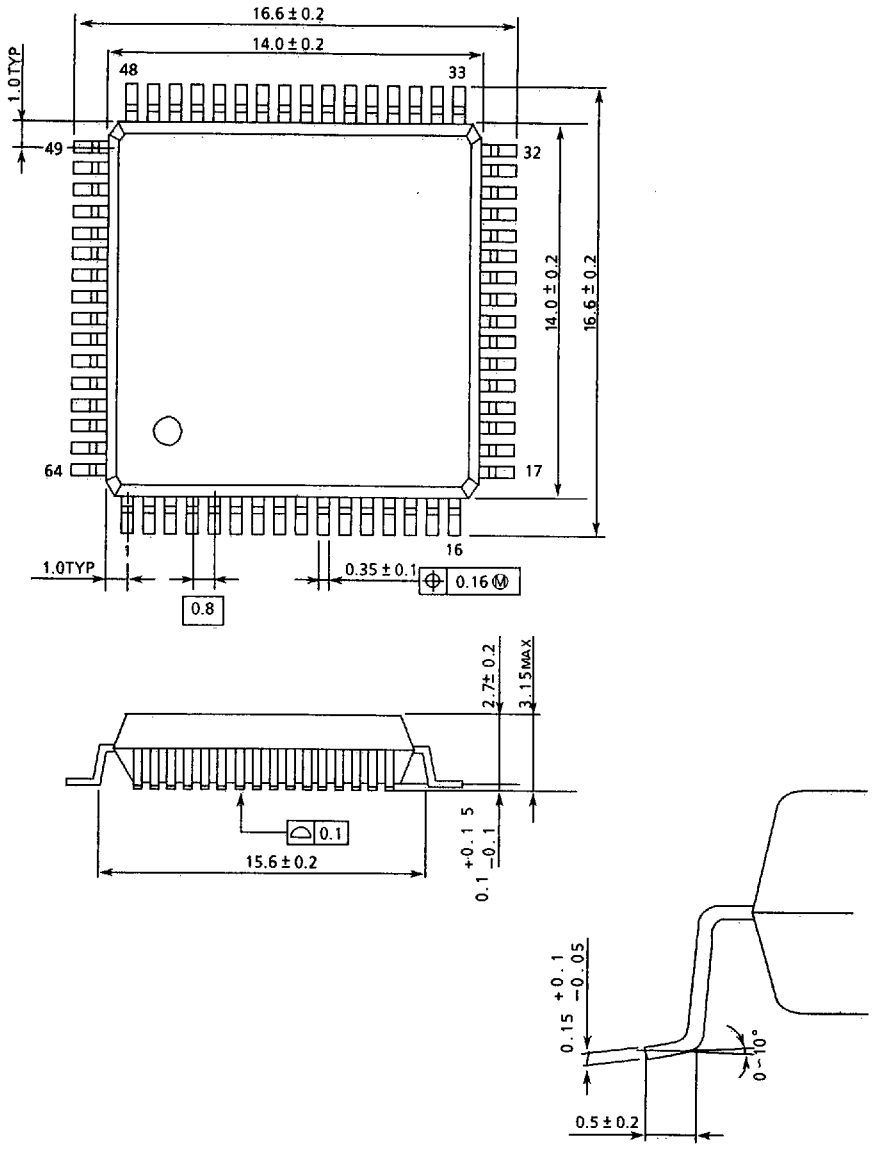
F SUFFIX 64 PIN QFP (Quad Flat Package)

(UNIT : mm)



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