TMP8155P-2/TMP8156P-2

256 BYTE STATIC RAM WITH I/O PORTS AND TIMER

1. GENERAL DESCRIPTION

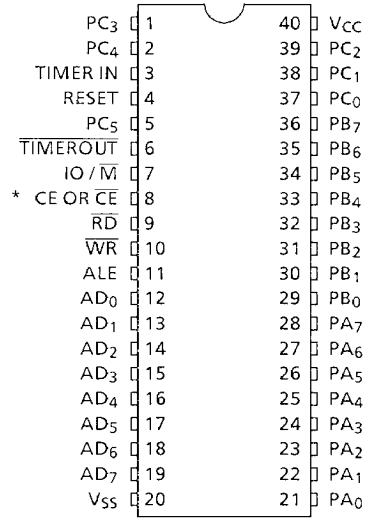
The TMP8155/8156P-2 are RAM including I/O ports and counter/timer on one chip for using in the TLCS-85A microcomputer system. The RAM portion is designed with 2K bit static memory cells organized as 256 x 8. The 14 bit programmable counter/timer is the down counter. It provides either a square wave terminal count pulse for the MPU system depending on timer mode.

The I/O portion consists of 2 programmable 8 bit I/O ports and 1 programmable 6 bit I/O port. The programmble I/O ports can be operated by BASIC MODE and STROBE MODE.

2. FEATURES

- Single +5V Power supply
- Access Time: 330 ns
- Internal Address Latch
- 2 Programmable 8 bit I/O Ports and 1 Programmable 6 bit I/O Port
- 256 x 8 bit RAM
- Programmable 14 bit Binary Counter/Timer
- Multiplexed Address/Data Bus
- Chip Enable Active High (TMP8156P-2) or Low (TMP8155P-2)
- 40 pin DIP

3. PIN CONNECTION (TOP VIEW)

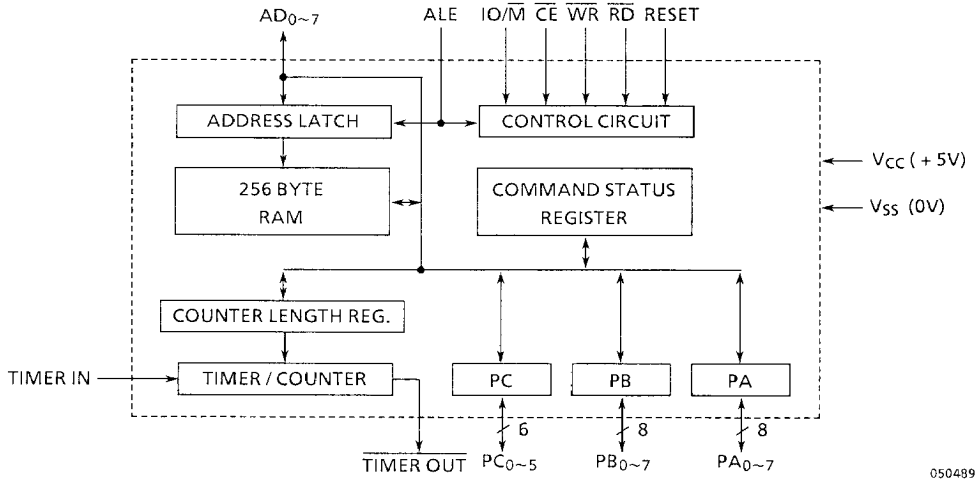


050489

Figure 3.1

Note : * TMP8155 = $\overline{CE}$
TMP8156 = CE

4. BLOCK DIAGRAM



050489

Figure 4.1

5. PIN NAMES AND PIN DESCRIPTION

- RESET (INPUT)

  The Reset signal is a pulse provided by TMP8085A to initialize the system. Input high on this line resets the chip and initializes the internal three I/O ports to input mode.

  The width of RESET pulse should typically be two clock cycles of TMP8085A.

- $AD_{0\sim7}$ (INPUT/OUTPUT, 3-STATE)

  These are 3-state Address/Data lines that interface with the MPU lower 8-bit Address/Data Bus. The 8-bit address can be applied to the memory section or the I/O section depending on the polarity of the IO/$\overline{M}$ input signal. 8-bit data is either written into or read from the TMP8155/8156 depending on the status of $\overline{WR}$ or $\overline{RD}$ input signal.

- CE OR $\overline{CE}$ (INPUT)

  Chip Enable : On the TMP8155P-2, this pin is $\overline{CE}$ and is Active Low.

  On The TMP8156P-2, this pin is CE and is Active High.

- $\overline{RD}$ (INPUT)

  Input low on this line with the Chip Enable active enables the $AD_{0\sim7}$ buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out from the $AD_{0\sim7}$ bus. Otherwise the content of the selected I/O port or command/status register will be read out from the $AD_{0\sim7}$ bus.

- $\overline{WR}$ (INPUT)

  Input low on this line with the active CE/$\overline{CE}$ causes the data on the $AD_{0\sim7}$ lines to be written to the RAM or I/O ports and command/status register depending on the polarity of IO/$\overline{M}$.

- ALE (INPUT)

  Address Latch Enable : This control signal latches both the data on the $AD_{0\sim7}$ lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.

- IO/$\overline{M}$ (INPUT)

  IO/Memory Select : This line selects the memory if low and selects the I/O or command/status register if high.

- $PA_{0\sim7}$ (INPUT/OUTPUT, 3-STATE)

  These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command Register.

- PB $_{0\sim7}$ (INPUT/OUTPUT, 3-STATE)
  These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command Register.

- PC $_{0\sim5}$ (INPUT/OUTPUT, 3-STATE)
  These 6 pins can function as either input port, output port, or as control signal for PA and PB. Programming is done through the Command Register.
  When PC $_{0\sim5}$ are used as control signals, they are defined as the following :

  PC0 - A INTR (Port A Interrupt)
  PC1 - A BF (Port A Buffer Full)
  PC2 - A $\overline{\text{STB}}$ (Port A Strobe)
  PC3 - B INTR (Port B Interrupt)
  PC4 - B BF (Port B Buffer Full)
  PC5 - B $\overline{\text{STB}}$ (Port B Strobe)

- TIMER IN (INPUT)
  This is the input to the counter-timer.

- $\overline{\text{TIMEROUT}}$ (OUTPUT)
  This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.

- VCC (Power)
  +5 volt supply

- VSS (Power)
  Ground Reference

6. FUNCTIONAL DESCRIPTION

6.1 PROGRAMMING THE COMMAND REGISTER

The command register consists of either latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when is acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXX000 during a WRITE operation. The functions of each bit of the command register is shown in Figure 6.1

Note that the command register is a write-only register and can not be read.

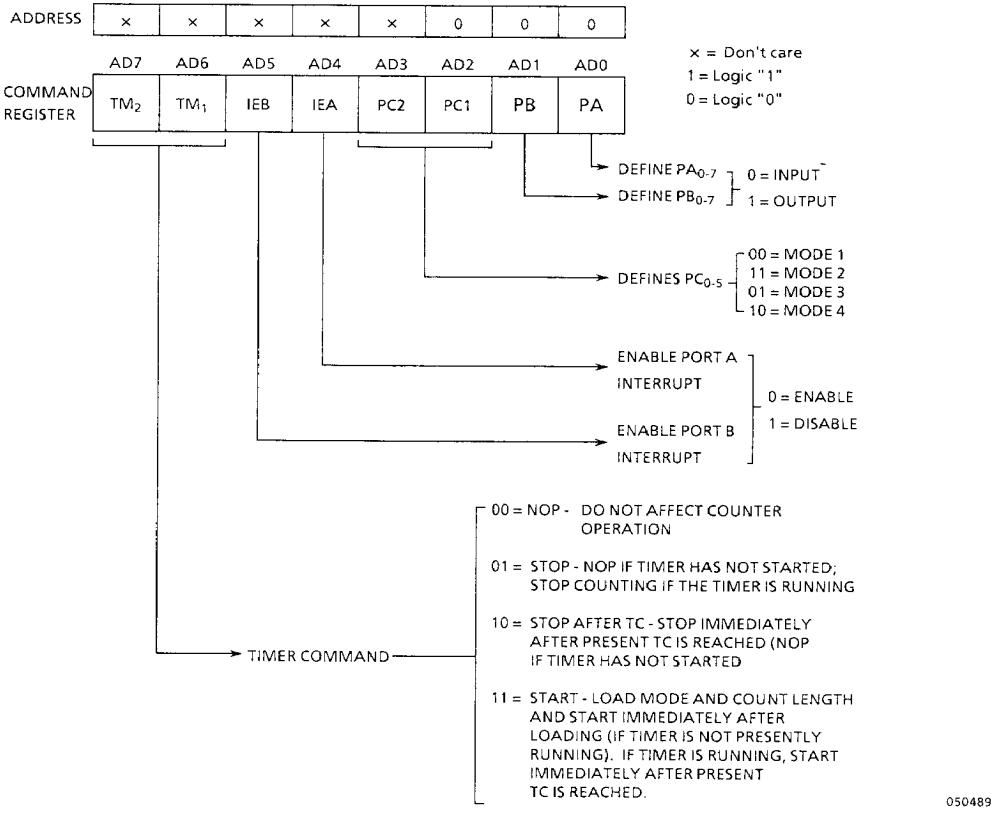


Figure 6.1 Command Register Bit Assignment

6.2 READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit ; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXX000). Status word format is shown in Figure 6.2.

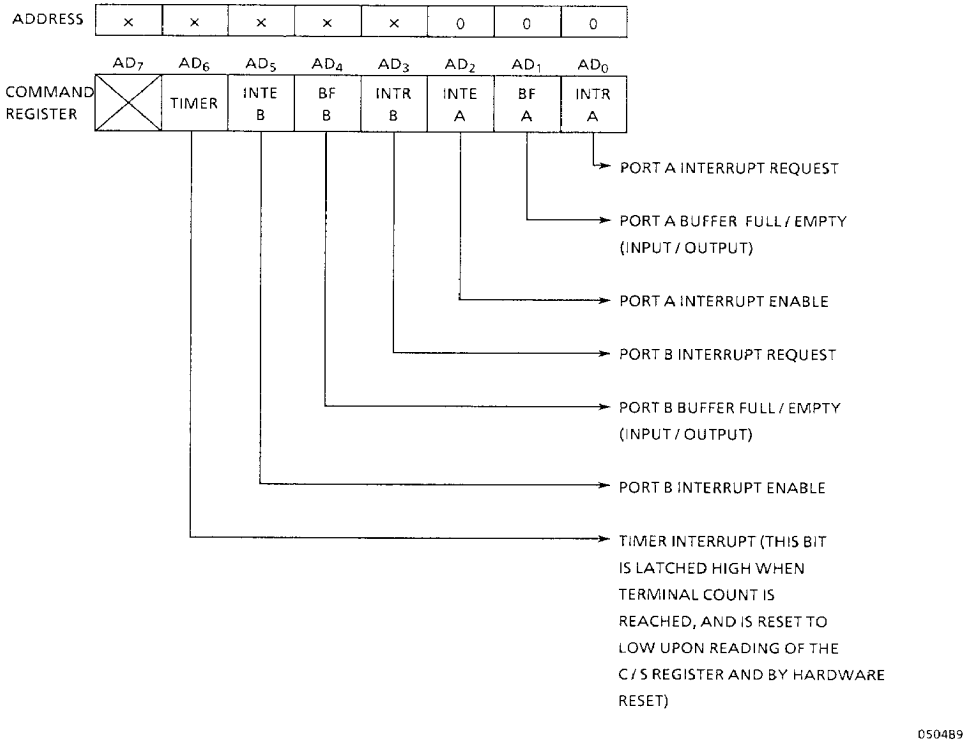


Figure 6.2 Status Register Bit Assignment

6.3 I/O SECTION

- COMMAND/STATUS REGISTER (C/S) – Both registers have the same address XXXXX000. When the C/S registers are selected during WRITE operation, a command is written into the C/S Register. The contents of this register are not accessible through the pins. When the C/S is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the $AD_{0\sim7}$ lines.

- PA Register – This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register.
  Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are $PA_{0\text{-}7}$. The address of this register is XXXXX001.

- PB Register – This register functions the same as PA Register. The I/O pins assigned are $PB_{0\text{-}7}$. The address of this register is XXXXX010.

- PC Register – This register has the address XXXXX011 and contains only 6-bits. The 6-bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S Register.
  When $PC_{0\text{-}5}$ is used as a control port, 3-bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the TMP8155/8156 issues. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 6.2.
  When the port C is programmed to either MODE 3 or MODE 4, the control signals for PA and PB are initialized as follows :

CONTROL MODE	BF	INTR	$\overline{STB}$
INPUT MODE	Low	Low	Input Control
OUTPUT MODE	Low	High	Input Control

050489

To summarize, the register's address assignments are shown in Table 6.1.

Table 6.1 I/O Port Addressing Scheme

I/O ADDRESS									SELECTION	NO. OF BITS
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
X	X	X	X	X	0	0	0	Internal	Command / Status Register	8
X	X	X	X	X	0	0	1	PA_{0-7}	General Purpose I / O Port A	8
X	X	X	X	X	0	1	0	PB_{0-7}	General Purpose I / O Port B	8
X	X	X	X	X	0	1	1	PC_{0-7}	General Purpose I / O Port or Control	6
X	X	X	X	X	1	0	0		Low-Order 8 bits of Timer Count	
X	X	X	X	X	1	0	1		High 6 bits / 2 bits of Timer Count	

050489

Table 6.2 Port Control Assignment

Pin	MODE 1	MODE 2	MODE 3	MODE 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A strobe)	A $\overline{STB}$ (Port A strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B strobe)

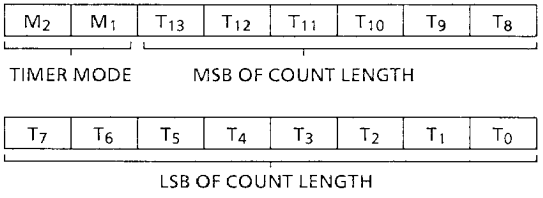
050489

6.4 TIMER SECTION

The timer is a 14-bit down-counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order of the register.

To program the timer, the COUNT LENGTH REGISTER is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode. The value loaded into the count length register can have any value from 2H through 3FFFH in bits 0-13.



0504B9

Figure 6.3 Timer Format

There are four timer modes which are defined by M2 and M1.

M2 M1

0 0 ——— Put out low during second half of count.

0 1 ——— Continuous square wave; The period of the square-wave equals the count length programmed with automatic reload at terminal count.

1 0 ——— Single pulse upon TC being reached.

1 1 ——— Continuous pulses.

Note : In case of an odd-numbered count, the first half-cycle of the square-wave output, which is high, is one count longer than the second (low) half-cycle as shown in Figure 6.3.

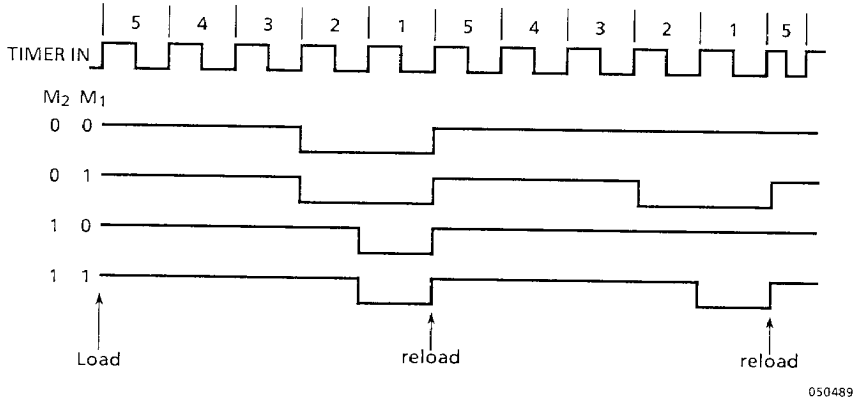


Figure 6.3 Asymmetrical Square-Wave Output resulting from Count 5

Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from;

TM2	TM1	
0	0	NOP : Do not affect counter operation.
0	1	STOP : NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC : Stop immediately after present TC is reached. (NOP if timer has not started)
1	1	START : Load mode and count length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and count length immediately after present TC is reached.

Note that while the counter is counting, a new count and mode can be loaded into the count length registers. Before the new count and mode will be used by the counter, a START command should be issued to the counter. This applies even though only the change of the count is required in the previous (same) mode.

The counter in the TMP8155/8156 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting.

Therefore a START command must be issued via the C/S register, because counting cannot begin following RESET.

Note that the timer circuit on the TMP8155/8156 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by two twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. Counter value '1' can't be loaded as the initial value into the count register because the timer operates as its terminal count value is 10 (binary). After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, the following operations should be done in order :

1. Stop the count.
2. Read in the 16-bit value from the count length registers.
3. Reset the upper two mode bits.
4. Reset the carry and rotate right one position all 16 bits through carry.
5. If carry is set, add 1/2 of the full original count (1/2 full count^{-1} if full count is odd.)

Note : When the initial count value is odd and the third count pulse has not come yet, it will be unknown whether one or two counts has occurred. Regardless of this, the TMP8155/8156 always counts out the right number of pulses in generating the $\overline{\text{TIMEROUT}}$ waveforms.

7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Units
V_{CC}	V_{CC} Supply Voltage with Respect to Vss	−0.5 to +7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260	°C
T_{STG}	Storage Temperature	−55 to +150	°C
T_{OPR}	Operating Temperature	0 to +70	°C

050489

7.2 D.C. CHARACTERISTICS

$TA = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	$V_{CC}+0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2mA$	−	0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	−	V
I_{IL}	Input Leakage	$V_{IN} = V_{CC}$ to 0V	−	±10	μA
I_{LO}	Output Leakage Current	$0.45V \leqq V_{OUT} \leqq V_{CC}$	−	±10	μA
I_{CC}	V_{CC} Supply Current		−	180	mA
I_{IL} (CE)	Chip Enable Leakage 8155 8156	$V_{IN} = V_{CC}$ to 0V.	−	 +100 −100	 μA μA

050489

7.3 A.C. CHARACTERISTICS

$TA = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameters	Min.	Max.	Units
t_{AL}	Address to Latch Setup Time	30	—	ns
t_{LA}	Address Hold Time after Latch	30	—	ns
t_{LC}	Latch to READ / WRITE Control	40	—	ns
t_{RD}	Valid Data out Delay from READ Control	—	140	ns
t_{AD}	Address Stable To Data Out Valid	—	330	ns
t_{LL}	Latch Enable Width	70	—	ns
t_{RDF}	Data Bus Float after READ	0	80	ns
t_{CL}	READ / WRITE Control Latch Enable	10	—	ns
t_{CC}	READ / WRITE Control Width	200	—	ns
t_{DW}	Data in to WRITE Setup Time	100	—	ns
t_{WD}	Data in Hold Time After WRITE	0	—	ns
t_{RV}	Recovery Time Between Controls	200	—	ns
t_{WP}	WRITE to Port Output	—	300	ns
t_{PR}	Port Input Setup Time	50	—	ns
t_{RP}	Port Input Hold Time	10	—	ns
t_{SBF}	Strobe to Buffer Full	—	300	ns
t_{SS}	Strobe Width	150	—	ns
t_{RBE}	READ to Buffer Empty	—	300	ns
t_{SI}	Strobe to INTR On	—	300	ns
t_{RDI}	Strobe to INTR Off	—	300	ns
t_{PSS}	Port Setup Time to Strobe	20	—	ns
t_{PHS}	Port Hold Time after Strobe	100	—	ns
t_{SBE}	Strobe to Buffer Empty	—	300	ns
t_{WBF}	WRITE to Buffer Full	—	300	ns
t_{WI}	WRITE to INTR Off	—	300	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMEROUT}}$ Low	—	300	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMEROUT}}$ High	—	300	ns
t_{RDE}	Data Bus Enable from READ Control	10	—	ns
t_L	TIMER-IN Low Time	40	—	ns
t_H	TIMER-IN High Time	70	—	ns
t_{CYC}	CLK Cycle Period	200	—	ns
t_r, t_f	CLK Rise and Fall Time	—	30	ns
t_{WT}	WRITE to TIMER-IN (for writes which start counting)	200	—	ns

230589

Notes : 1. Test conditions CL = 150pF
2. Timing defining signal voltage are ;
Output High level = 2V, Low level = 0.8V

8. TIMING WAVEFORMS

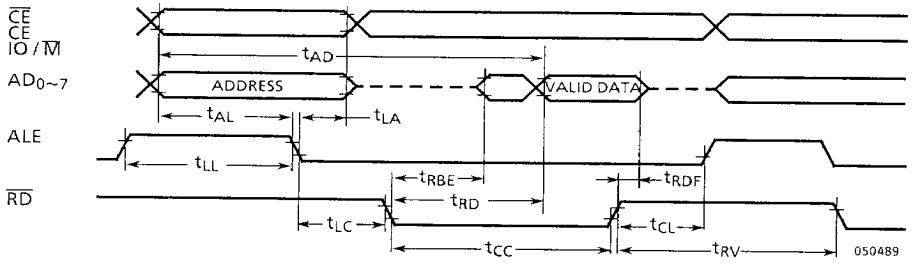


Figure 8.1 READ CYCLE

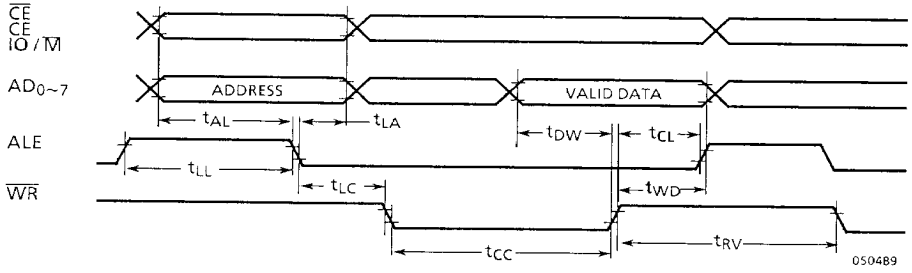


Figure 8.2 WRITE CYCLE

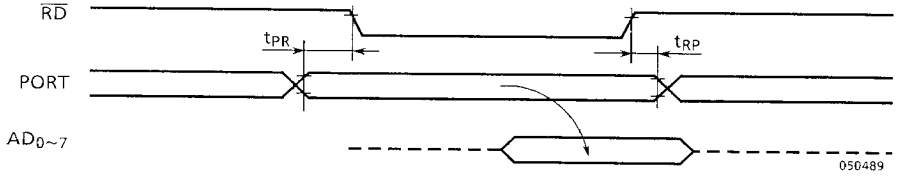


Figure 8.3 BASIC INPUT MODE

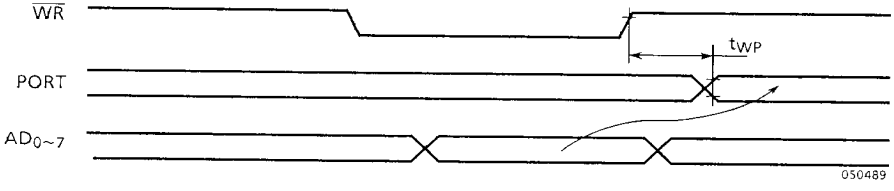


Figure 8.4 BASIC OUTPUT MODE

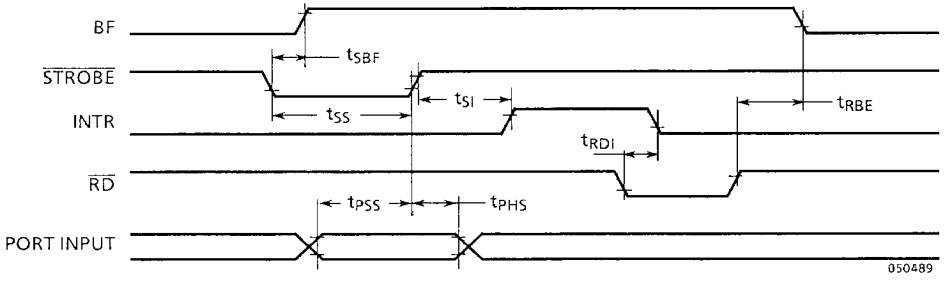


Figure 8.5 STROBED INPUT MODE

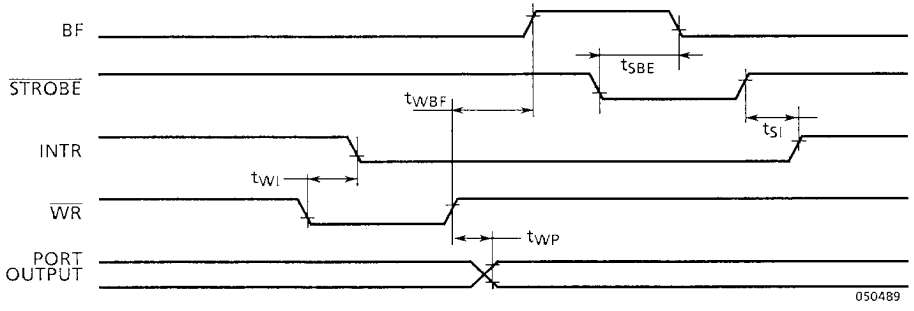


Figure 8.6 STROBED OUTPUT MODE

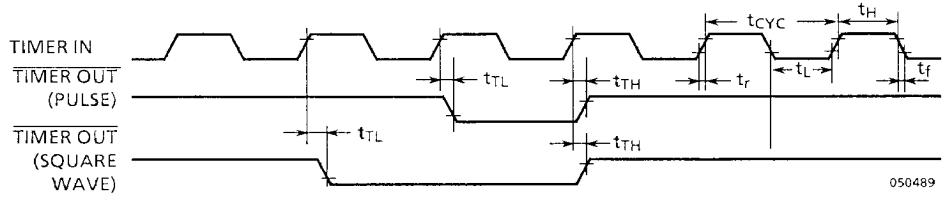
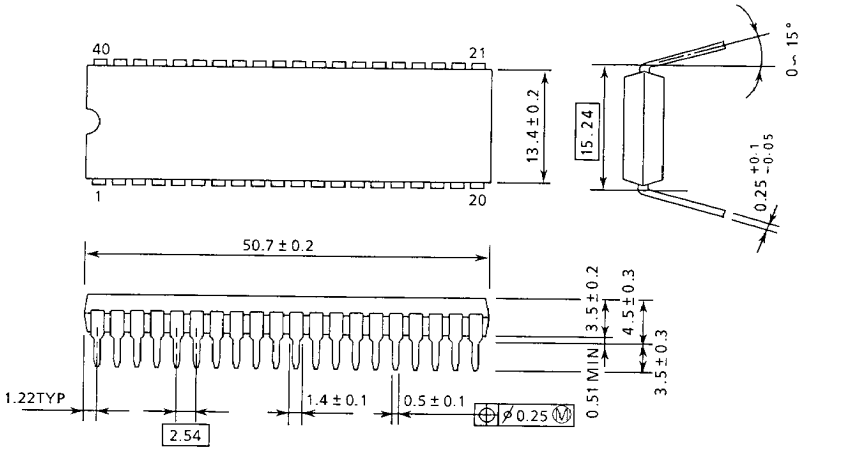


Figure 8.7 TIMER OUTPUT WAVEFORM

9. OUTLINE DRAWING (40Pins Plastic Package)

DIP40-P-600

Unit : mm



270289

Note : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No. 1 and No. 40 leads.