

P-channel enhancement mode vertical DMOS FET

ZVP0540

FEATURES

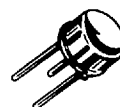
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0540A	-400V	-0.045A	150 Ω
ZVP0540B	-400V	-0.1A	150 Ω

ZVP0540

ZETEX SEMICONDUCTORS

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	-400	-400	V
I_D	Continuous drain current (@ $T_A = 25^\circ\text{C}$)	-0.045	-0.045	A
I_D	Continuous drain current (@ $T_C = 25^\circ\text{C}$)	-	-0.100	A
I_{DM}	Pulsed drain current	-0.40	-0.40	A
V_{GS}	Gate-source voltage	± 20	± 20	V
P_D	Max. power dissipation (@ $T_A = 25^\circ\text{C}$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25^\circ\text{C}$)	-	5	W
T_J, T_{stg}	Operating/storage temperature range	-55 to +150		$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (at $T = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	-400	-	V	$I_D = -1\text{mA}$, $V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate-source threshold voltage	-1.5	-4.5	V	$I_D = -1\text{mA}$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	-	20	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
I_{DSS}	Zero gate voltage drain current	-	-20	μA	$V_{DS} = \text{Max. rating}$, $V_{GS} = 0\text{V}$
		-	-2	mA	$V_{DS} = 0.8 \times \text{Max. rating}$ $V_{GS} = 0\text{V}$ ($T = 125^\circ\text{C}$) (2)
$I_{D(on)}$	On-state drain current (1)	-100	-	mA	$V_{DS} = -25\text{V}$, $V_{GS} = -10\text{V}$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	-	150	Ω	$I_D = -50\text{mA}$, $V_{GS} = -10\text{V}$
g_{fs}	Forward transconductance (1) (2)	40	-	mS	$V_{DS} = -25\text{V}$, $I_D = -50\text{mA}$
C_{iss}	Input capacitance (2)	-	120	pF	$V_{DS} = -25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
C_{oss}	Common source output capacitance (2)	-	20	pF	
C_{rss}	Reverse transfer capacitance (2)	-	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	-	10	ns	$V_{DD} \approx -25\text{V}$, $I_D = -50\text{mA}$
t_r	Rise time (2) (3)	-	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	-	15	ns	
t_f	Fall time (2) (3)	-	20	ns	

(1) Measured under pulsed conditions. Width = $300\mu\text{s}$. Duty cycle $\leq 2\%$.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and $< 5\text{ns}$ rise time on a pulse generator.