Digital NTSC Encoder
BU1414AK

This IC converts digital RGB input to analog video signals in the NTSC format.

●Applications
Video CDs (NTSC)

●Features
1) Supports 13.5MHz input clocks, ideal for NTSC video CDs
2) Input signal is RGB 24-bit
3) Master system compatible
4) Three channels (NTSC, Y and C) are output via 9-bit, high-speed DAC (internal 75Ω driver)
5) Single 5.0V power supply

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}, AV_{DD}, DV_{DD}	−0.5~7.0	V
Input voltage	V_{IN}	−0.5~V_{DD}+0.5	V
Storage temperature	Tstg	−55~150	℃
Power dissipation	P_d	1375*1	mW

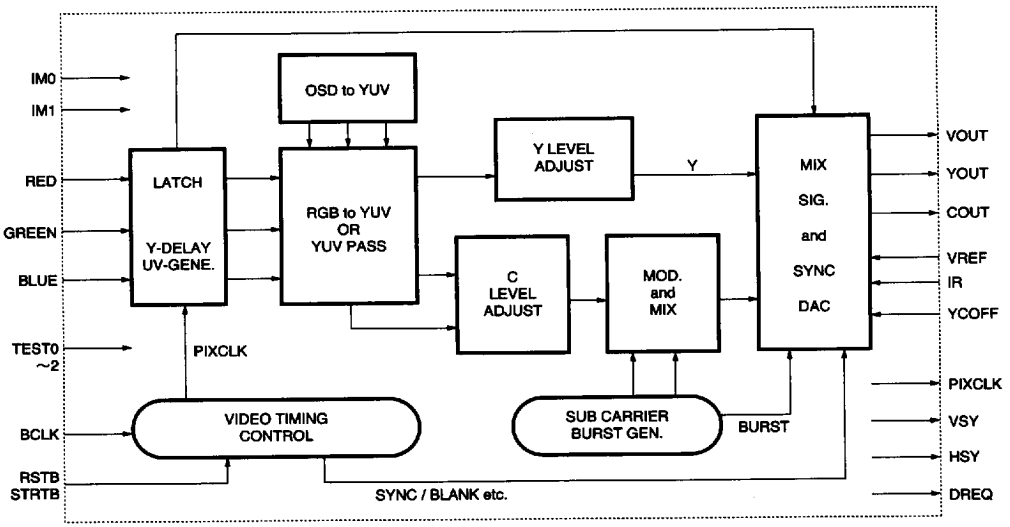
*1 Reduced by 11 mW for each increase in Ta of 1℃ over 25℃.
When mounted to a 70 × 70 × 1.6 mm glass epoxy board.
* Does not represent guaranteed performance.
◎ Not designed for radiation resistance.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}=AV_{DD}=DV_{DD}*	4.75~5.25	V
Input voltage, high level	V_{IH}	2.1~V_{DD}	V
Input voltage, low level	V_{IL}	0~0.8	V
Analog input voltage	VAIN	0~AV_{DD}	V
Operating temperature	Topr	−25~60	℃

* Use at V_{DD} = AV_{DD} = DV_{DD}

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	BOSD	PULLDOWN TO GND
2	GD0	GREEN DATA Bit0 (LSB)
3	GD1	GREEN DATA Bit1
4	GD2	GREEN DATA Bit2
5	GD3	GREEN DATA Bit3
6	GD4	GREEN DATA Bit4
7	GD5	GREEN DATA Bit5
8	GD6	GREEN DATA Bit6
9	GND	DIGITAL GROUND
10	GD7	GREEN DATA Bit7 (MSB)
11	BD0	BLUE DATA Bit0 (LSB)
12	BD1	BLUE DATA Bit1
13	BD2	BLUE DATA Bit2
14	BD3	BLUE DATA Bit3
15	OSDSW	NORMALLY OPEN
16	NC	—
17	BD4	BLUE DATA Bit4
18	BD5	BLUE DATA Bit5
19	BD6	BLUE DATA Bit6
20	BD7	BLUE DATA Bit7 (MSB)
21	GND	DIGITAL GROUND
22	DREQ	PULLDOWN TO GND
23	IM0	INPUT MODE SET Bit0
24	IM1	INPUT MODE SET Bit1
25	TEST1	NORMALLY PULLDOWN TO GND
26	TEST2	NORMALLY PULLDOWN TO GND
27	VSY	V - SYNC OUTPUT FOR MPEG
28	HSY	H - SYNC OUTPUT FOR MPEG
29	PIXCLK	BCLK THROUGH OUTPUT
30	STRTB	FUNCTION START ENABLE
31	VDD	DIGITAL VDD
32	NC	—
33	NC	—
34	NC	—
35	VREF	REFERENCE VOLTAGE (1.29V)
36	CGND	CHROMA OUTPUT GROUND
37	COUT	CHROMA OUTPUT
38	VGND	COMPOSITE OUTPUT GROUND
39	VOUT	COMPOSITE OUTPUT
40	AVSS	ANALOG (DAC,VREF) GROUND
41	NC	—
42	IR	REFERENCE RESISTOR (1.2k)
43	AVDD	ANALOG (DAC,REF) VDD
44	YGND	LUMINANCE OUTPUT GROUND
45	YOUT	LUMINANCE OUTPUT
46	NC	—
47	NC	—
48	YCOFF	DAC (YOUT,COUT) OFF
49	DVSS	DIGITAL (DAC_CTRL) GROUND
50	DVDD	DIGITAL (DAC_CTRL) VDD
51	BCLK	13.5MHz CLOCK INPUT
52	RSTB	LOGIC PART INITIAL RESET
53	TESUT0	NORMALLY PULLDOWN TO GND
54	RD0	RED DATA Bit0 (LSB)
55	RD1	RED DATA Bit1
56	RD2	RED DATA Bit2
57	ROSD	PULLDOWN TO GND
58	RD3	RED DATA Bit3
59	RD4	RED DATA Bit4
60	RD5	RED DATA Bit5
61	VDD	DIGITAL VDD
62	RD6	RED DATA Bit6
63	RD7	RED DATA Bit7
64	GOSD	PULLDOWN TO GND

●Electrical characteristics (unless otherwise noted, Ta=25℃, V_{DD}=AV_{DD} = DV_{DD}=5.0V, fBCLK=13.5MHz, load resistance=37.5Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock frequency	fBCLK	—	13.5	—	MHz	
Burst frequency	fBST	—	3.5795	—	MHz	Subcarrier frequency
Burst cycle	CBST	—	9	—	CYC	
Operating circuit current	IDD	—	120.0	—	mA	
Output voltage, high level	VOH	4.2	4.6	—	V	IOH=−2.0mA
Output voltage, low level	VOL	—	0.4	0.8	V	IOL=2.0mA
Input voltage, high level	VIH	2.4	—	—	V	
Input voltage, low level	VIL	—	—	0.8	V	
Input current 1, high level	IIH	—	1.0	10.0	μA	VIH=5.0V
Input current 1, low level	IIL	−10.0	0	—	μA	VIL=0.0V
DAC resolution	RES	—	9	—	BITS	
Differential linearity error	DNL	—	±1	—	LSB	Best straight line
Integral linearity error	INL	—	±3	—	LSB	Best straight line
Y white level current	IYW	—	25.14	—	mA	VREF=1.29V、IR=1.2kΩ
Y black level current	IYB	—	7.24	—	mA	VREF=1.29V、IR=1.2kΩ
Y zero level current	IYZ	−10.0	0.0	10.0	μA	

●Circuit operation

(1) General

The BU1414AK converts 8-bit digital RGB image signals to television signal output comprising a 9-bit composite signal, luminosity signal (Y) and color signal (C) in the NTSC format.

RGB signal input is synchronized to the 13.5MHz pixel clock (output of the PIXCLK pin), and can be converted to NTSC television signals with a maximum per-line (horizontal) resolution of 710 bits. Because the input synchronization signals — horizontal and vertical synchronization signals (outputs of pins HSY and VSY, respectively) — are generated internally, RGB data can be transferred according to TV encoder demands (i.e., synchronization signal) without the need for the complicated field sequence timing of NTSC. The format for digital data input is set with pins IM1 and IM0 (see Table 1 below). Moreover, digital RGB input can be output as analog GB signals in the through mode.

Table 1 : Setting the input format

IM1	IM0	Input format	Output signal
0	0	R (8 bits), G (8 bits), B (8 bits)	Television signals (9-bit resolution)
1	1	ROSD, GOSD and BOSD expanded to LSB for input RGB	RGB analog signal (9 bits)

Table 2 : Bit assignment in RGB through mode

Output pin	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VOUT	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	ROSD
YOUT	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	GOSD
COUT	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	BOSD

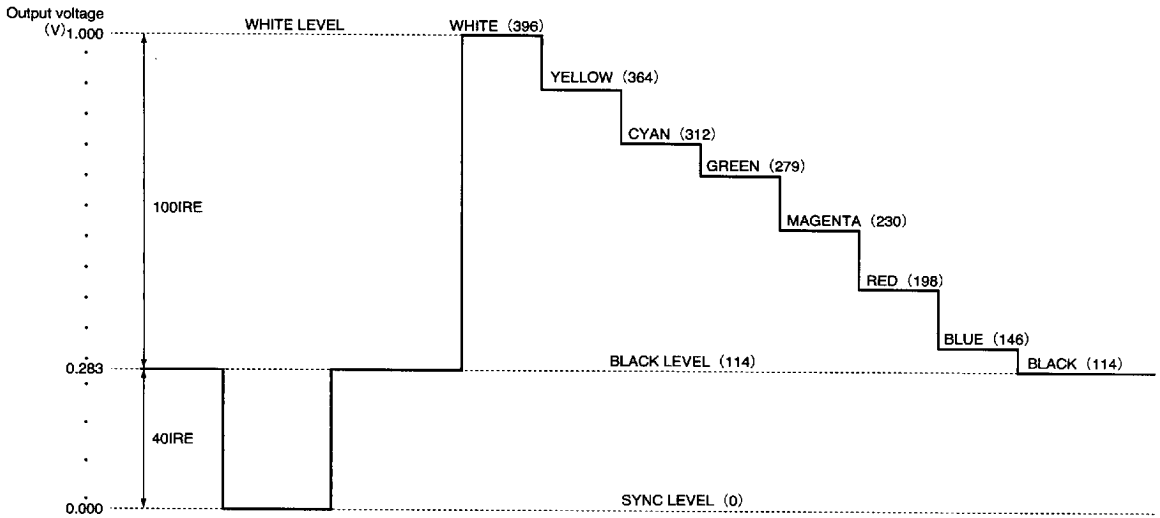
Input RGB signals are YUV-converted, while signals Y, U and V are adjusted to the 100IRE level when set to the NTSC format. U and V signals are phase-modulated by an internally ordered 3.58MHz subcarrier, generating modulated color signals.
Finally, the needed synchronization levels, color blank level and burst signals, etc., are mixed, and NTSC composite signals, luminance signals and color signals are output through the 9-bit DAC. The connections are as follows :

NTSC composite : VOUT
Luminance signal (Y) : YOUT
Color signal (C) : COUT

When also connecting the video input pin (75Ω), the output voltage range is $1.0V_{P\text{-}P}$.

(2) Output level

The figures below show pin output voltage level and the digital values of DAC output.



( ) Parentheses indicate the value of digital DAC output.
When VREF = 1.29 V, IR = 1.2 KΩ

Fig. 1 NTSC Y (luminosity) signal output level

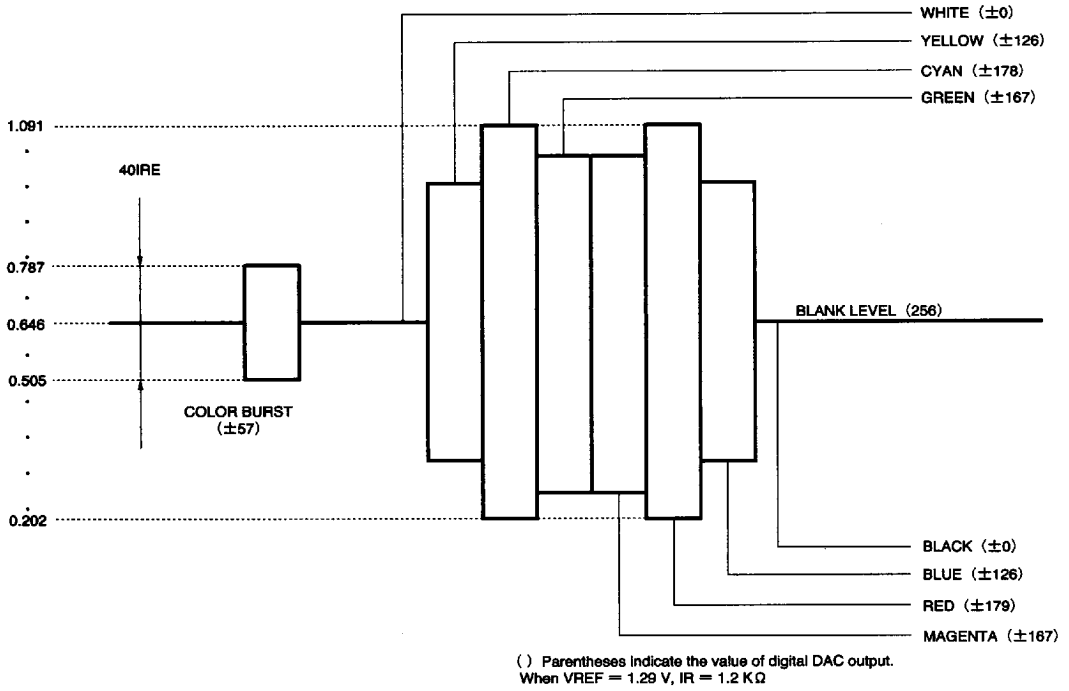
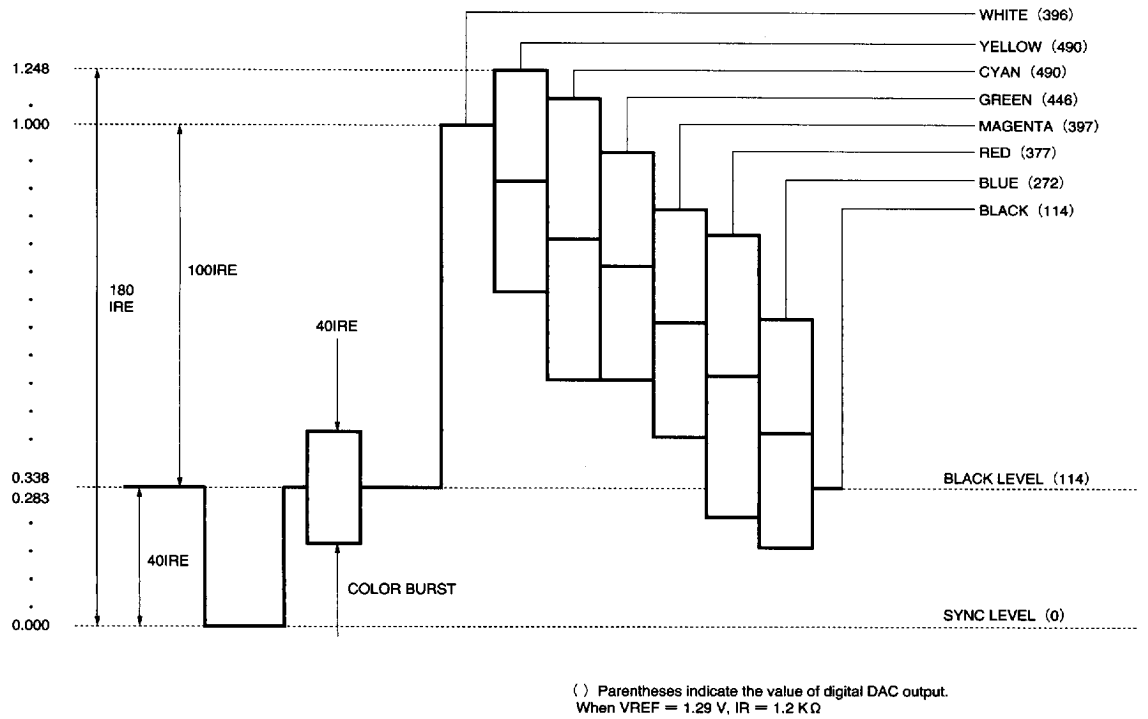


Fig. 2 NTSC C (chroma) signal output level



( ) Parentheses indicate the value of digital DAC output.
When VREF = 1.29 V, IR = 1.2 KΩ

Fig. 3 NTSC V (composite) signal output level

(3) Timing

The BU1414AK generates NTSC signal timing using a 13.5MHz clock signal (BCLK input pin) in accordance with the termination of the reset signal. The timing chart below shows the input and output of timing pins.

Table 3 : Timing input/output (BU1414AK)

Pin No	Pin	Pin Name	Input/output	Function
1	51	BCLK	Input	13.5 MHz clock input
2	52	RSTB	Input	Reset input
3	30	STRTB	Input	Function start timing input
4	29	PIXCLK	Output	Pixel clock output (13.5 MHz)
5	27	VSY	Output	Vertical synchronization signal
6	25	HSY	Output	Horizontal synchronization signal

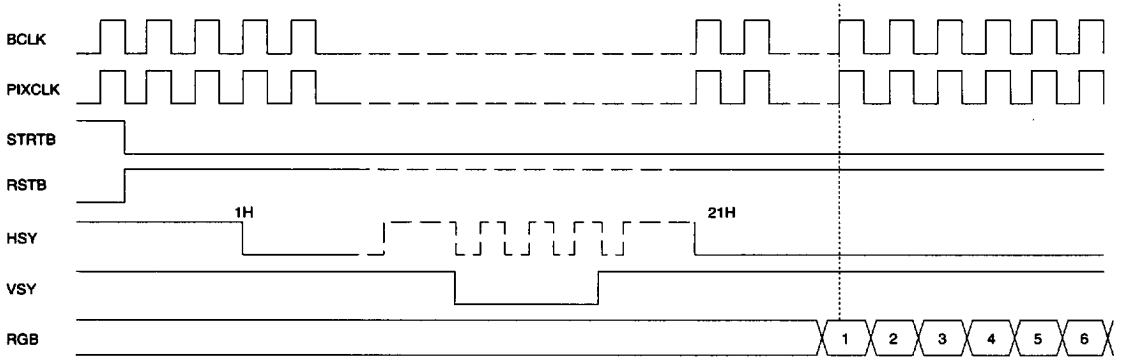


Fig. 4 BU1414AK Control timing 1

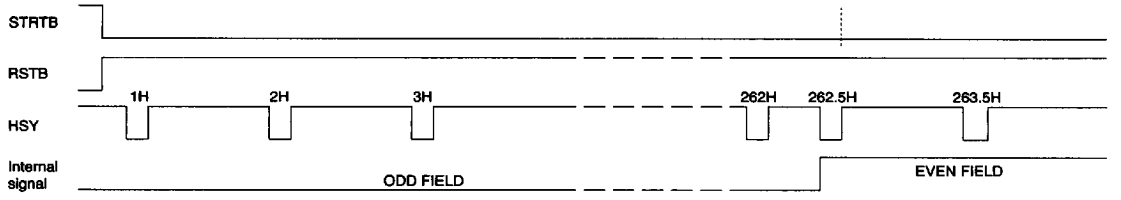


Fig.5 BU1414AK Control timing 2

* Connect STRTB to GND when using the BU1414AK as a timing master.

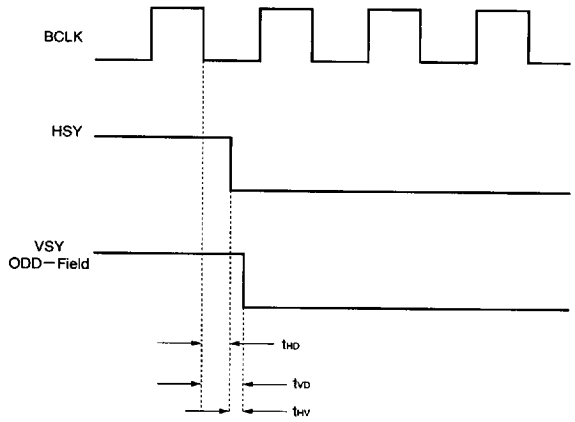


Fig. 6 Timing of synchronization signal output

Table 4

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
HYS output delay	t_{HD}	—	30.0	—	nS	
VSY output delay	t_{VD}	—	30.0	—	nS	
HSY-VSY timing offset	Δt_{HV}	−20	0.0	20	nS	

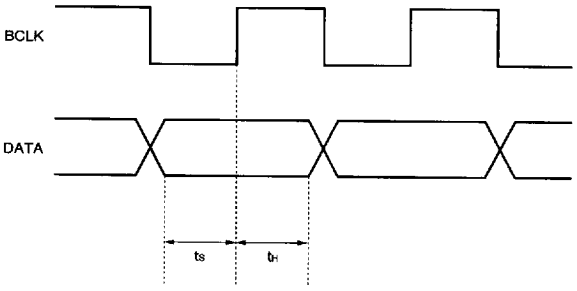


Fig. 7 Clock and signal input timing

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Setup time	ts	—	—	34.0	nS	
Hold time	t_H	—	—	34.0	nS	

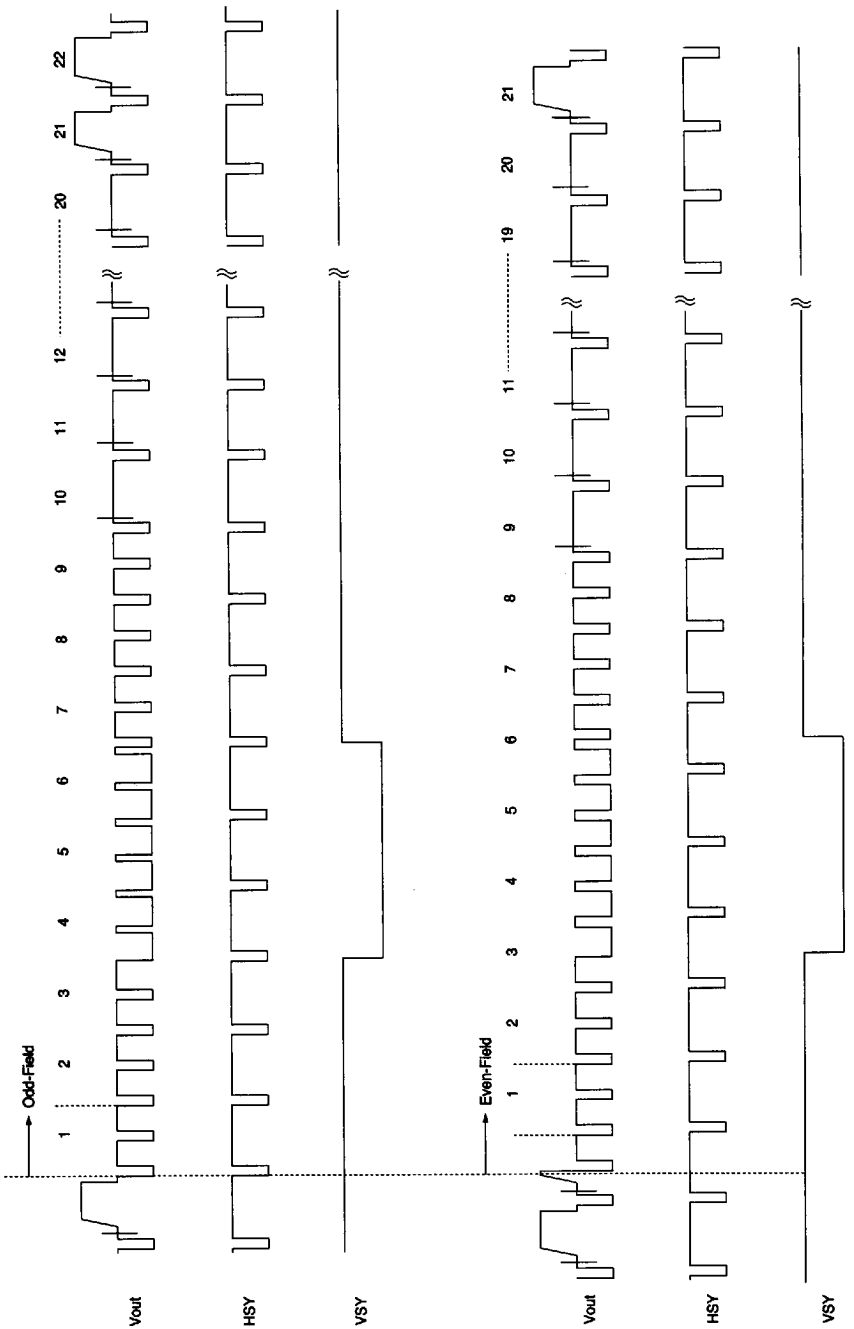


Fig. 8 Frame timing

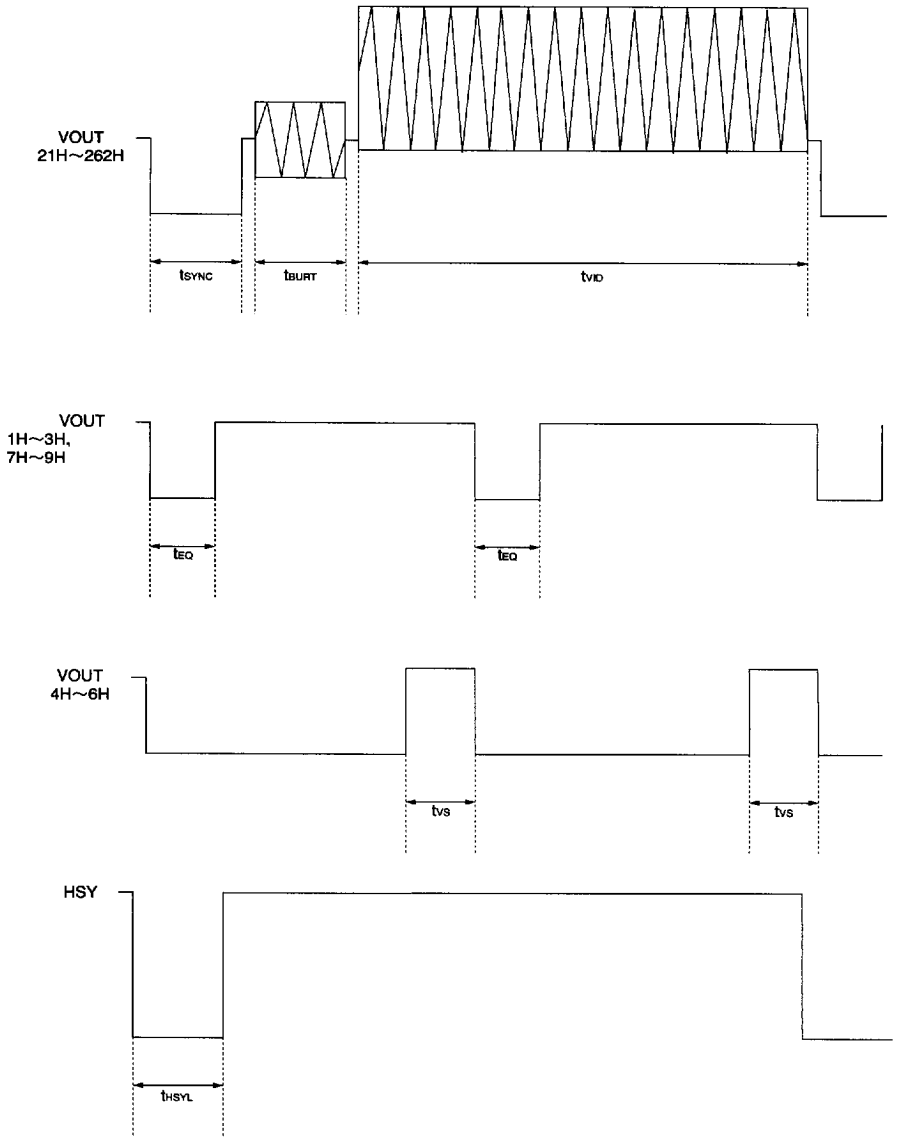


Fig. 9 Data timing during 1H

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
HSYNC width	t_{SYNC}	—	64	—	tCLK	tCLK=1/13.5MHz
Burst duration	t_{BURT}	—	35	—	tCLK	〃
Video output duration	t_{VID}	—	711	—	tCLK	〃
Equivalent pulse width	t_{EQ}	—	31	—	tCLK	〃
Vertical synch pulse width	t_{VS}	—	64	—	tCLK	〃
HSY L duration	t_{HSYL}	—	64	—	tCLK	〃

(4) Low power consumption mode
The BU1414AK can be set to either the normal mode or the low power consumption mode.

Table 7

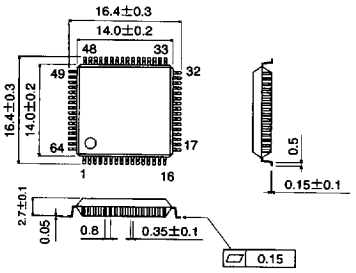
Pin No.	Pin name	Output mode and power consumption			
	YCOFF	VOUT	YOUT	COUT	Power consumption
48	L	Composite signal	Luminance signal	Color signal	0.65W
	H	Composite signal	No output (0 V)	No output (0 V)	0.35W

(5) The DAC output level is determined by the internal DAC output current and the attached DAC output resistor. The output current of each DAC bit is determined by the VREF pin (pin 35) voltage and by the resistor attached to the IR pin (pin 42) (see below).
I (1LSB) = VVREF/(RIR+R0) ∗1/16 (equation 1)

VVREF : voltage opplied on VREF [V]
RIR : resistor attached to IR [Ω]
R0 : Internal parasitic resistance of IC [Ω]

Thus, when VVREF = 1.29V and RIR = 1.2kΩ, the current output for each LSB is 63.48 μA. The white level of Y has a digital value of 396 (decimal) and therefore is calculated as follows :
V (Y white) = 0.06348 ∗ 396 = 25.14 [mA]
If a 37.5Ω resistor is attached to DAC output, amplitude is 0.943 [V_{P-P}].
The DAC output level can be fine-tuned according to equation 1 above. Please contact ROHM when using constants that differ significantly from those above (i.e., output level = 1 V_{P-P}, VVREF = 1.29V, RIR = 1.2kΩ, attached DAC output resistor = 37.5Ω).

●External dimensions (Units: mm)



QFP - A64