ZETEX SEMICONDUCTORS

P-channel enhancement mode vertical DMOS FET

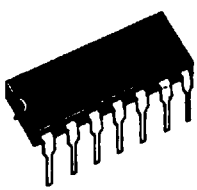
ZVP2110

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

E-LINE (TO-92)
SUFFIX A or C

TO-39
SUFFIX B



14 LEAD MOULDED DIL
SUFFIX E

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2110A*	−100V	−0.23A	8Ω
ZVP2110B*	−100V	−0.60A	8Ω
ZVP2110C	−100V	−0.23A	8Ω
ZVP2110E	−100V	−0.23A	8Ω

*BS-CECC approved

ZVP2110

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	DIL	Units
V_{DS}	Drain-source voltage	−100	−100	−100	V
I_D	Continuous drain current (@ T_A = 25°C)	−0.23	−0.23	−0.23	A
I_D	Continuous drain current (@ T_C = 25°C)	–	−0.60	–	A
I_{DM}	Pulsed drain current	−3	−3	−3	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ T_A = 25°C)	0.7	0.7	0.85	W
P_D	Max. power dissipation (@ T_C = 25°C)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−100	–	V	I_D = −1mA, V_{GS} = 0V
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	I_D = −1mA, V_{DS} = V_{GS}
I_{GSS}	Gate body leakage	–	20	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	–	−1	μA	V_{DS} = Max. rating, V_{GS} = 0V
		–	−100	μA	V_{DS} = 0.8 × Max. rating, V_{GS} = 0V (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−750	–	mA	V_{DS} = −25V, V_{GS} = −10V
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	8	Ω	I_D = −375mA, V_{GS} = −10V
g_{fs}	Forward transconductance (1) (2)	125	–	mS	V_{DS} = −25V, I_D = −375mA
C_{iss}	Input capacitance (2)	–	100	pF	V_{DS} = −25V, V_{GS} = 0V, f = 1MHz
C_{oss}	Common source output capacitance (2)	–	35	pF	
C_{rss}	Reverse transfer capacitance (2)	–	10	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	V_{DD} ≈ −25V, I_D = −375mA
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

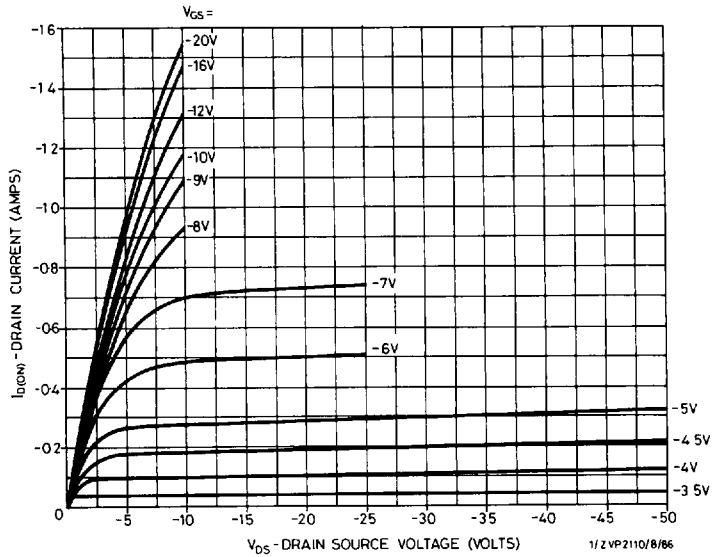


Fig. 1 Typical output characteristics

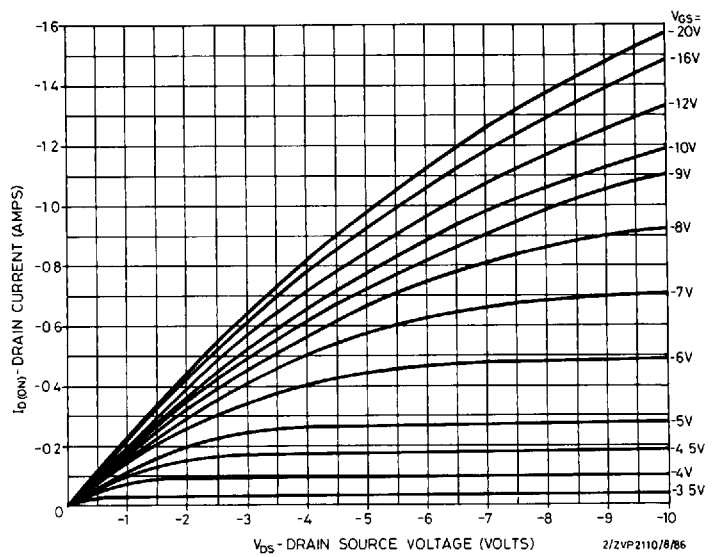


Fig. 2 Typical saturation characteristics

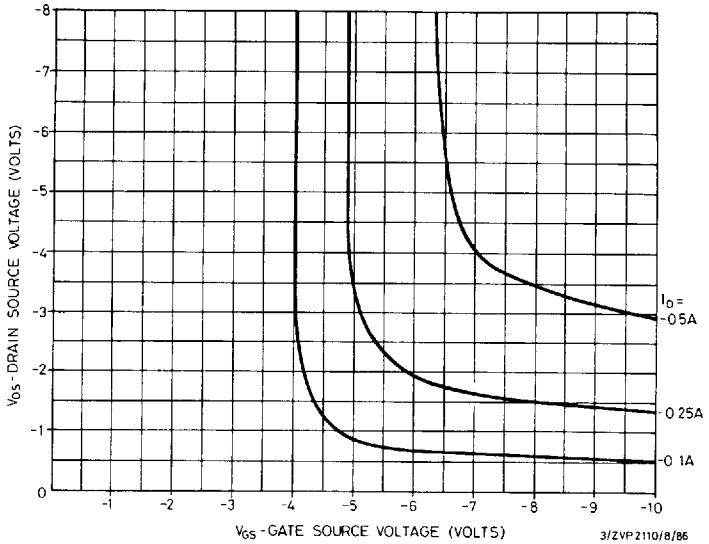


Fig. 3 Typical voltage saturation characteristics

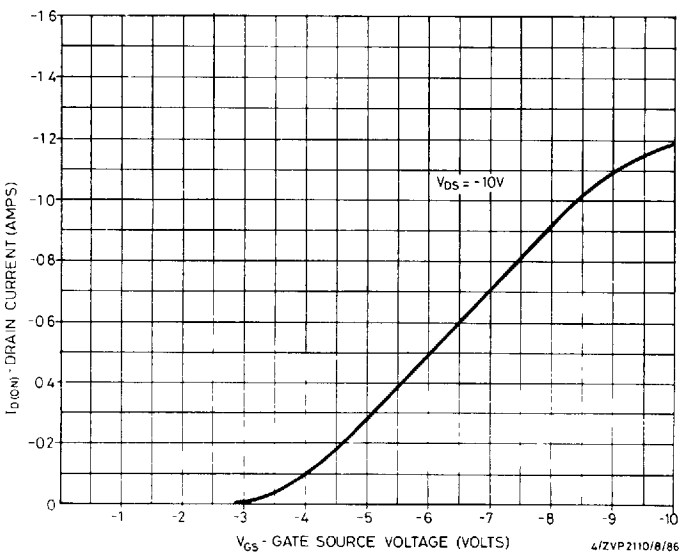


Fig. 4 Typical transfer characteristics

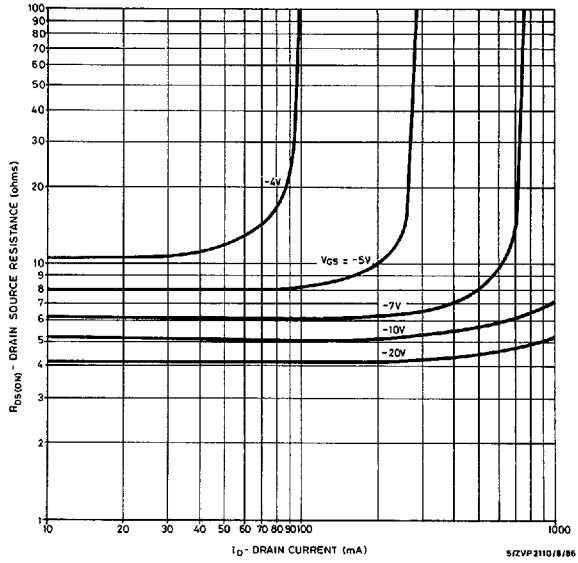


Fig. 5 Typical on-resistance v drain current

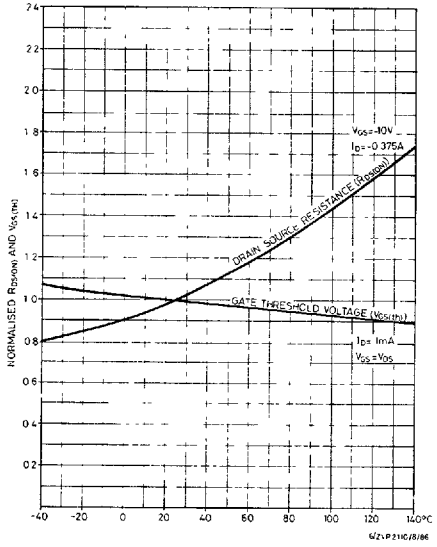


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

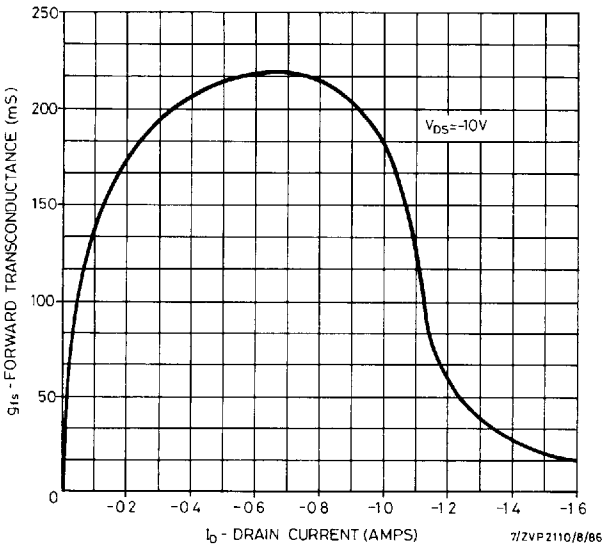


Fig. 7 Typical transconductance v drain current

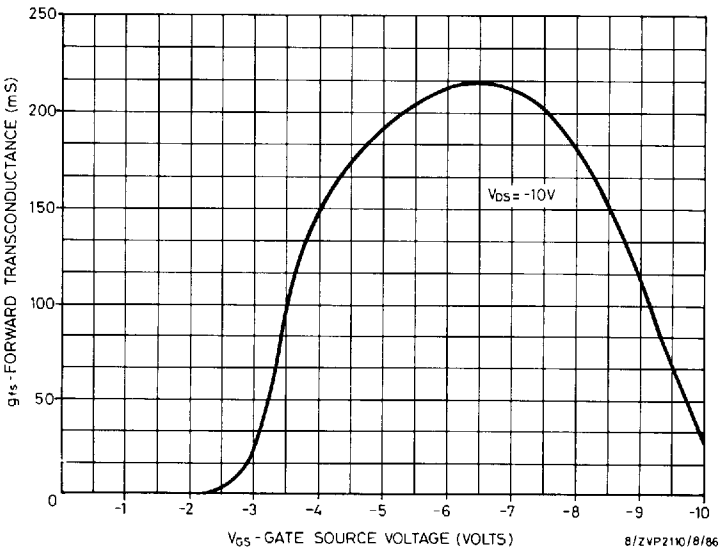


Fig. 8 Typical transconductance v gate-source voltage

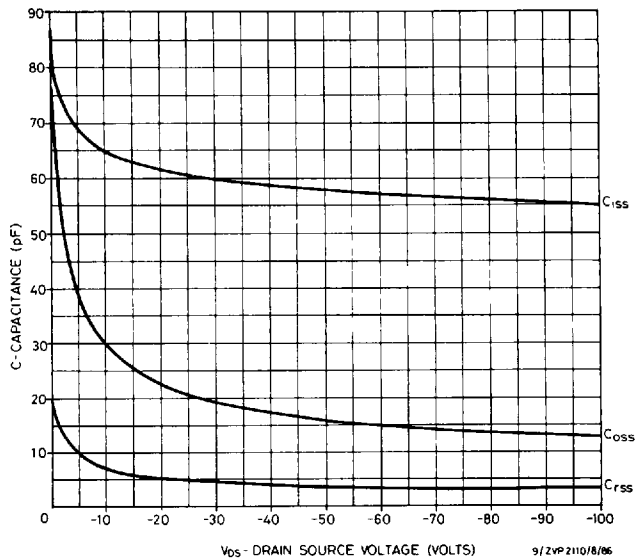


Fig. 9 Typical capacitance v drain-source voltage

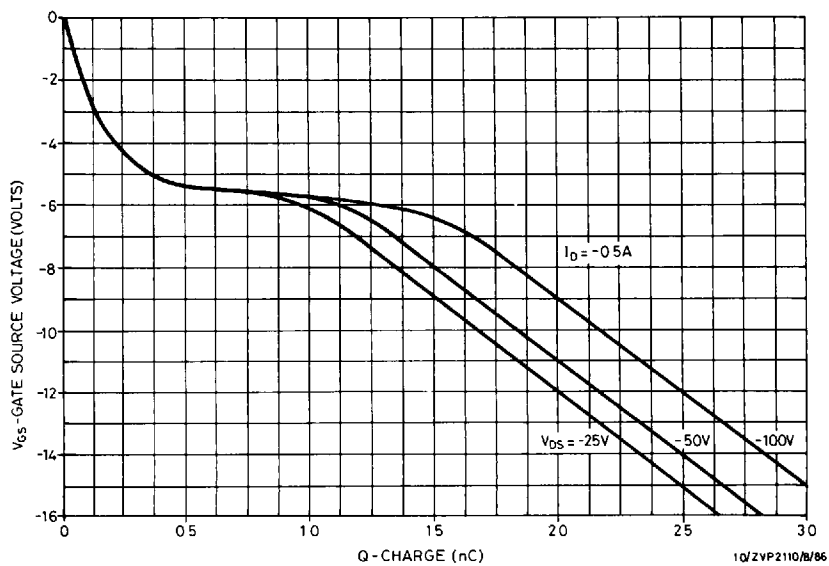


Fig. 10 Typical gate charge v gate-source voltage

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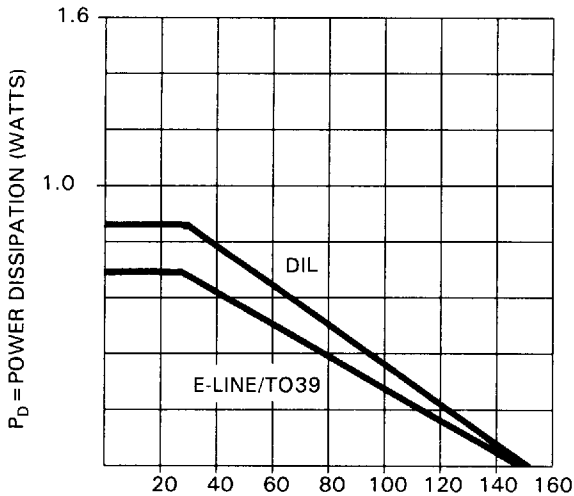

Fig. 11 Power v temperature derating curve (ambient)

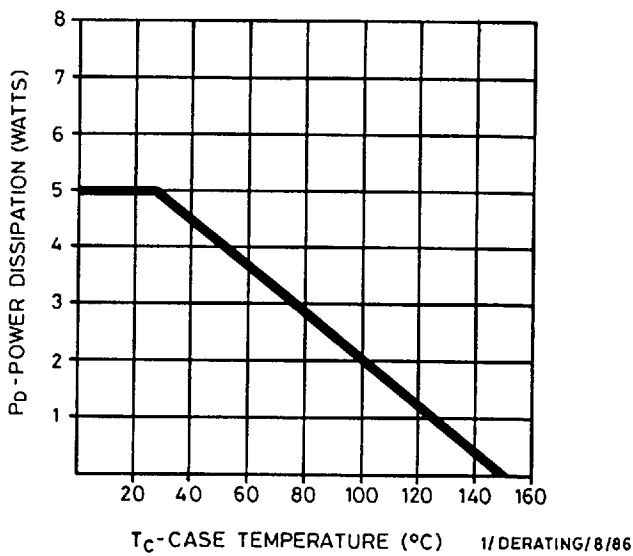

Fig. 12 Power v temperature derating curve (case)