

CMOS 8-BIT MICROCONTROLLERS

TMP91P640N / TMP91P640F

1. OUTLINE AND CHARACTERISTICS

The TMP91P640 is a system evaluation LSI having a built in One-Time PROM for TMP91C640.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP91C640 or TMP90C840A by programming to the internal PROM.

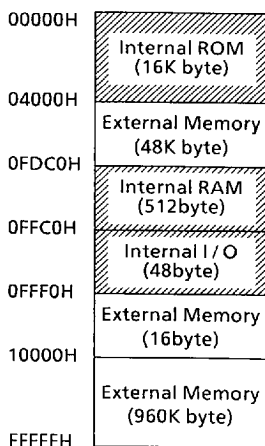
The different points between TMP91P640 and TMP90C840A are the memory size (ROM/RAM) and maximum operating frequency.

The operating frequency range of TMP91P640 is from 1MHz to 12.5MHz.

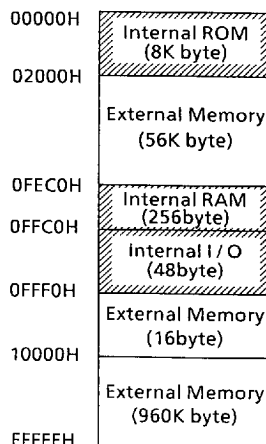
The TMP91P640N is in a Shrink Dual Inline Package (SDIP64-P-750).

The TMP91P640F is in a Quad Flat Package (QFP64-P-1420A).

The following are the memory map of TMP91C640 and TMP90C840A.



TMP91C640 Memory Map



TMP90C840A Memory Map

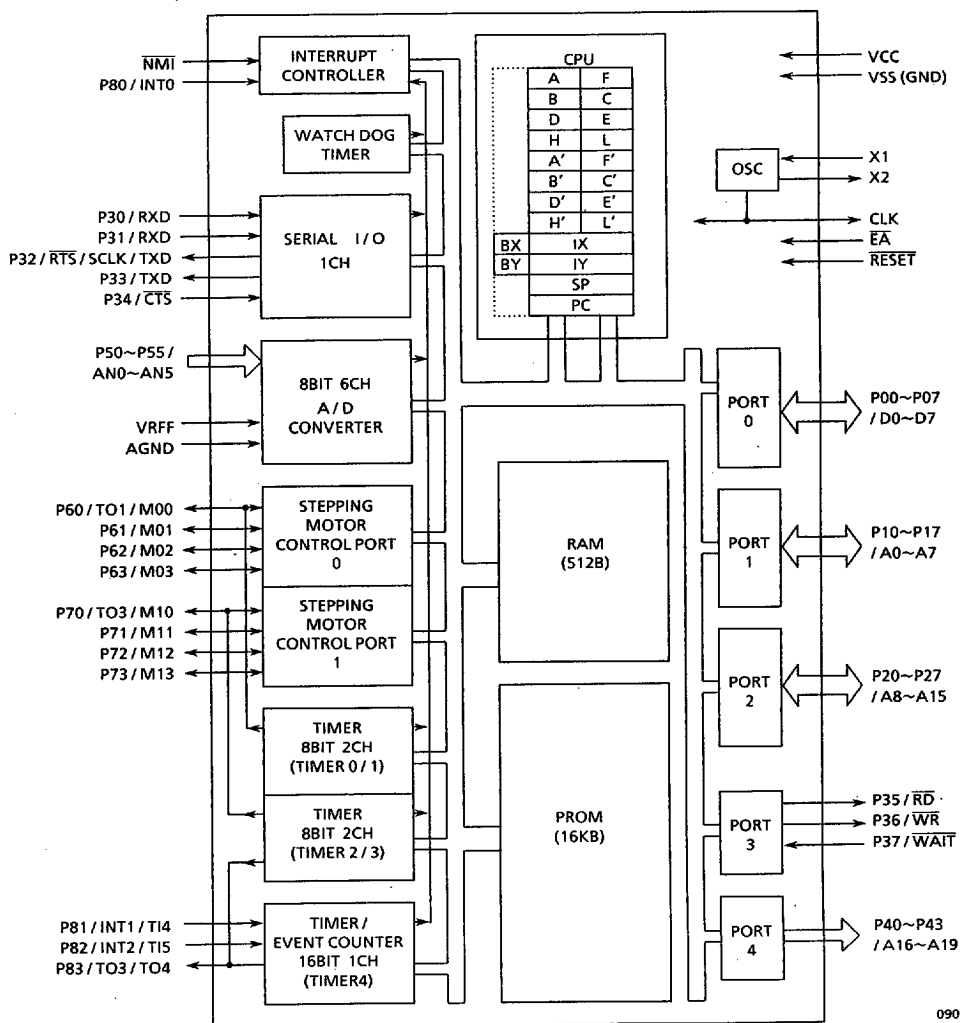
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PARTS NO.	ROM	RAM	PACKAGE	ADAPTER SOCKET NO.
TMP91P640N	OTP 16384 × 8bit	512 × 8bit	64-SDIP	8M1115A
TMP91P640F			64-FP	8M1116A

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Figure 1 TMP91P640 Block Diagram

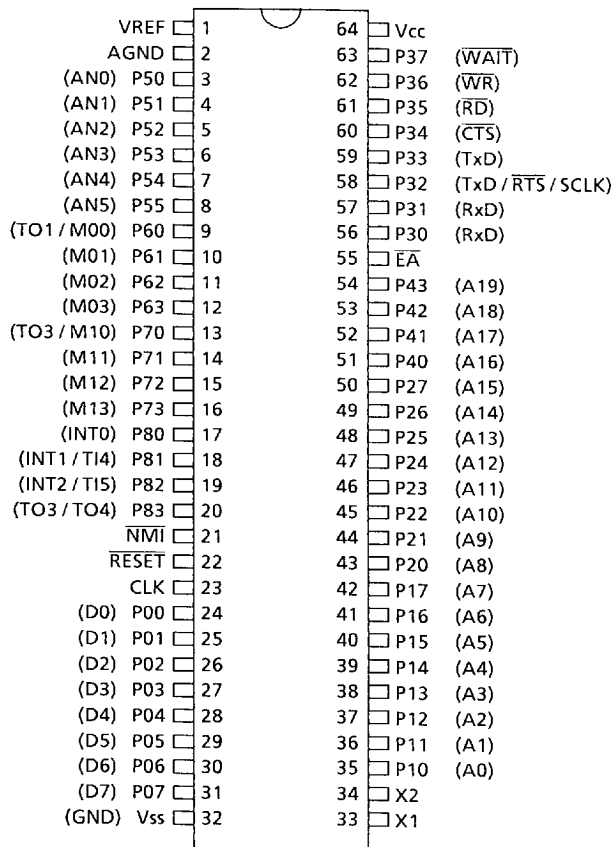
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2. PIN ASSIGNMENT AND FUNCTIONS

2.1 Pin Assignment

Figure 2.1 (1) shows pin assignment of the TMP91P640N.



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Figure 2.1 (1) Pin Assignment (64-SDIC / SDIP)

The diagram shows the ATmega16 microcontroller with its 40 pins. The pins are numbered 1 to 40. The functions for each pin are listed on the left and right sides of the chip. The internal connections are shown as lines connecting the pins to the internal logic blocks.

Pin Functions:

- Pin 1: (AN0) P50
- Pin 2: (AN1) P51
- Pin 3: (AN2) P52
- Pin 4: (AN3) P53
- Pin 5: AGND
- Pin 6: VREF
- Pin 7: Vcc
- Pin 8: (WAIT) P37
- Pin 9: (WR) P36
- Pin 10: (RD) P35
- Pin 11: (CTS) P34
- Pin 12: (TXD) P33
- Pin 13: (TXD/RTS/SCLK) P32
- Pin 14: P14 (A4)
- Pin 15: P15 (A5)
- Pin 16: P16 (A6)
- Pin 17: P17 (A7)
- Pin 18: P20 (A8)
- Pin 19: P21 (A9)
- Pin 20: P22 (A10)
- Pin 21: P23 (A11)
- Pin 22: P24 (A12)
- Pin 23: P25 (A13)
- Pin 24: P26 (A14)
- Pin 25: P27 (A15)
- Pin 26: P40 (A16)
- Pin 27: P41 (A17)
- Pin 28: P42 (A18)
- Pin 29: P43 (A19)
- Pin 30: P30 (RXD)
- Pin 31: P31 (RXD)
- Pin 32: X1
- Pin 33: Vss (GND)
- Pin 34: P06 (D6)
- Pin 35: P05 (D5)
- Pin 36: P04 (D4)
- Pin 37: P03 (D3)
- Pin 38: P02 (D2)
- Pin 39: P07 (D7)
- Pin 40: X2

Internal Connections:

- Pin 14 (P14) is connected to the internal logic block.
- Pin 15 (P15) is connected to the internal logic block.
- Pin 16 (P16) is connected to the internal logic block.
- Pin 17 (P17) is connected to the internal logic block.
- Pin 18 (P20) is connected to the internal logic block.
- Pin 19 (P21) is connected to the internal logic block.
- Pin 20 (P22) is connected to the internal logic block.
- Pin 21 (P23) is connected to the internal logic block.
- Pin 22 (P24) is connected to the internal logic block.
- Pin 23 (P25) is connected to the internal logic block.
- Pin 24 (P26) is connected to the internal logic block.
- Pin 25 (P27) is connected to the internal logic block.
- Pin 26 (P40) is connected to the internal logic block.
- Pin 27 (P41) is connected to the internal logic block.
- Pin 28 (P42) is connected to the internal logic block.
- Pin 29 (P43) is connected to the internal logic block.
- Pin 30 (P30) is connected to the internal logic block.
- Pin 31 (P31) is connected to the internal logic block.
- Pin 32 (X1) is connected to the internal logic block.
- Pin 33 (Vss) is connected to the internal logic block.
- Pin 34 (P06) is connected to the internal logic block.
- Pin 35 (P05) is connected to the internal logic block.
- Pin 36 (P04) is connected to the internal logic block.
- Pin 37 (P03) is connected to the internal logic block.
- Pin 38 (P02) is connected to the internal logic block.
- Pin 39 (P07) is connected to the internal logic block.
- Pin 40 (X2) is connected to the internal logic block.

Figure 2.1 (2) Pin Assignment (64-FP)

2.2 Pin Names and Functions

The TMP91P640 has MCU mode and PROM mode.

(1) MCU Mode (The TMP91C640 and the TMP91P640 are pin compatible)

Pin Names and Functions (1/2)

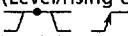
Pin Name	No. of pins	I/O 3 states	Function
P00~P07 /D0~D7	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
		3 states	Data bus: Also functions as 8-bit bidirectional data bus for external memory
P10~P17 /A0~A7	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
		Output	Address bus: The lower 8 bits address bus for external memory
P20~P27 /A8~A15	8	I/O	Port 2: 8-bit I/O port that allows selection on bit basis
		Output	Address bus: The upper 8 bits address bus for external memory
P30 /RxD	1	Input	Port 30: 1-bit input port
			Receiver Serial Data
P31 /RxD	1	Input	Port 31: 1-bit input port
			Receiver Serial Data
P32 /TxD /RTS /SCLK	1	Output	Port 32: 1-bit output port
			Transmitter serial Data
			Request to send serial data
			Serial clock output
P33 /TxD	1	Output	Port 33: 1-bit output port
			Transmitter Serial Data
P34 /CTS	1	Input	Port 34: 1-bit input port
			Clear to send Serial data
P35 /RD	1	Output	Port 35: 1-bit output port
			Read: Generates strobe signal for reading external memory
P36 /WR	1	Output	Port 36: 1-bit output port
			Write: Generates strobe signal for writing into external memory
P37 /WAIT	1	Input	Port 37: 1-bit input port
			Wait: Input pin for connecting slow speed memory or peripheral LSI
P40~P43 /A16~A19	4	Output	Port 4: 4-bit output port that allows selection of Port/Address Bus on bit basis
			Address bus: Also functions as address bus for external memory (4 bits of bank address)
P50~P55 /AN0~AN5	6	Input	Port 5: 6-bit input port
			Analog input: 6 analog inputs to A/D converter

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Pin Names and Functions (2/2)

Pin Name	No. of pins	I/O 3 states	Function
VREF	1		Input of reference voltage to A/D converter
AGND	1		Ground pin for A/D converter
P60~P63 /M00~M03 /TO1	4	I/O Output Output	Port 6: 4-bit I/O port that allows I/O selection on bit basis Stepping motor control port 0 Timer output 1: Output of Timer 0 or 1
P70~P73 /M10~M13 /TO3	4	I/O Output Output	Port 7: 4-bit I/O port that allows I/O selection on bit basis Stepping motor control port 1 Timer output 3: Output of Timer 2 or 3
P80 /INT0	1	Input	Port 80: 1-bit input port Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable) 
P81 /INT1 /TI4	1	Input	Port 81: 1-bit input port Interrupt request pin 1: interrupt request pin (Rising/falling edge is programmable)  Timer input 4: Counter/capture trigger signal for Timer 4
P82 /INT2 /TI5	1	Input	Port 82: 1-bit input port Interrupt request pin 2: rising edge interrupt request pin Timer input 5: capture trigger signal for Timer 4
P83 /TO3/TO4	1	Output	Port 83: 1-bit output port Timer output 3/4: Output of Timer 2, 3 or 4
NMI	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin 
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
EA	1	Input	External access: Connects with Vcc pin using internal PROM, and with GND pin not using internal PROM.
RESET	1	Input	Reset : Initializes the LSI. (Built in pull-up resistor)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator
Vcc	1		Power supply (+ 5V)
Vss (GND)	1		Ground (0V)

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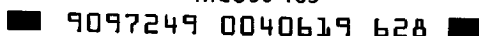
(2) PROM Mode

Table 2.1

Pin Function Name	No. of pins	I/O	Function	Pin Name (MCU mode)
A7~A0	8	Input	Address Input	P17~P10
A13~A8	6	Input		P25~P20
A14	2	Input	Be fixed to "L" level.	P26
A15				P27
D7~D0	8	I/O	Data Input/Output	P07~P00
$\overline{OE}$	1	Input	Output Enable Input	P35
$\overline{CE}$	1	Input	Chip Enable Input	P36
VPP	1	Power Supply	12.5V / 5V (Programming Power Supply)	$\overline{EA}$
VCC	1	Power Supply	5V	VCC
VSS	1	Power Supply	0V	VSS
Pin Name	No. of pins	I/O	Pin Setting	
P30, P31	2	Input	Be fixed to "L" level.	
P32, P33	2	Output	Open	
P34, P37	2	Input	Be fixed to "L" level.	
P43~P40	4	Output	Open	
P55~P50	6	Input	Be fixed to "L" level.	
P63~P60	4			
P73~P70	4			
P82~P80	3			
P83	1	Output	Open	
VREF	1		Be fixed to "L" level.	
AGND	1		Be fixed to "L" level.	
RESET	1	Input	Be fixed to "L" level.	
CLK	1	Input	Be fixed to "L" level.	
NMI	1	Input	Be fixed to "H" level.	
X1	1	Input	Resonator connection pin	
X2	1	Output		

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3. OPERATION

The TMP91P640 is the OTP version of the TMP91C640 that is replaced an internal ROM from Mask ROM to One-Time PROM.

The function of TMP91P640 is exactly same as that of TMP90C840A except the internal ROM/RAM size.

Refer to the TMP90C840A except the functions which are not described this section.

The following is an explanation of the hardware configuration and operation in relation to the TMP91P640.

The TMP91P640 has an MCU mode and a PROM mode.

3.1 MCU Mode

(1) Mode Setting and Function

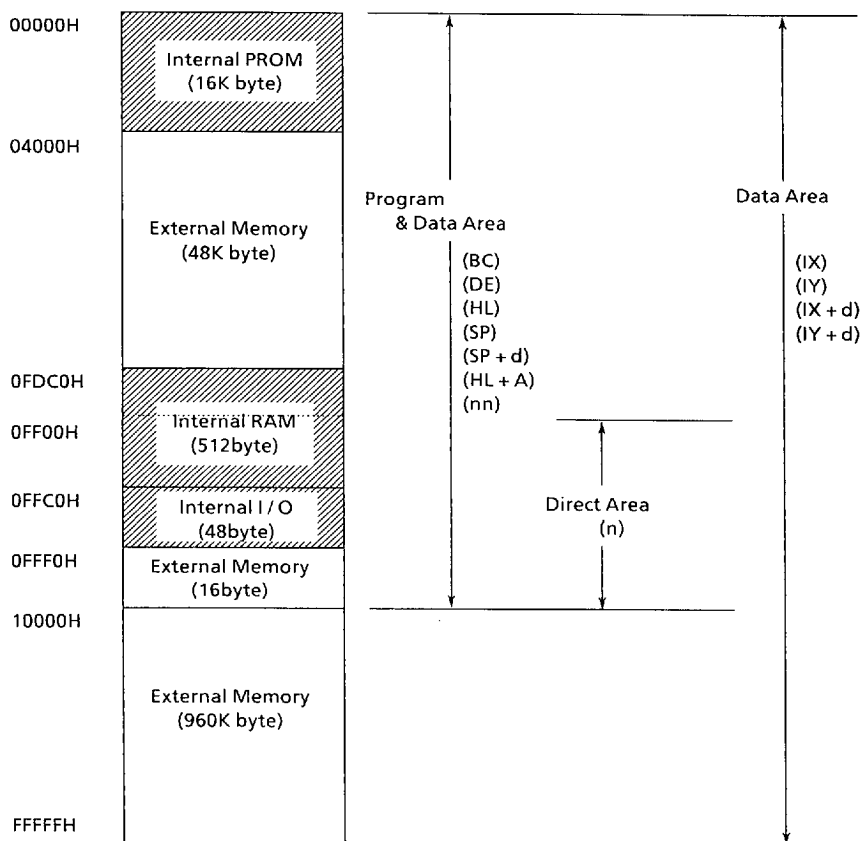
The MCU mode is set by opening the CLK pin (Output status).

In the MCU mode, the operation is same as that of TMP91C640.

(2) Memory Map

The memory map is same as that of TMP91C640.

Figure 3.1 shows the memory map of TMP91P640, and the accessing area by the respective addressing mode.



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Figure 3.1 TMP91P640 Memory Map

3.2 PROM Mode

(1) Mode Setting and Function

PROM mode is set by setting the **RESET** and **CLK** pins to the "L" level.

The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket. The device selection (ROM Type) should be "27256" with following conditions.

size : 256Kbit (32K×8bit) VPP : 12.5V TPW: 1ms

The TMP91P640 is not supported an electric signature mode.

Figure 3.2 shows the setting of pins in PROM mode.

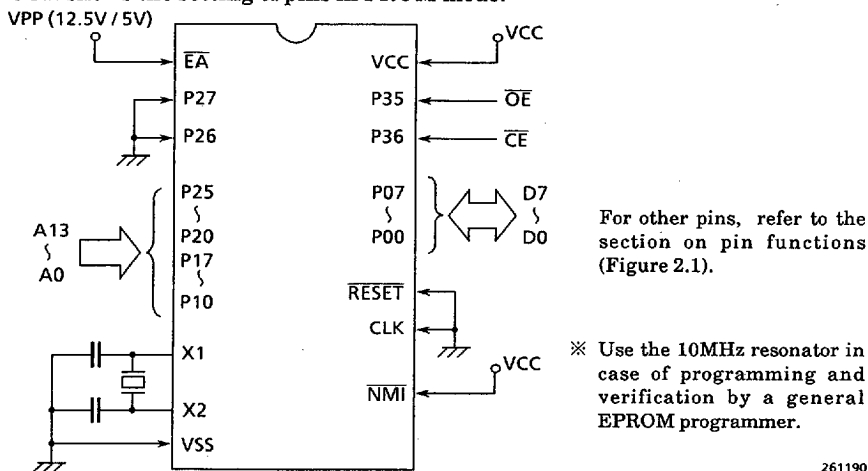


Figure 3.2 PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.5V (programming voltage) to the VPP pin when the following pins are set as follows,

(Vcc : 6.0V
RESET : "L" level
CLK : "L" level)

* These conditions can be obtained by using adaptor socket.

After the address and data have been fixed, a data on the Data Bus is programmed when the **CE** pin is set to "Low" (1ms plus is required).

General programming procedure of an EPROM programmer is as follows,

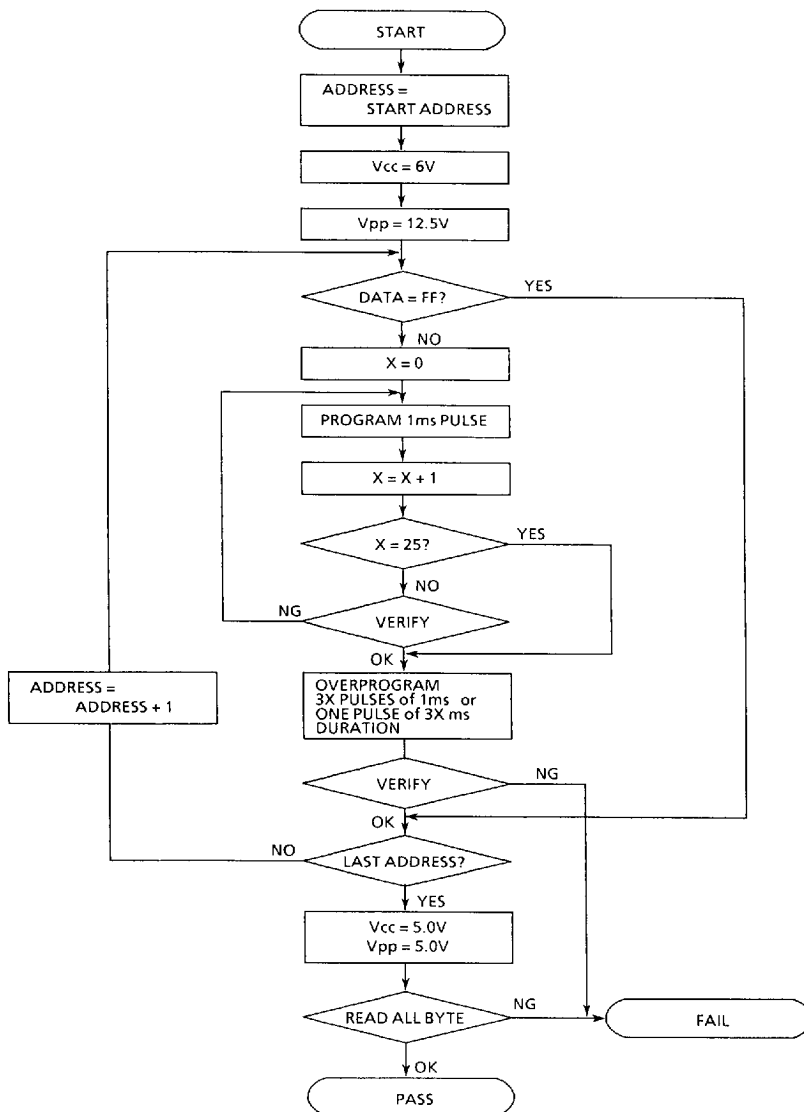
- Write a data to a specified address for 1ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writing is performed by using three times longer programming pulse width (1ms×programming times), or using three times

more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of $V_{pp}=V_{cc}=5V$ after all data were written.

Figure 3.3 shows the programming flow chart.



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Figure 3.3 Flow Chart

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4. ELECTRICAL CHARACTERISTICS

TMP91P640N/TMP91P640F

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V _{CC}	Supply voltage	-0.5 ~ +6.5	V
V _{IN}	Input voltage	-0.5 ~ V _{CC} + 0.5	V
P _D	Power dissipation (T _a = 85°C)	F 500 N 600	mW
T _{SOLDER}	Soldering temperature (10 s)	260	°C
T _{STG}	Storage temperature	-65 ~ 150	°C
T _{OPR}	Operating temperature	-40 ~ 85	°C

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4.2 DC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)Typical Values are for TA = 25°C and V_{CC} = 5V.

Symbol	Parameter	Min	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage (P0)	-0.3	0.2V _{CC} - 0.1	V	
V _{IL1}	P1, P2, P3, P4, P5, P6, P7, P8	-0.3	0.3V _{CC}	V	
V _{IL2}	RESET, INTO (P80), NMI	-0.3	0.25V _{CC}	V	
V _{IL3}	EA	-0.3	0.3	V	
V _{IL4}	X1	-0.3	0.2V _{CC}	V	
V _{IH}	Input High Voltage (P0)	0.2V _{CC} + 1.1	V _{CC} + 0.3	V	
V _{IH1}	P1, P2, P3, P4, P5, P6, P7, P8	0.7V _{CC}	V _{CC} + 0.3	V	
V _{IH2}	RESET, INTO (P80), NMI	0.75V _{CC}	V _{CC} + 0.3	V	
V _{IH3}	EA	V _{CC} - 0.3	V _{CC} + 0.3	V	
V _{IH4}	X1	0.8V _{CC}	V _{CC} + 0.3	V	
V _{OL}	Output Low Voltage		0.45	V	I _{OL} = 1.6mA
V _{OH} V _{OH1} V _{OH2}	Output High Voltage	2.4 0.75V _{CC} 0.9V _{CC}		V V V	I _{OH} = -400μA I _{OH} = -100μA I _{OH} = -20μA
I _{DAR}	Darlington Drive Current (8 I/O pins)	-1.0	-3.5	mA	V _{EXT} = 1.5V R _{EXT} = 1.1 kΩ
I _{LI}	Input Leakage Current	0.02 (Typ)	± 5	μA	0.0 ≤ V _{IN} ≤ V _{CC}
I _{LO}	Output Leakage Current	0.05 (Typ)	± 10	μA	0.2 ≤ V _{IN} ≤ V _{CC} - 0.2
I _{CC}	Operating Current (RUN) Idle 1 Idle 2	20 (Typ) 1.5 (Typ) 9 (Typ)	40 5 15	mA mA mA	f _{osc} = 10MHz
	STOP (TA = -40 ~ 85°C) STOP (TA = 0 ~ 50°C)	0.2 (Typ)	50 10	μA μA	0.2 ≤ V _{IN} ≤ V _{CC} - 0.2
V _{STOP}	Power Down Voltage (@STOP) RAM BACK UP	2	6	V	V _{IL2} = 0.2V _{CC} , V _{IH2} = 0.8V _{CC}
R _{RST}	RESET Pull Up Resistor	50	150	kΩ	
C _{IO}	Pin Capacitance		10	pF	testfreq = 1MHz
V _{TH}	Schmitt width RESET, NMI, INTO	0.4	1.0(Typ)	V	

Note : I_{DAR} is guaranteed for a total of up to 8 optional ports.

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4.3 AC Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = -40 \sim 85^\circ C$ (1~10MHz)
 $CL = 50pF$ $T_A = -20 \sim 70^\circ C$ (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	OSC. Period = x	80	1000	100		80		ns
t_{CYC}	CLK Period	4x	4x	400		320		ns
t_{WL}	CLK Low width	2x - 40		160		120		ns
t_{WH}	CLK High width	2x - 40		160		120		ns
t_{AC}	Address Setup to $\overline{RD}$, $\overline{WR}$	x - 45		55		35		ns
t_{RR}	$\overline{RD}$ Low width	2.5x - 40		210		160		ns
t_{CA}	Address Hold Time After $\overline{RD}$, $\overline{WR}$	0.5x - 40		10		0		ns
t_{AD}	Address to Valid Data In		3.5x - 95		255		185	ns
t_{RD}	$\overline{RD}$ to Valid Data In		2.5x - 80		170		120	ns
t_{HR}	Input Data Hold After $\overline{RD}$	0		0		0		ns
t_{WW}	$\overline{WR}$ Low width	2.5x - 40		210		160		ns
t_{DW}	Data Setup to $\overline{WR}$	2x - 50		150		110		ns
t_{WD}	Data Hold After $\overline{WR}$	30	90	30	90	30	90	ns
t_{CWA}	$\overline{RD}$, $\overline{WR}$ to Valid $\overline{WAIT}$		1.5x - 100		50		20	ns
t_{AWA}	Address to Valid $\overline{WAIT}$		2.5x - 130		120		70	ns
t_{WAS}	$\overline{WAIT}$ Setup to CLK	70		70		70		ns
t_{WAH}	$\overline{WAIT}$ Hold After CLK	0		0		0		ns
t_{RV}	$\overline{RD}$, $\overline{WR}$ Recovery Time	1.5x - 35		115		85		ns
t_{CPW}	CLK to Port Data Output		x + 200		300		280	ns
t_{PRC}	Port Data Setup to CLK	200		200		200		ns
t_{CPR}	Port Data Hold After CLK	100		100		100		ns
t_{CHCL}	$\overline{RD}$ / $\overline{WR}$ Hold After CLK	x - 60		40		20		ns
t_{CLC}	$\overline{RD}$ / $\overline{WR}$ Setup to CLK	1.5x - 50		100		70		ns
t_{CLHA}	Address Hold After CLK	1.5x - 80		70		40		ns
t_{ACL}	Address Setup to CLK	2.5x - 80		170		120		ns
t_{CLD}	Data Setup to CLK	x - 50		50		30		ns

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- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 - D7)
High 0.8V_{CC}/Low 0.2V_{CC} (excluding D0 - D7)

* t_{CA} spec is different from other parts of TLC5-90.

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4.4 A/D Conversion Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = -20 \sim 70^\circ\text{C}$ (1~12.5MHz)
 $T_A = -40 \sim 85^\circ\text{C}$ (1~10MHz)

Symbol	Parameter	Min	Typ	Max	Unit
V_{REF}	Analog reference voltage	$V_{CC} - 1.5$	V_{CC}	V_{CC}	V
AGND	Analog reference voltage	V_{SS}	V_{SS}	V_{SS}	
V_{AIN}	Allowable analog input voltage	V_{SS}		V_{CC}	
I_{REF}	Supply current for analog reference voltage		0.5	1.0	mA
Error	Total error ($T_A = 25^\circ\text{C}$, $V_{CC} = V_{REF} = 5.0V$)		1.0		LSB
	Total error			3.0	

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4.5 Zero- Cross Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = -20 \sim 70^\circ\text{C}$ (1~12.5MHz)
 $T_A = -40 \sim 85^\circ\text{C}$ (1~10MHz)

Symbol	Parameter	Condition	Min	Max	Unit
V_{zx}	Zero- cross detection input	AC coupling $C = 0.1\mu\text{F}$	1	1.8	VAC p - p
A_{zx}	Zero- cross accuracy	50/60Hz sine wave		135	mV
F_{zx}	Zero- cross detection input frequency		0.04	1	kHz

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4.6 Serial Channel Timing – I/O Interface Mode

$V_{CC} = 5V \pm 10\%$ $T_A = -40 \sim 85^\circ\text{C}$ (1~10MHz)
 $CL = 50pF$ $T_A = -20 \sim 70^\circ\text{C}$ (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		Unit
		Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x		800		ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x - 150		450		ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x - 120		80		ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0		0		ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid		6x - 150		450	ns

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4.7 16-bit Event Counter

$V_{CC} = 5V \pm 10\%$ $T_A = -40 \sim 85^\circ\text{C}$ (1~10MHz)
 $T_A = -20 \sim 70^\circ\text{C}$ (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t_{VCK}	TI4 clock cycle	$8x + 100$		900		ns
t_{VCKL}	TI4 Low clock pulse width	$4x + 40$		440		ns
t_{VCKH}	TI4 High clock pulse width	$4x + 40$		440		ns

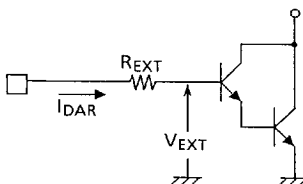
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4.8 Interrupt Operation

$V_{CC} = 5V \pm 10\%$ $T_A = -40 \sim 85^\circ\text{C}$ (1~10MHz)
 $T_A = -20 \sim 70^\circ\text{C}$ (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t_{INTAL}	NMI, INT0 Effective pulse width ()	$4x$		400		ns
t_{INTAH}	NMI, INT0 Effective pulse width ()	$4x$		400		ns
t_{INTBL}	INT1, INT2 Effective pulse width ()	$8x + 100$		900		ns
t_{INTBH}	INT1, INT2 Effective pulse width ()	$8x + 100$		900		ns

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(Reference) Definition of I_{DAR} 

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4.9 Read Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = -40~85°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V _{PP}	V _{PP} Read Voltage	—	4.5	5.5	V
V _{IH1}	Input High Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	—	0.7 × V _{CC}	V _{CC} + 0.3	V
V _{IL1}	Input Low Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	—	-0.3	0.3 × V _{CC}	V
t _{ACC}	Address to Output Delay	C _L = 50pF	—	2.25TCYC + α	ns

TCYC = 400ns (10MHz Clock)

010491

α = 200ns

4.10 Programming Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = 25 ± 5°C Vcc = 6V ± 0.25V

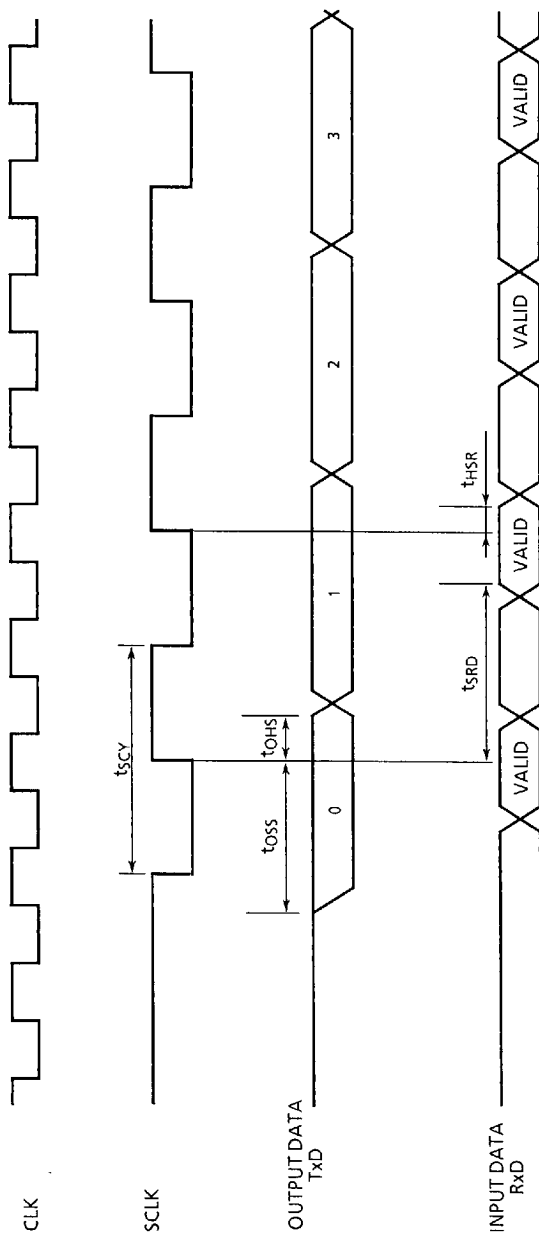
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{PP}	Programing Voltage	—	12.25	12.50	12.75	V
V _{IH}	Input High Voltage (D0~D7)	—	0.2V _{CC} + 1.1		V _{CC} + 0.3	V
V _{IL}	Input Low Voltage (D0~D7)	—	-0.3		0.2V _{CC} - 0.1	V
V _{IH1}	Input High Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	—	0.7V _{CC}		V _{CC} + 0.3	V
V _{IL1}	Input Low Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	—	-0.3		0.3V _{CC}	V
I _{CC}	V _{CC} Supply Current	f _{OSC} = 10MHz	—		50	mA
I _{PP}	V _{PP} Supply Current	V _{PP} = 13.00V	—		50	mA
t _{PW}	$\overline{CE}$ Programming Pulse Width	C _L = 50pF	0.95	1.00	1.05	ms

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■ 9097249 0040628 630 ■

4.11 I/O Interface Mode Timing Chart

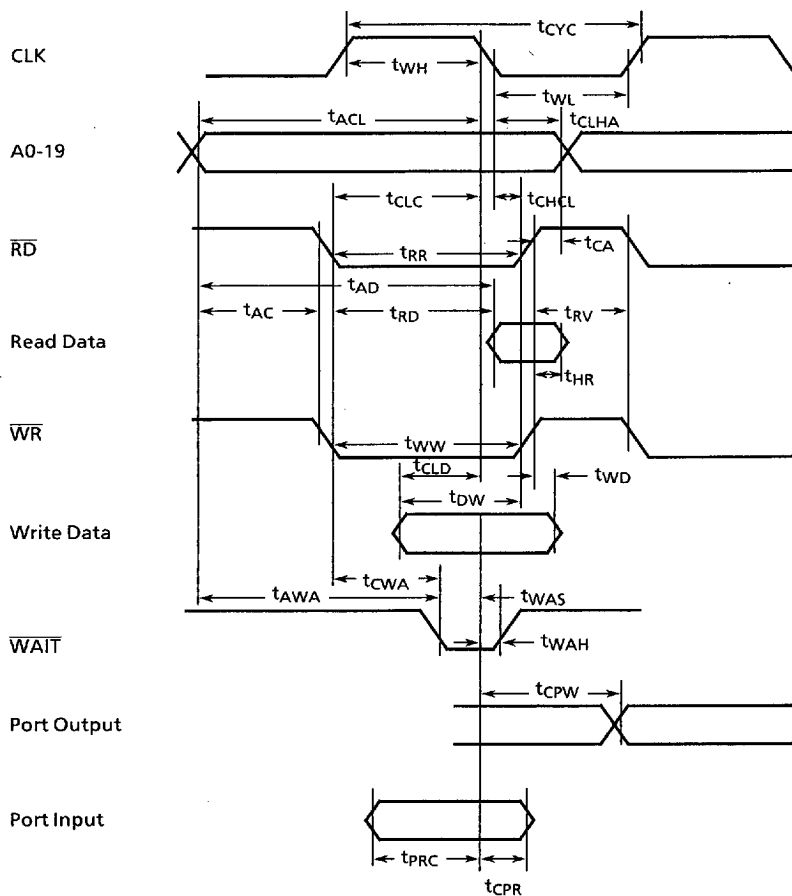


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■ 9097249 0040629 577 ■

4.12 Timing Chart

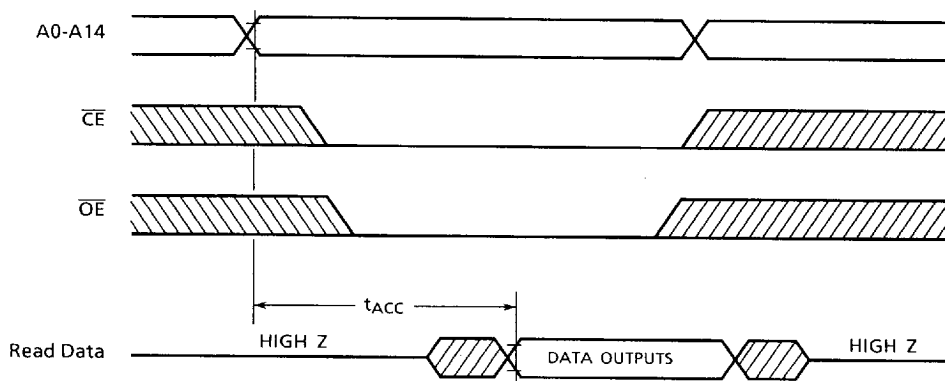


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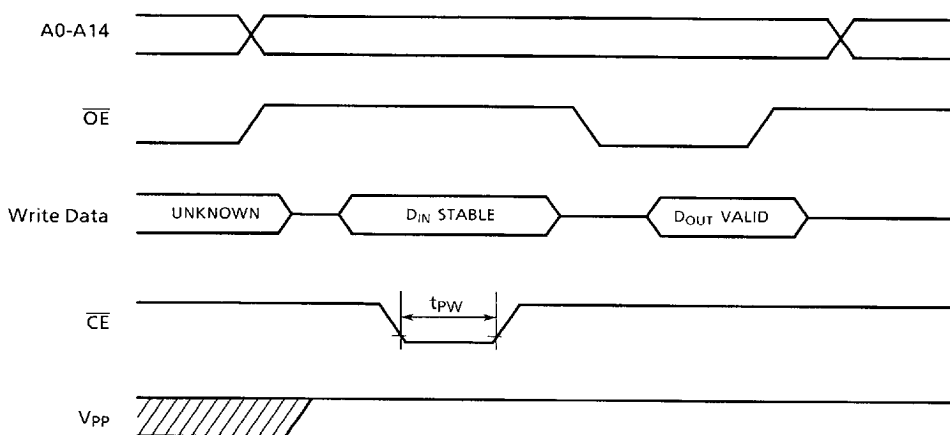
■ 9097249 0040630 299 ■

4.13 Read Operation Timing Chart (PROM Mode)



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4.14 Programming Operation Timing Chart (PROM Mode)



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 9097249 0040631 125