Low Voltage/Low Power
CMOS 16-bit Microcontrollers
TMP93CM40AF/TMP93CM41AF

1. Outline and Device Characteristics

TMP93CM40A/M41A are high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP93CM41A does not have a ROM, the TMP96CM40A has a built-in ROM. Otherwise, the devices function in the same way.

TMP93CM40AF/TMP93CM41AF are housed in 100-pin mini flat package. Device characteristics are as follows:

(1) Original 16-bit CPU (900L CPU)
- TLCS-90 instruction mnemonic upward compatible.
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- High-speed micro DMA
  - 4 channels (1.6 µs/2 bytes at 20MHz)

(2) Minimum instruction execution time
- 200ns at 20MHz

(3) Internal RAM: 2K byte
Internal ROM:

TMP93CM40A	32K-byte ROM
TMP93CM41A	None

(4) External memory expansion
- Can be expanded up to 16M bytes (for both programs and data).
- AM8/$\overline{16}$ pin (select the external data bus width).
- Can mix 8- and 16-bit external data buses.
  ···Dynamic data bus sizing

(5) 8-bit timer: 2 channels
(6) 8-bit PWM timer: 2 channels
(7) 16-bit timer: 2 channels
(8) Pattern generator: 4 bits, 2 channels
(9) Serial interface: 2 channels
(10) 10-bit A/D converter: 4 channels
(11) Watchdog timer
(12) Chip select/wait controller: 3 blocks
(13) Interrupt functions
- 2 CPU interrupts··· ···SWI instruction, and Illegal instruction
- 14 internal interrupts ┐
- 6 external interrupts ┘ 7-level priority can be set.

(14) I/O ports:
79 pins for TMP93CM40A and 61 pins for TMP93CM41A
(15) Standby function : 4 halt modes (RUN, IDLE2, IDLE1, STOP)
(16) Clock Gear Function
- High-frequency clock can be changed fc to fc/16
- Dual clock operation

(17) Wide Operating Voltage
- V_{CC} = 2.7 to 5.5V

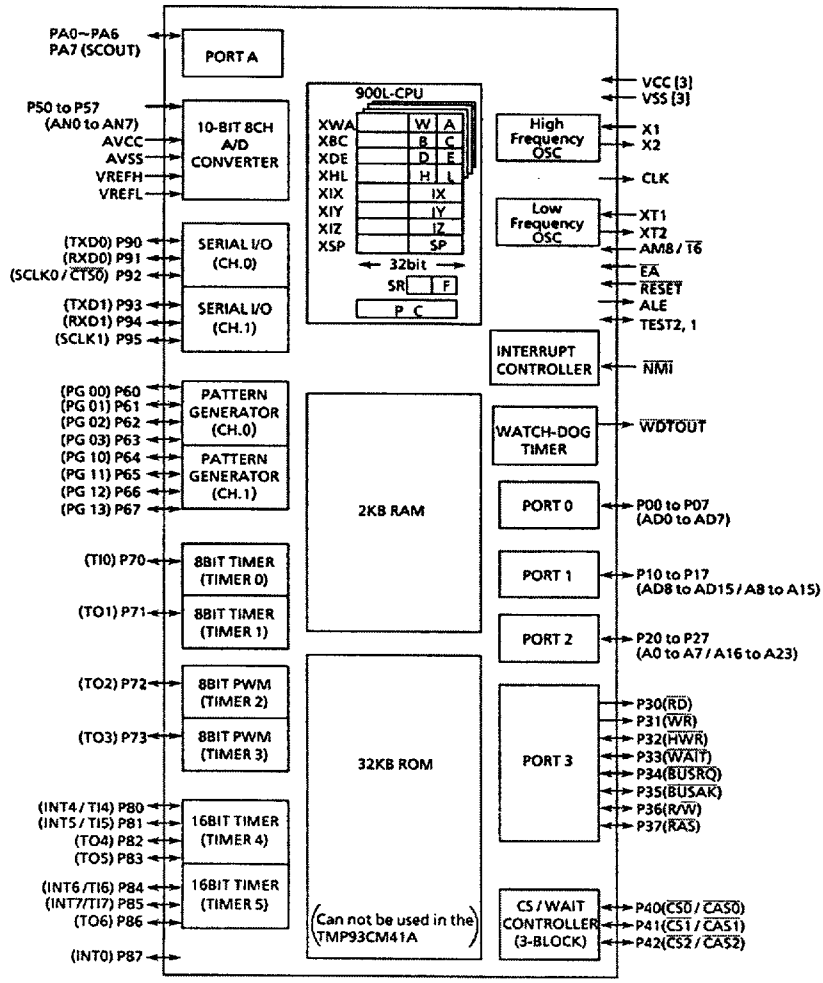


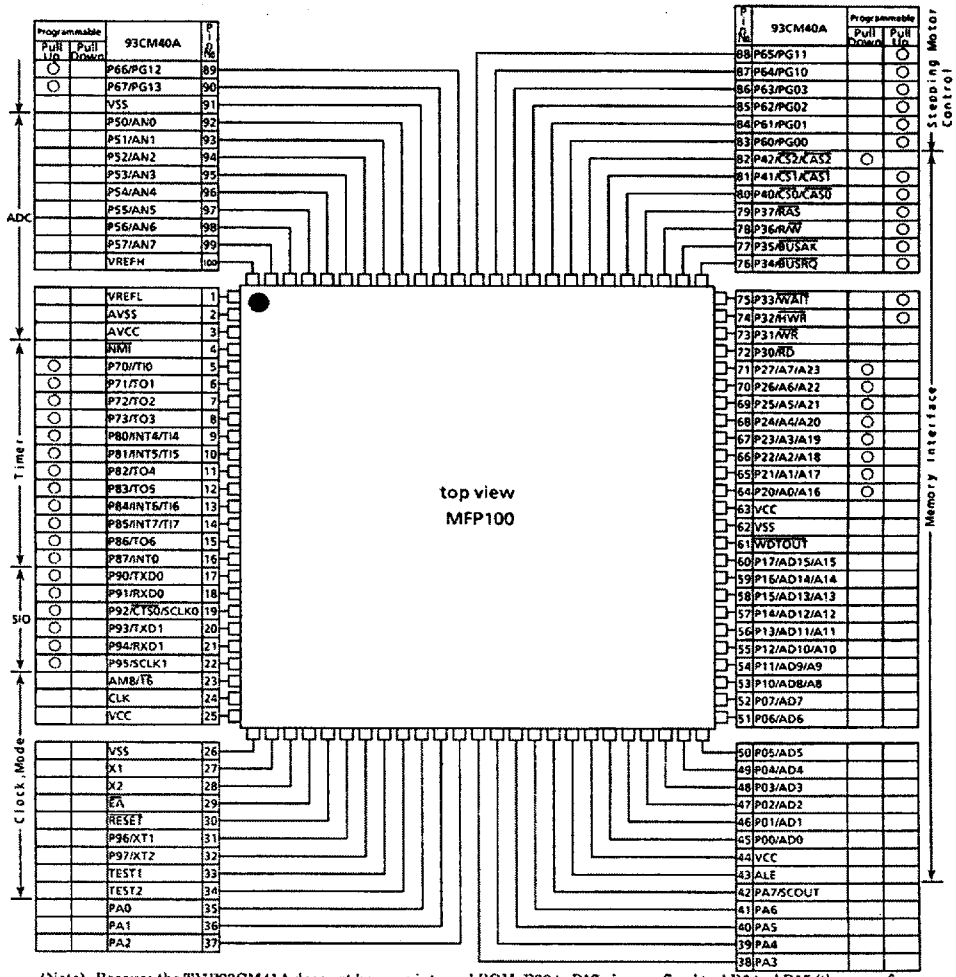
Figure 1. TMP93CM40A/TMP93CM41A Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for TMP93CM40A/ TMP93CM41A, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP93CM40A/ TMP93CM41A.



(Note) Because the TMP93CM41A does not have an internal ROM, P00 to P17 pins are fixed to AD0 to AD15 (the case of AM8/$\overline{16}$ = 0), or to AD0 to AD7, A8 to A15 (the case of AM8/$\overline{16}$ = 1) ; P30 to $\overline{RD}$; and P31 to $\overline{WR}$.

Figure 2.1. Pin Assignment (100-pin MFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2. Pin Names and Functions

Pin Name	Number of Pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected on a bit basis Address / data (lower): 0 to 7 for address / data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected on a bit basis Address data (upper): 8 to 15 for address / data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs RAS strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area.

Note: With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

Pin Name	Number of Pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-up resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P53 AN0 to AN3	4	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREF	1	Input	Pin for reference voltage input to A/D converter
AGND	1	Input	Ground pin for A/D converter
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 to 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 to 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Pin Name	Number of Pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{CTS0}$ SCKL0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial Clock I/O
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA7 SCOUT	1	I/O Output	Port A7: I/O port System clock output: Outputs system clock or 1/2 oscillation clock for synchronizing to external circuit.
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs ⌈System Clock ÷ 2 ⌋ Clock. Pulled-up during reset (can be reset to Output Disable for reducing noise).
$\overline{EA}$	1	Input	External access: "0" should be input with TMP93CM41A "1" should be input with TMP96CM40A.
AM8/$\overline{16}$	1	Input	Address mode: Selects external data bus width for external access is set by Chip Select/WAIT Control register, Port 1 Control register. For TMP93CM41A: "0" should be input with fixed 16bit bus width or 16bit bus interlarded with 8bit bus. "1" should be input with fixed 8bit bus width.
ALE	1	Output	Address latch enable. Can be set Output disable for reducing noise.
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	Oscillator connecting pin
XT1 P96	1	Input I/O	Low Frequency Oscillator connecting pin Port 96: I/O port (Open Drain Output)
XT2 P97	1	Output I/O	Low Frequency Oscillator connecting pin Port 97: I/O port (Open Drain Output)
TEST1/TEST2	2	Output Input	TEST1 Should be connected with TEST2 pin
VCC	3		Power supply pin
VSS	3		GND pin (0V)
AVCC	1		Power supply pin for A/D converter
AVSS	1		GND pin for A/D converter (0V)

Note: Pull-up/pull-down resistor can be released from the pin by software.

3. Operation

This section describes in blocks the functions and basic operations of TMP93CM40A/M41A devices.

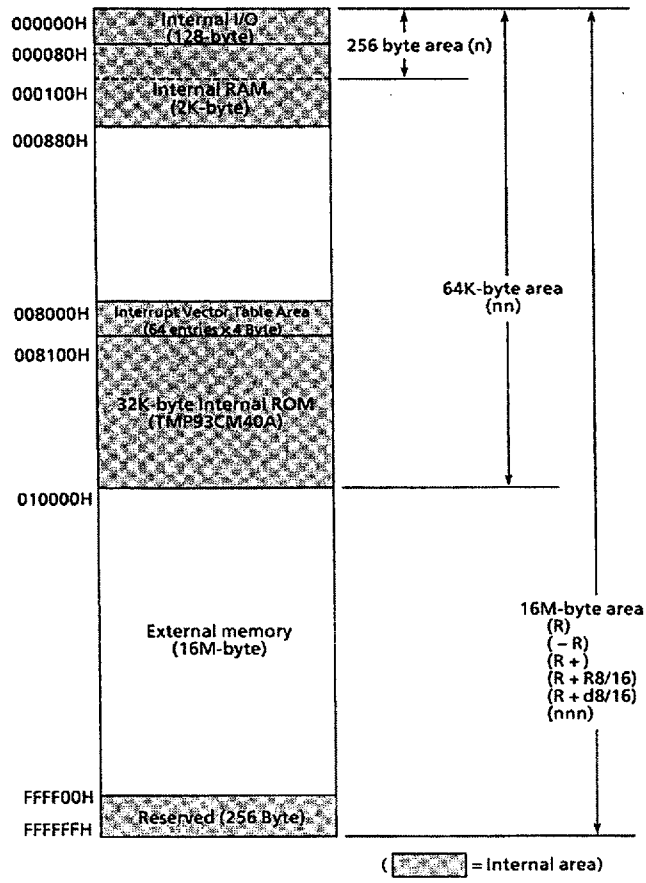
Check the [7. Care Points and Restriction] in TMP93CM40/TMP93CM41 because of the Care Points, etc., are described.

3.1 CPU

TMP93CM40A/M41A devices have a built-in high-performance 16-bit CPU (900L CPU). (For CPU operation, see TLCS-900 CPU in the previous section).

3.2 Memory Map

Figure 3.2 is a memory map of the TMP93CM40A/M41A.



Note : Resetting sets the stack pointer (XSP) to 100H.
The 256 Byte Area from FFFF00H to FFFFFFH can not be used.

Figure 3.2. Memory Map