

Low-voltage RDS / RBDS decoder

BU2661FV

The BU2661FV is a RDS / RBDS decoder that employs a digital PLL and has a built-in anti-aliasing filter and an eight-stage BPF (switched-capacitor filter). It can operate at a low-voltage power supply (from 2.7V). Linear CMOS circuitry is used for low power consumption.

●Applications

RDS / RBDS compatible FM receivers, stereo systems and FM pagers.

●Features

- 1) Low operating voltage (Min 2.7V).
- 2) Low current (Min 1.8mA).
- 3) Anti-aliasing filter.
- 4) 57kHz bandpass filter.
- 5) DSB demodulation (digital PLL).
- 6) Quality indication output for demodulated data.

●Absolute maximum ratings (Ta = 25°C)

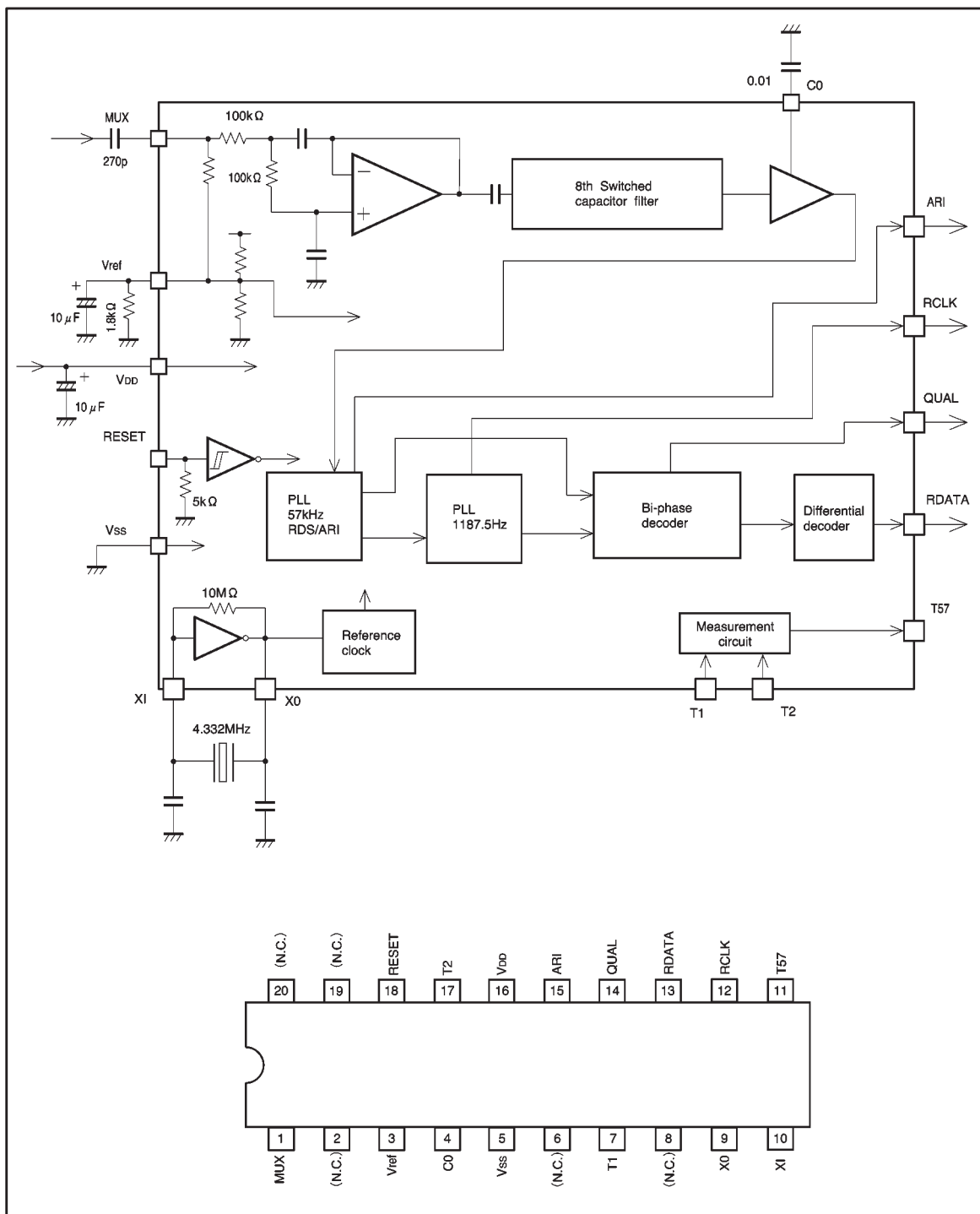
Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	V _{DD}	-0.3~+7.0	V	V _{DD}
Maximum input voltage	V _{MAX}	-0.3~V _{DD} +0.3	V	All input pins
Maximum output current	I _{MAX}	±4.0	mA	All output pins
Power dissipation	P _d	350*	mW	
Operating temperature	T _{opr}	-25~+75	°C	
Storage temperature	T _{stg}	-55~+125	°C	

*Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{DD}	2.7	—	3.3	V

● Block diagram



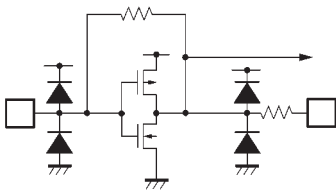
● Pin descriptions

Pin No.	Symbol	Pin name	Function	Input/output type
1	MUX	Input	Composite signal input (refer to input/output circuits)	TYPE D
2	(N.C.)	—	—	—
3	V _{ref}	Reference voltage	Refer to input/output circuits	TYPE E
4	CO	Comparator	Refer to input/output circuits	TYPE F
5	V _{ss}	—	—	—
6	(N.C.)	—	—	—
7	T1	Test input	Open or connected to ground	TYPE B
8	(N.C.)	—	—	—
9	XO	Crystal oscillator	Connects to 4.332MHz oscillator (refer to input/output circuits)	TYPE A
10	XI			
11	T57	Test output	Open	TYPE C
12	RCLK	Demodulator clock	1187.5kHz clock (refer to the timing diagram)	
13	RDATA	Demodulator data	Refer to the timing diagram	
14	QUAL	Demodulator quality	Good data: High, bad data: Low	
15	ARI	ARI signal discrimination	ARI ARI+RDS: High, RDS: Low, When no signal: Low	
16	V _{DD}	Power supply	2.7~3.3V	—
17	T2	Test input	Open or connected to ground	TYPE B
18	RESET	Reset	High: reset, Low: open operation	TYPE B
19	(N.C.)	—	—	—
20	(N.C.)	—	—	—

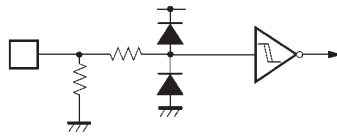
*N.C.: not connected to anything.

● Input / output circuits

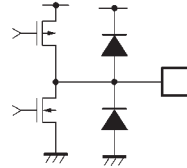
TYPE A



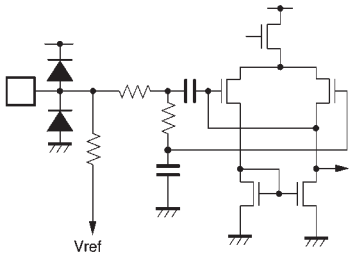
TYPE B



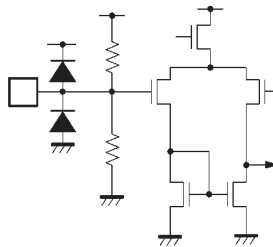
TYPE C



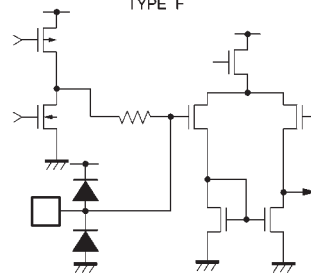
TYPE D



TYPE E



TYPE F



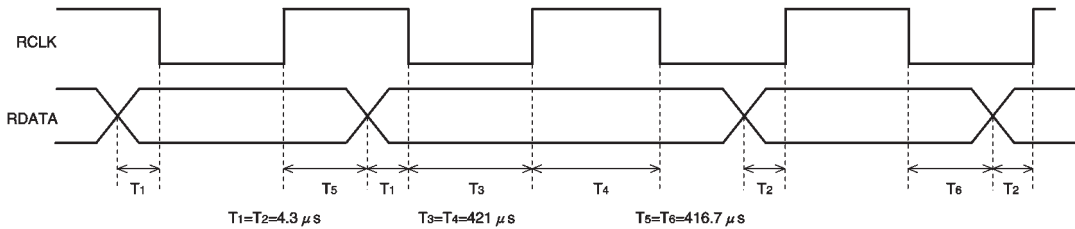
●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 3.0V, V_{SS} = 0.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Coniditions
Operating current	I _{DD1}	—	1.8	3.0	mA	I _{DD}
Power supply current at reset	I _{DD2}	—	2.4	3.5	mA	I _{DD}
Reference voltage	V _{ref}	—	1/2V _{DD2}	—	V	Pin 3
Input current 1	I _{IN1}	—	—	1.0	μA	MUX V _{IN} =V _{DD}
Output current 1	I _{OUT1}	—	—	1.0	μA	MUX V _{IN} =V _{DD}
Input current 2	I _{IN2}	—	—	1.0	μA	RESET V _{IN} =V _{DD}
Output current 2	I _{OUT2}	—	—	1.0	μA	RESET V _{IN} =V _{DD}
Input current 3		—	0.35	—	μA	XI
Output current 3		—	0.35	—	μA	XO
Output high level voltage 1	V _{OH1}	V _{DD} —1.0	V _{DD} —0.3	—	V	RCLK RDATA QUAL ARI I _o =1.0mA
Output low level voltage 1	V _{OL1}	—	0.2	1.0	V	RCLK RDATA QUAL ARI I _o =1.0mA
Input high level voltage	V _{IH}	0.8V _{DD}	—	—	V	RESET
Input low level voltage	V _{IL}	—	—	0.2V _{DD}	V	RESET
Feedback resistor	R _F	—	10.0	—	MΩ	X1-X0
〈Filter block〉						
Center frequency	FC	56.5	57.0	57.5	kHz	
Gain	GA	23	26	30	dB	F=57.0kHz
Attenuation 1	ATT1	7	10	—	dB	57kHz±4kHz
Attenuation 2	ATT2	65	80	—	dB	38kHz
Attenuation 3	ATT3	35	50	—	dB	67kHz
S / N ratio	SN	30	40	—	dB	57kHz V _{IN} =10mVrms
Maximum input level	VMAX1	—	—	500	mV	
〈Demodulator〉						
RDS detector sensitivity	SRDS	—	0.8	1.5	mVrms	
RDS input level	VRDS	1.5	—	300	mVrms	
Lockup time (RDS)	TL	—	100	200	ms	
Data rate	DRATE	—	1187.5	—	Hz	
Clock transient vs. data	CT	—	4.3	—	μs	

◎Not designed for radiation resistance.

● Circuit operation

Output data timing



The clock (RCLK) frequency is 1187.5Hz. Depending on the state of the internal PLL clock, the data (RDATA) is replaced in synchronous with either the rising or falling edge of the clock. To read the data, you may choose either the rising or falling edge of the clock as the reference. The data is valid for 416.7 μs after the reference clock edge.

QUAL pin operation: Indicates the quality of the demodulated data.

- (1) Good data: HI
- (2) Poor data: LO
- (3) No signal: LO
- (4) Noise input: HI / LO (flutters)

ARI pin operation: ARI / RDS distinction

- (1) ARI: HI
- (2) RDS + ARI: HI
- (3) RDS: LO
- (4) No signal: unstable
- (5) Noise input: unstable

RESET input pin: Resets the digital circuit. Connect to ground or leave open during operation.

● External dimensions (Units: mm)

