Microcontroller for battery chargers
BU3451

The BU3451 is a 4-bit single-chip microcontroller developed for charging circuits. It is equipped with analog and comparator inputs, and can be used for charging control of various types of batteries with very few attachments.

●Applications

Controllers using A/D, such as battery chargers

●Specifications

Series	BU3451
Program memory (ROM) (bytes)	2048
Data memory (RAM) (bits)	96×4
Subroutine nesting levels	3
Instruction sets	38
I/O ports *1	4
Input ports *2	4
Large current outputs	4
Analog inputs	4
Analog reference inputs	1
Instruction cycle (μs)	1.68 (fosc=3.58MHz)
Power supply voltage (V) typ.	5

*1 The format of the I/O circuit can be selected using the mask option. (See I/O Circuit Formats.)

*2 Standby function provided (See Description of HALT function.)

●Features

1) Equipped with 38 types of instruction sets.
2) High-speed instruction execution time (machine cycle) of 1.68 μs (3.58MHz, 5V).
3) ROM ..... 2048 × 8 bits
4) RAM (general-purpose) ..... 96 × 4 bits
5) Subroutine nesting ..... 3 levels
6) Inputs (PIX) 4
7) Inputs/outputs (PIO) 4
8) Large current outputs (POX : LED direct drive) .. 4
9) Analog inputs (ADI) ..... 4 ch
10) Comparator input (CMP) ..... 1 ch
11) Internal Power an reset
12) Internal chopping wave generator for A/D conversion (constant current source)
Adding an external capacitor to the C_{OUT} pin enables chopping wave voltage to be generated with a high level of precision. Software processing enables A/D conversion of analog input voltage.
13) Watchdog timer can be built in (mask option)
14) Ceramic oscillation possible
15) Operating frequency ..... 0.3 ~ 4.2MHz

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	−0.3～7.0	V
Power dissipation	Pd	450*	mW
Storage temperature	T_{STG}	−55～125	℃
Input voltage	V_{IN}	−0.3～V_{DD}+0.3	V
Output voltage	V_{OUT}	−0.3～V_{DD}+0.3	V

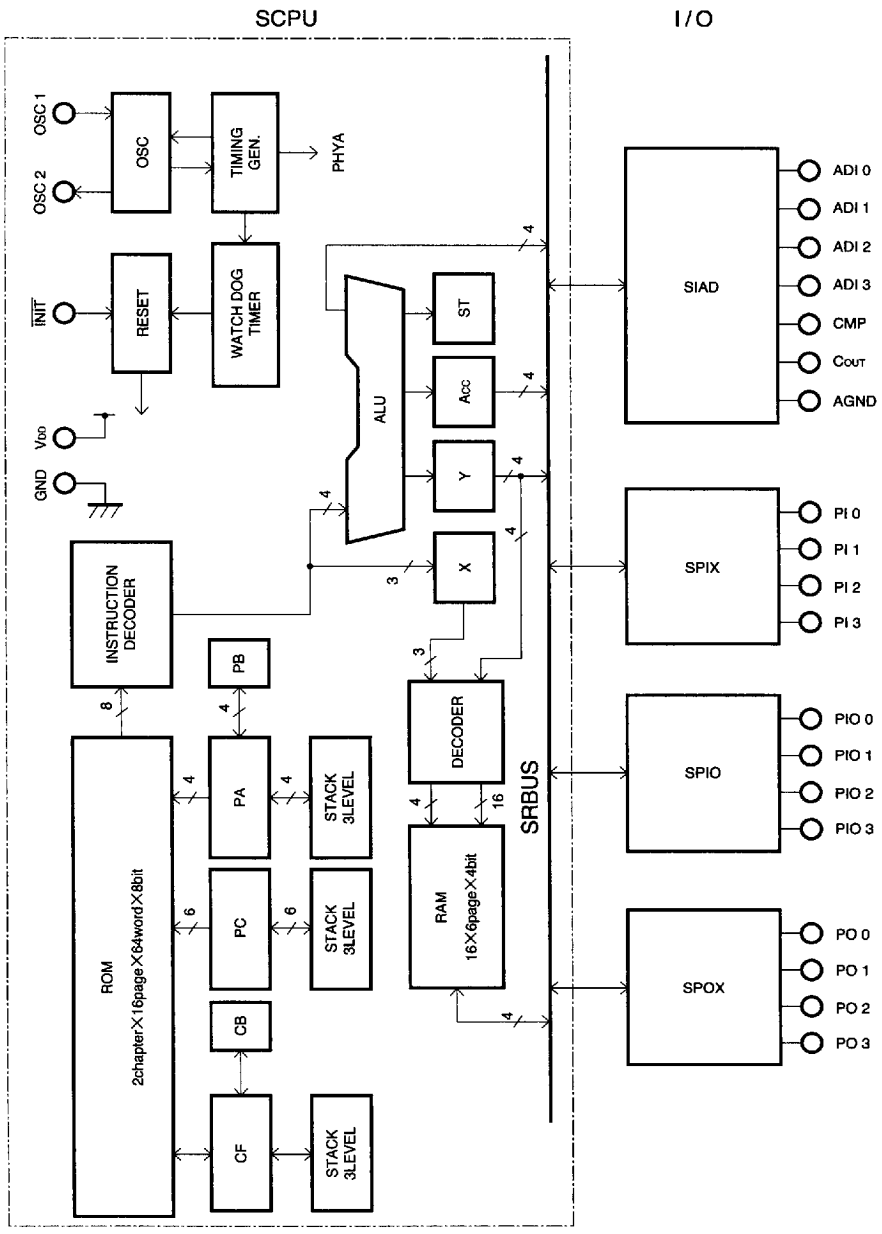
* Reduced by 4.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25℃).

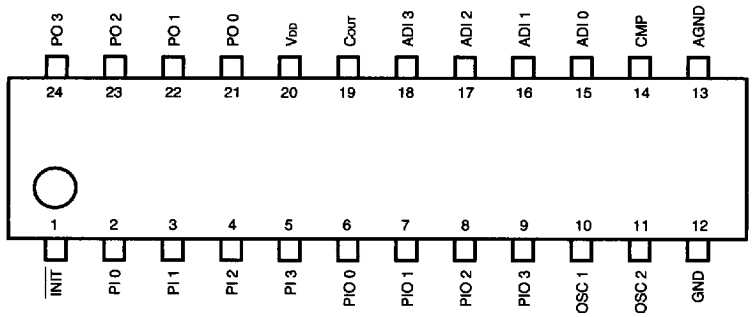
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	4.0～6.0	V
Input voltage (HIGH)*	V_{IH}	0.7V_{DD}～V_{DD}	V
Input voltage (LOW)*	V_{IL}	0.0～0.3V_{DD}	V
$\overline{INIT}$ input voltage (HIGH)	$V_{IH\ INIT}$	0.75V_{DD}～V_{DD}	V
$\overline{INIT}$ input voltage (LOW)	$V_{IL\ INIT}$	0.0～0.25V_{DD}	V
AIN input voltage	V_{IAIN}	0.6～V_{DD}−1.2	V
CMP input voltage	V_{ICMP}	0.6～V_{DD}−1.2	V
Operating temperature	T_{OPR}	−25～85	℃

* OSC1 pin and $\overline{INIT}$ pin not included.

●Block diagram



●Block diagram

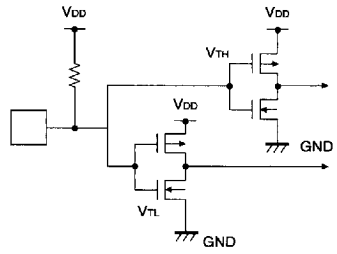
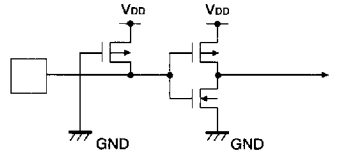
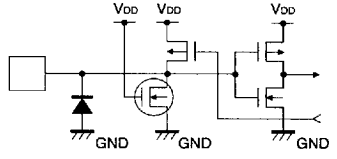
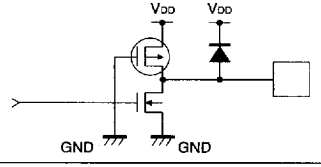
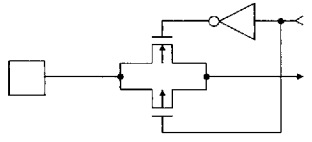
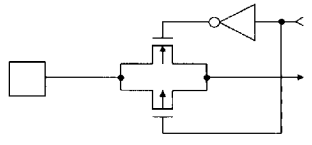


●Pin description

Pin Name	I/O	Function	Status at reset	Status in HALT mode
V_{DD}	—	Used to connect 4.0 V ~ 6.0 V power supply.	—	—
GND	—	Reference voltage for digital input/output (0 V).	—	—
AGND	—	Reference voltage for analog input (0 V).	—	—
$\overline{INIT}$	Input	INIT Manual reset input. Internal PUR*. Setting this pin to LOW sets the ROM address to 0 page, 0 address.	—	—
PI0~PI3	Input	4-bit input ports. Internal PUR *.	—	—
PIO0~PIO3	Input/output	4-bit input/output ports. Output is Pch open drain output. Input is enabled when the various outputs are LOW or Hi-Z. The mask option can be used to select whether or not PDR* is to be used for each individual bit.	Hi-Z or LOW output	—
PO0~PO3	Output	4-bit large-current Nch open drain outputs. The mask option can be used to select whether or not PUR* is to be used for each individual bit.	Hi-Z or HIGH output	—
ADI0~ADI3	Input	Analog inputs. Switching the four inputs is done via the program.	ADI0 selected	—
CMP	Input	Analog reference voltage input; used with comparator operation.	Not selected	—
COUT	Output	A capacitor is connected between this and GND (to produce chopping waves).	LOW output	—
OSC1	Input	Clock generator input pin.	—	H
OSC2	Output	Clock generator output pin.	—	H

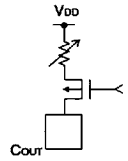
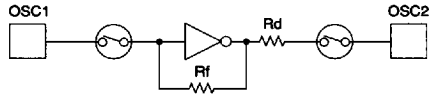
— : No change in status (status maintained)
PUR* : Pull-up resistance
PDR* : Pull-down resistance

●Input/output circuits

Pin Name	I/O	I/O Circuit	Notes
$\overline{INIT}$	Input		Hysteresis input Internal pull - up resistor About.400kΩ
PI0~PI3	Input		For pull-up Internal MOS Tr About.100kΩ
PIO0~PIO3	Input/output		For pull-down Internal MOS Tr About.100kΩ
PO0~PO3	Output		Large-current output For pull-up Internal MOS Tr About.100kΩ
ADI0~ADI3	Input		Analog input
CMP	Input		Analog input

○ Items are mask options.

●Input/output circuits

Pin Name	I/O	I/O Circuit	Notes
COUT	Output		
OSC1	Input		Internal MOS Tr for feedback Rf : About. 1 MΩ Internal damping resistance Rd : About. 1 kΩ
OSC2	Output		

○ Items are mask options.

●Electrical characteristics (Unless otherwise noted, Ta=25℃, V_{DD}=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
$\overline{INIT}$ "H" input current	I_{IHIT}	−1.0	−	+1.0	μA	$V_I=V_{DD}$	Fig.1
$\overline{INIT}$ "L" input current	I_{ILIT}	−6	−11	−20	μA	V_I=GND	Fig.1
OSC1 "H" input current	I_{IHOSC}	−1.0	−	+1.0	μA	$V_I=V_{DD}$ With ceramic oscillation	Fig.1
OSC1 "L" input current	I_{ILOSC}	−2	−5	−10	μA	V_I=GND With ceramic oscillation	Fig.1
OSC1 input current	I_{IOSC}	−1.0	−	+1.0	μA	With CR oscillation	Fig.1
"H" input current	I_{IH}	−1.0	−	+1.0	μA	$V_I=V_{DD}$ PIX	Fig.1
"L" input current	I_{IL}	−35	−65	−120	μA	V_I=GND PIX	Fig.1
"L" output voltage	V_{OL}	−	0.25	0.4	V	I_{OL}=10mA POX	Fig.3
"H" output voltage	V_{OH}	4.4	4.6	−	V	I_{OH}=−1.0mA PIO	Fig.2
"H" output current	I_{OH}	−35	−65	−120	μA	With pull-up resistance POX Output Tr: OFF	Fig.4
"L" output current	I_{OL}	35	65	120	μA	With pull-down resistance PIO Output Tr: OFF	Fig.5
Open drain output leakage current	I_L	−1.0	−	+1.0	μA	With no pull-up or pull-down resistance POX, PIO	Fig.6 Fig.7
ADI input current	I_{ADI}	−1.0	−	+1.0	μA		Fig.8
CMP input current	I_{CMP}	−1.0	−	+1.0	μA		Fig.8
Comparator offset voltage	V_{FOFF}	−10	0	+10	mV	V_{in}=0.6~3.8 (V)	−
Triangular wave peak value voltage	V_{PEAK}	3.8	3.9	−	V		−
*1 A/D conversion differential error	V_{DERR}	+1.5	0	−1.5	mV	External C=0.1 μF f=3.58MHz When using 11-bit precision program	−
Operating circuit current	I_{DDOP}	0.3	0.8	2.0	mA	f_{OSC}=3.58MHz Comparator stopped, ceramic oscillation	Fig.10
Static circuit current	I_{DDST}	−	−	+1.0	μA	In HALT mode (oscillation stopped)	Fig.9
Operating frequency	f_{CK}	0.3	−	4.2	MHz	External clock	−

©Not designed for radiation resistance

●Measurement circuits

Fig.1 ① Input current (HIGH) measurement circuit
② Input current (LOW) measurement circuit

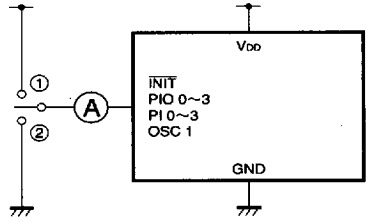


Fig. 2 Output voltage (HIGH) measurement circuit (Output Pch - Tr: ON)

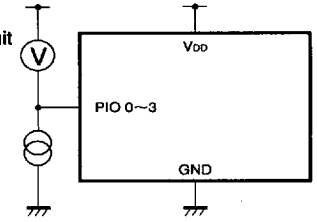


Fig. 3 Output voltage (LOW) measurement circuit (Output Nch - Tr: ON)

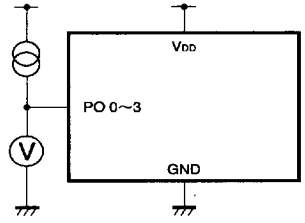


Fig. 4 Output current (HIGH) measurement circuit (Output Nch - Tr: OFF)

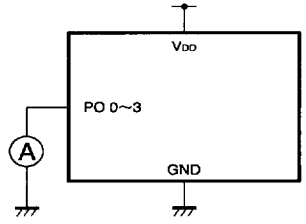


Fig. 5 Output current (LOW) measurement circuit (Output Pch - Tr: OFF)

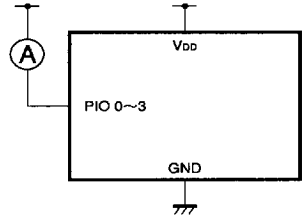
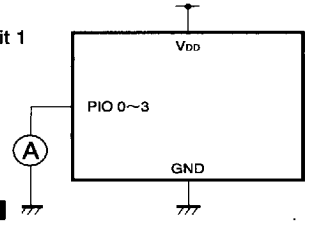


Fig. 6 Output leakage current measurement circuit 1 (Output Pch - Tr: OFF)



●Measurement circuits

Fig. 7 Output leakage current measurement circuit 2 (Output Nch - Tr: OFF)

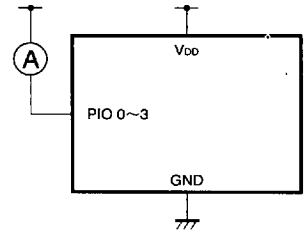


Fig. 8 ADI, CMP input current measurement circuit

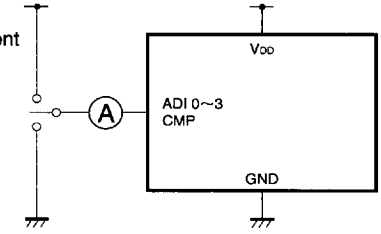


Fig. 9 Current measurement circuit (circuit stopped) (HALT mode)

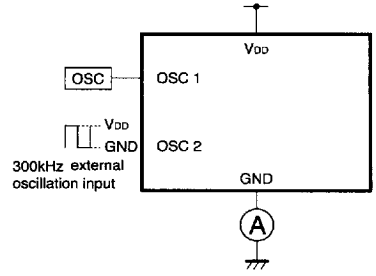
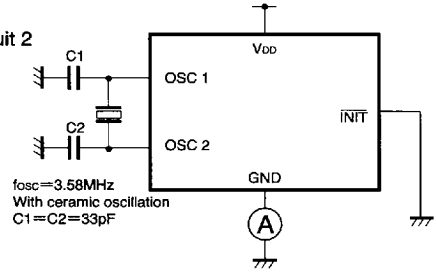


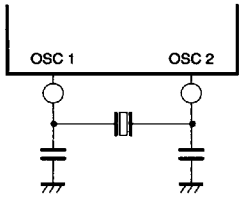
Fig. 10 Current measurement circuit 2 (circuit operating)



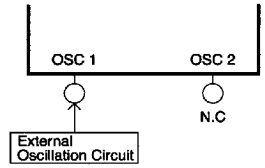
●Clock generator

The clock generator can produce oscillation either through a ceramic resonator or external input. If ceramic oscillation is used, clock signals are obtained through an internal feedback resistance and damping resistance, and an external ceramic resonator and oscillation capacitor. (When selecting the ceramic resonator, please refer to the recommended values of the pertinent manufacturer.)

If clock signals are being input from an external source, they are input through the OSC1 pin, and the OSC2 pin is left open.



Ceramic oscillator external circuit



External clock input circuit

≪Oscillation circuit configuration example≫

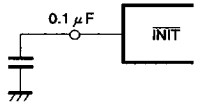
●Reset function

Two reset functions are available to initialize the CPU. When the CPU is initialized, the program counter executes instructions from 0 page, 0 address.

(1) Reset through an external pin

A reset can be executed by setting the INIT pin to LOW, which is done by specifying an interval of four or more machine cycles. (One machine cycle = $1/f_{OSC} \times 6$)

If a reset is executed by turning on the power supply, a capacitor can be connected between the INIT pin and the GND and an integrated circuit configured with the internal pull-up resistance (approximately 400kΩ). This generates a reset pulse when the power supply is turned on. However, this method is effective only when a valid reset pulse is input while the power supply voltage is within the operating voltage range and the clock oscillation has stabilized.



≪ Initial reset Circuit configuration example≫

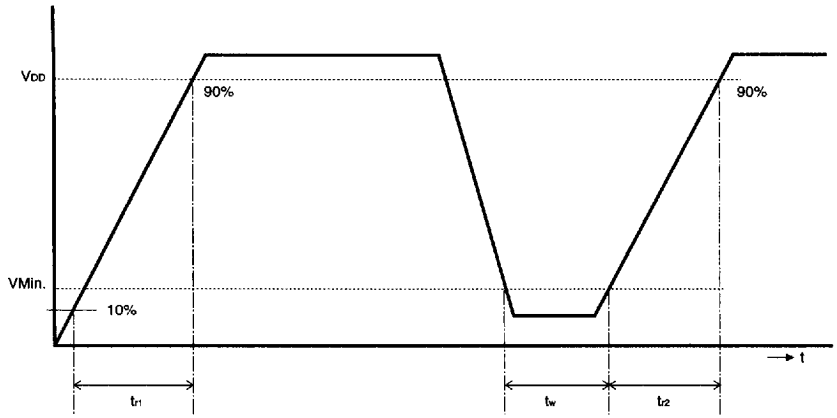
* Capacitor value must be changed according to the rising time of power supply.
(The power supply rising time shown in the circuit example is at 10 ms or less.)

(2) Reset using the power on reset circuit

the power on reset circuit is valid when the following conditions are satisfied. In this case, the external capacitor on the INIT pin may be omitted.

Power on reset standard (Ta=25℃, V_{DD}=5 V, fck=3.58 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply rise time	t_{r1}	—	—	5	ms	VMin.=2.5V
Rise time when interrupted	t_{r2}	—	—	5	ms	VMin.=2.5V
Power supply interrupt time	tw	5	—	—	ms	VMin.=2.5V



≪Power ON reset operation≫

●HALT function

By executing the HALT command, the microcontroller goes to HALT state.

・In HALT state:

1. Oscillation comes to a halt and current consumption is reduced to an extremely low level.
2. The watchdog timer (WDT) is reset.
3. Each output pin keeps the value it was at prior to HALT state.

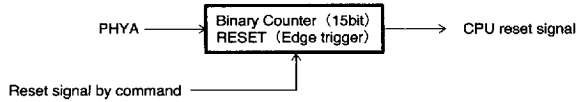
When executing the HALT OFF function, the mask option can be used to reset any or all of the bits in PIX input. When any of the PIX input settings is set to "L", the HALT state is canceled.

・When the HALT state is canceled:

1. Segments with unstable oscillation (during ceramic oscillation) are disabled, for which reason regular operation does not resume until the wait timer has gone into operation and the effective clock is set to 1024 × 6.
2. When the microcontroller returns to regular operation, the WDT resumes counting from 0. However, the conditions for cancellation of HALT already exist when the HALT command is executed, the microcontroller treats the HALT command as an NOP command, and does not enter HALT state.

●Watchdog timer

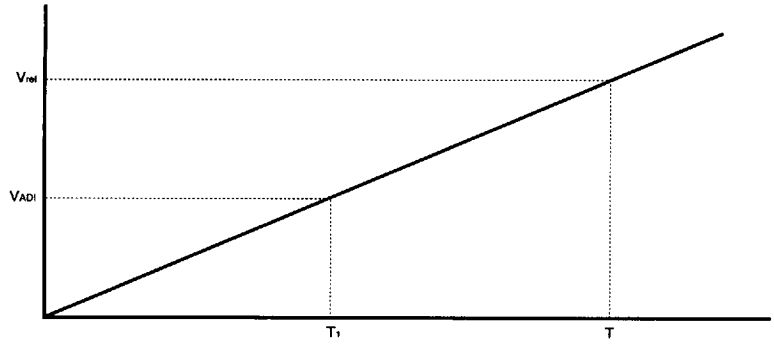
Using the mask option, a watchdog timer can be used for runaway monitoring. The watchdog timer is configured of a 15-bit binary counter, and a clock signal of fosc/6 is input as the initial stage input. When this counter overflows, a CPU reset signal is issued, and the system is initialized. The overflow detection time is set to 2^{14}/PHYA (23ms at 4.2MHz ; PHYA = fosc/6). Normally, prior to the overflow of the binary counter, the Watch Dog Timer Reset (WDTR) instruction must be executed in order to reset this counter.



≪Watchdog timer block diagram≫

●Analog input

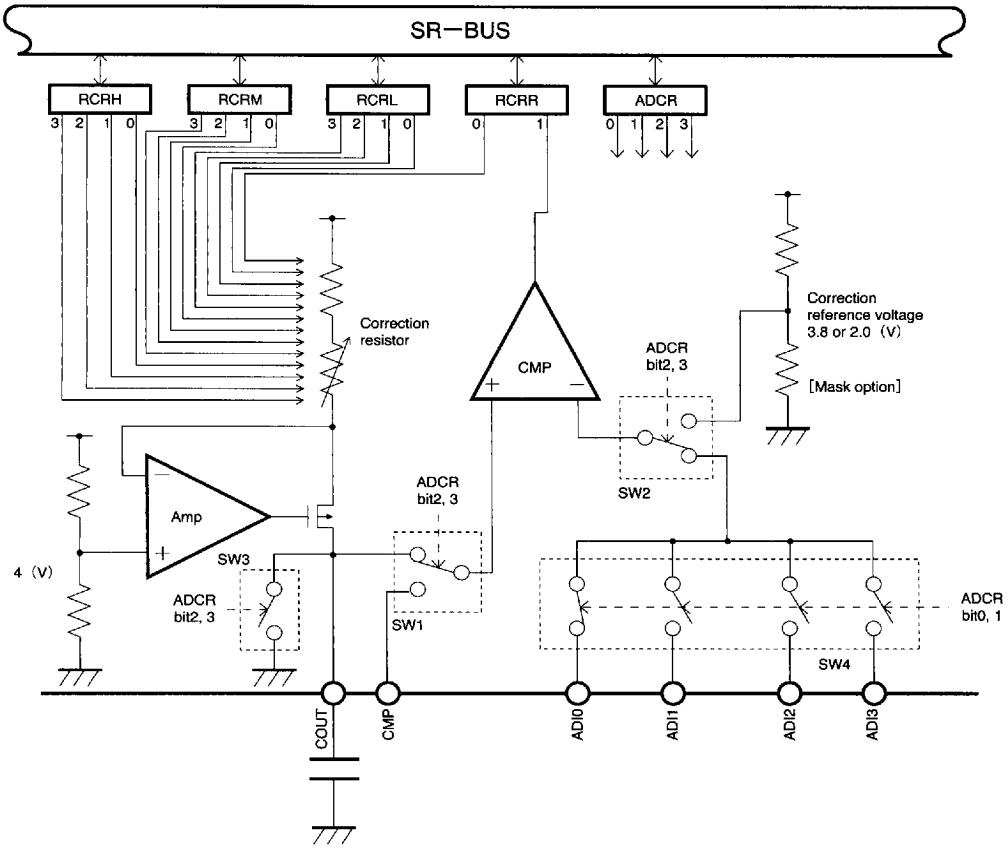
Analog input is used in A/D conversion and comparison of the voltage input through the analog input pins (ADI0 ~ 3). A/D conversion is carried out by a chopping wave voltage being created when the external capacitor on the C_{OUT} pin is charged with constant current, and the voltage of the chopping wave is compared with that of the analog input pins. The time from the beginning of charging to the point where the comparison results are inverted serves in relative terms as the input voltage and A/D conversion is carried out. The inclination of the chopping wave can be determined by the external capacitor.



$V_{ADI}=V_{ref}\times(T_1 / T)$

V_{ref} : Triangular wave peak value
V_{ADI} : Analog input voltage
T : Time for reaching peak value
T_1 : Comparison result inversion time

≪Relationship between triangular wave and analog input voltage≫



≪A/D convertor configuration diagram≫

[A/D conversion control register (ADCR)]
Operating mode setting (Bits 2 and 3 of ADCR)
Analog input pin selection (Bits 0 and 1 of ADCR)
When reset, the AINO pin is selected at operation stop.

A/D conversion control register (ADCR)

	bit3	bit2	bit1	bit0
0	Operating mode settings		Selection of analog input pin	
1				

Operating mode settings (ADCR bit 2 and bit 3)

bit3	bit2	Operating mode	Reference voltage
0	0	Operation stopped	—
0	1	A/D converter mode	Cout voltage
1	0	Comparator operating mode	CMP voltage
1	1	Set-up mode for compensated resistance	Cout voltage

Selecting analog input pin (ADCR bit 0, bit 1)

bit1	bit0	ADI pin selection
0	0	ADI 0
0	1	ADI 1
1	0	ADI 2
1	1	ADI 3

[Correction resistance control registers (RCRH, RCRM, RCRL, RCRR)]
In order to compensate for inclination of the chopping wave, an internal resistance is provided which can be set via the software (Bit 13). The resistance value can be selected within a range from around 60kΩ to 260kΩ in units of 25Ω, centering around 160kΩ. To set the correction resistance, the chopping wave is compared with the internal comparison voltage. The comparison voltage used when setting the correction resistance can be specified as one of two voltages, using the mask option.

Comparison voltages for correction resistance setting (V_{DD}=5.0V)

Symbol	Min.	Typ.	Max.	Unit	Conditions
A	—	2.00	—	V	Set using mask option
B	—	3.8	—	V	

Correction resistance control register H (RCRH).
Bits 0, 1, 2, and 3 are used to set the resistance value, based on the correction resistance.
Correction resistance control register H (RCRH).

	bit3	bit2	bit1	bit0
0	Setting of correction resistance			
1				

Correction resistance control register M (RCRM).
Bits 0, 1, 2, and 3 are used to set the resistance value, based on the correction resistance.
Correction resistance control register M (RCRM).

	bit3	bit2	bit1	bit0
0	Setting of correction resistance			
1				

Correction resistance control register L (RCRL).
Bits 0, 1, 2, and 3 are used to set the resistance value, based on the correction resistance.
Correction resistance control register L (RCRL).

	bit3	bit2	bit1	bit0
0	Setting of correction resistance			
1				

Correction resistance control register R (RCRR)
Bit 0 is used to set the resistance value, based on the correction resistance.
Bit 1 is used to store the comparison results data (read only).

	1	0
0	V_{ADI} > Reference voltage	Setting of correction resistance
1	V_{ADI} < Reference voltage	

Setting the correction resistance (set values)

	RCRH				RCRM			
	bit3	bit2	bit1	bit0	bit3	bit2	bit1	bit0
0	0	0	0	0	0	0	0	0
1	101215	50657	25337	12647	6324	3150	1569	792

	RCRL				RCRR
	bit3	bit2	bit1	bit0	bit0
0	0	0	0	0	0
1	410	204.5	102	68	34

Because an internal fixed resistance of 58275.06Ω is provided, the correction resistance will be the selected value added to 58275.06Ω. When a reset is carried out, each bit is reset to 0, and the correction resistance value is set to 58275.06Ω. The various resistance values are used as the reference values.

●Principle of A/D conversion

The A/D conversion circuit in the BU3451 is generally like that shown below.

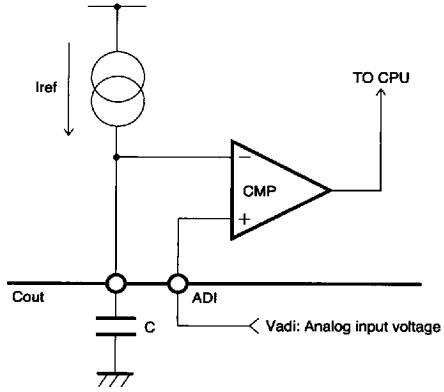


Fig. 11 A/D conversion circuit

The triangular wave is created by this constant current circuit and an external capacitor.
The time required to arrive at the internal reference voltage (Vref) is assumed to be T1, and the time required to arrive at the analog input voltage (ADI) is read as T2.
Based on this, the value of the analog input voltage in relation to Vref can be judged.

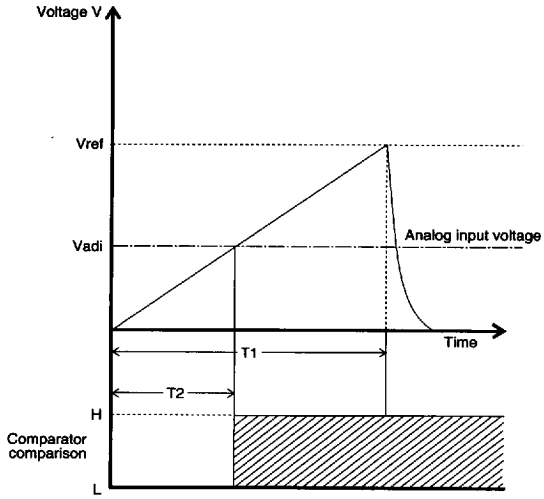
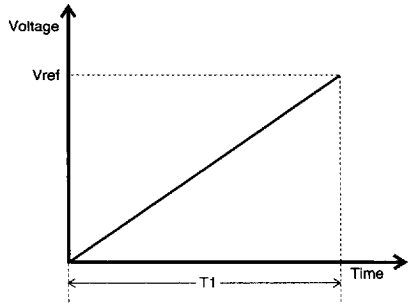


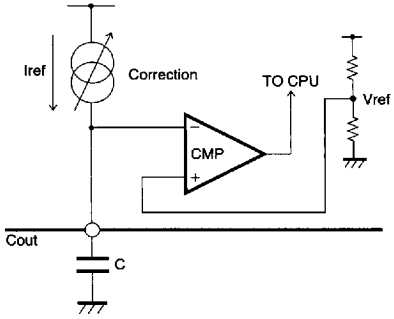
Fig. 12 A/D conversion waveform

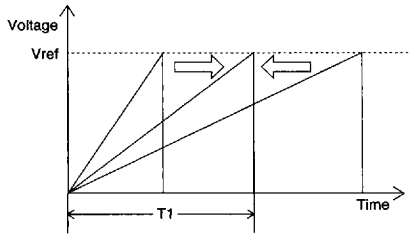
●Constant current adjustment

In A/D conversion, the T1 time is determined by the program, based on the A/D resolution. Thus, before A/D conversion is carried out, the triangular wave must be adjusted to the following inclination.



The constant current section has a 13-bit weighting, and the inclination of the triangular wave is adjusted by the program, by carrying out conversion 13 times.





●A/D conversion principle and constant current adjustment time

(1) Constant current adjustment time

In the constant current section, the resistance with the 13-bit weighting is set to the optimum resistance value. Specifically, conversion is being continually carried out to judge whether or not each of the 13 individual resistances is valid. For this reason, a time period which is 13 times the A/D conversion time is required.

A/D resolution (bits)	8	9	10	11
Constant current adjustment time (msec)	54.9	139.8	279.6	559.1

(2) A/D conversion time

The program periodically checks the results of the comparison between the external A/D input and the internal triangular wave, and reads the A/D count as the number of counts when the results are inverted (the A/D input exceeds the chopping wave). For this reason, the time required for A/D conversion is as follows.

A/D resolution (bits)	8	9	10	11
Constant current adjustment time (msec)	4.2	10.8	21.5	43.0

●External capacitor

The capacitance of the external capacitor is based on the A/D resolution, as shown below.
A film capacitor should be used.

A/D resolution (bits)	8	9	10	11
Capacitance (nF)	8.2	18	33	68

●A/D error

The method by which A/D error for the BU3451 is calculated is shown below.

(1) The error for 1LSB is determined.
The error for 1LSB is determined using the following equation.

$$1\text{LSB error} = \frac{(\text{Vref} \pm \text{corrected error}) \times (\text{Vref error}) \times (\text{power supply error})}{2^{(\text{A/D resolution})}}$$

Vref : Reference voltage built into the microcontroller (3.8V or 2)
Correction err : Error produced when correcting the internal correction resistance in the microcontroller. +0.06%, -0% in relation to Vref (if REF = 3.8V, +2.28mV, -0V)
Vref error : Error for Vref (±1.3%)
Power supply error : Power supply error applied to the microcoroller (±?% (Ex. : ±4%))
A/D resolution : A/D resolution expressed as a number of bits (normally a value between 8 and 12 bits)

(2) Determine the A/D reading error in relation to the threshold value that has to be read. Determine the maximum and minimalues for the A/D reading.
Max. = (threshold value) × (maximum value for 1 LSB) + (comparator offset) + (quantum error)
Min. = (threshold value) × (maximum value for 1 LSB) − (comparator offset) − (quantum error)

Threshold value : Threshold value specified by the microcontroller program (LSB value)
Max./Min./ values for 1LSB : Maximum and minimum values for the error of 1LSB determined in step (1).
Comparator offset : Offset voltage of the comparator built into the microcontroller (±10mV)
Quantum error : Error wh A/D conversion is carried out
The quantum error is as follows, depending on how the threshold value is determined.

How threshold value is determined	Quantum error
Rounded off to upper value	+1. -0 LSB
Rounded off to lower value	+0. -1 LSB
Rounded off to whichever value is closer	±0.5 LSB

The results determined from steps (1) and (2) above serve as the A/D error for the microcontroller.
Please note the precautions on the following page concerning this procedure.

●Application example

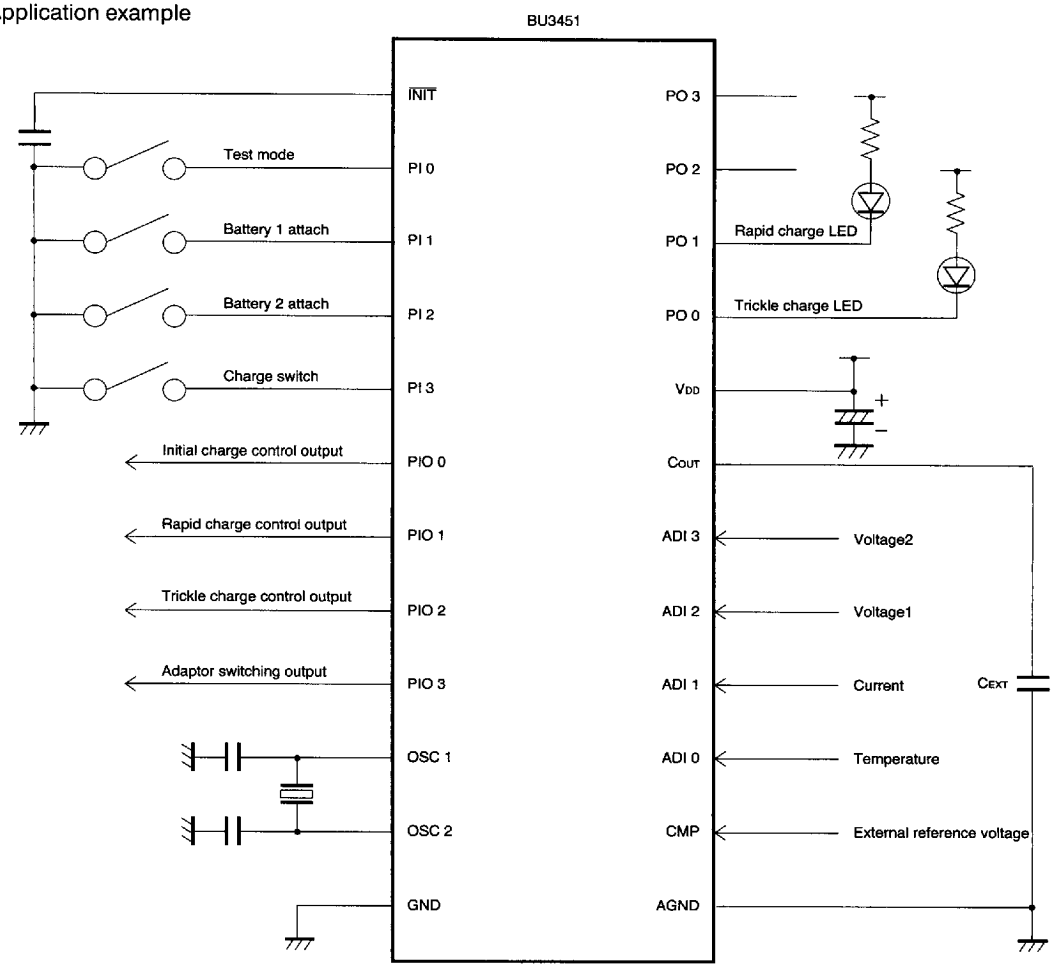


Fig.13 Application example showing use in battery charger

●Precautions

(1) In actual use, the tolerance range for the threshold value should be determined based on this result and the error up to the point of microcontroller input.

(2) The power supply error in step (1) is produced because the microcontroller Vref is configured of the resistance divisions of the power supply. If the power supply error is such as the A/D input is the same as Vref, the power supply error should be ignored. For instance, this applies in cases where the battery thermistor is used and the divided resistance value is used for the A/D input.

(3) The error is the absolute value from the equations on the previous page. When determining an absolute value (such as $-\Delta V$), the following should be ignored : the power supply error in step (1), and the comparator offset in step (2). Also, the quantum error at this point will be $+0/-1$ LSB.

(4) This error calculation does not include error based on leakage current from the capacitor. In order to minimize influence from leakage current, a film capacitor should be used.

●Electrical characteristic curves

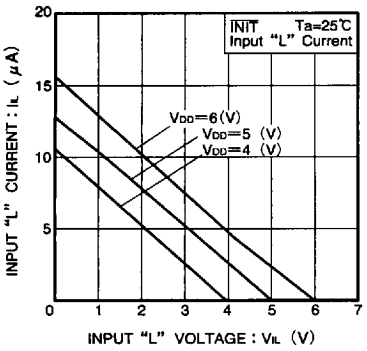


Fig. 14 INIT input "L" current characteristic

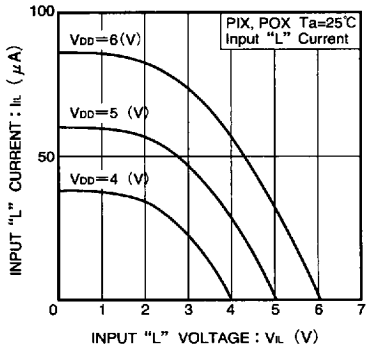


Fig.15 PIX and POX input "L" current characteristic

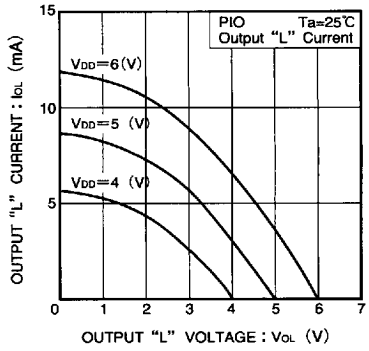


Fig.16 PIO output "L" current characteristic

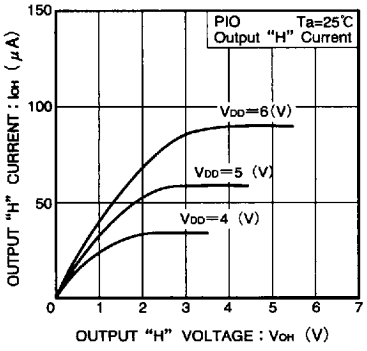


Fig.17 PIO output "H" current characteristic

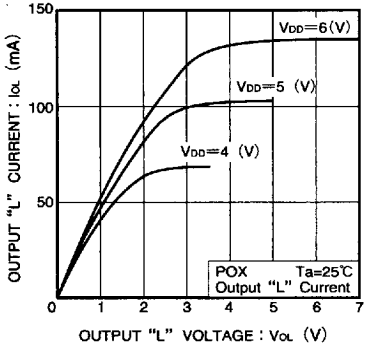


Fig. 18 POX output "L" current characteristic

●External dimensions (Units: mm)