Zytrex

ZX54AHCT
ZX74AHCT

193

February 1985

OBJECTIVE
SPECIFICATIONS

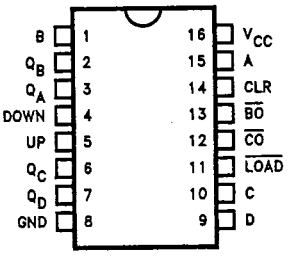
Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

T-45-23-09

Features

- **Look-ahead circuitry enhances cascaded counters**
- **Fully synchronous in count modes**
- **Parallel asynchronous load for modulo-N count lengths**
- **Asynchronous clear**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: 74AHCT: −40°C to +85°C 54AHCT: −55°C to +125°C**

Pin Configuration



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Description

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

Fabricated using Zytrex's proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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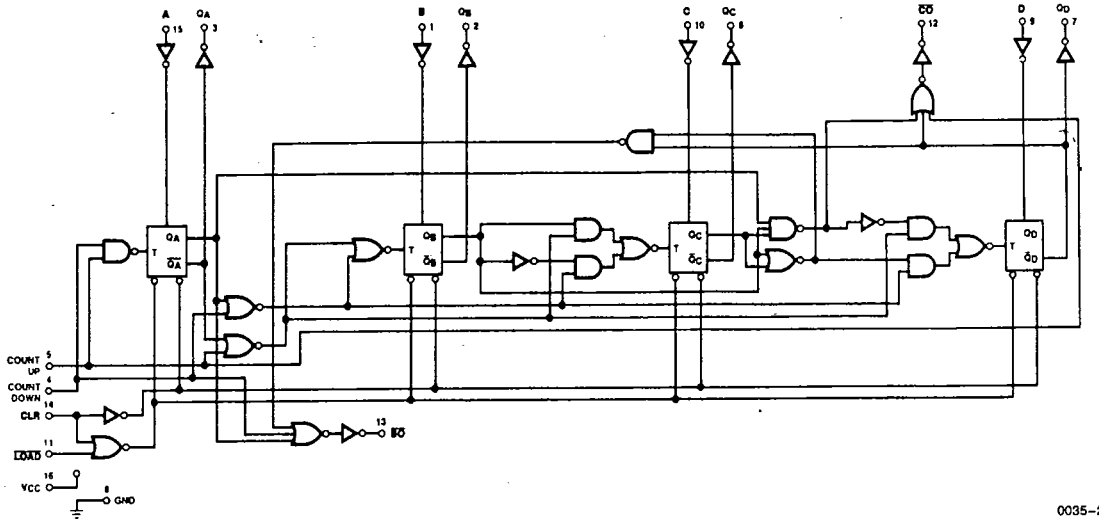
Logic Diagram



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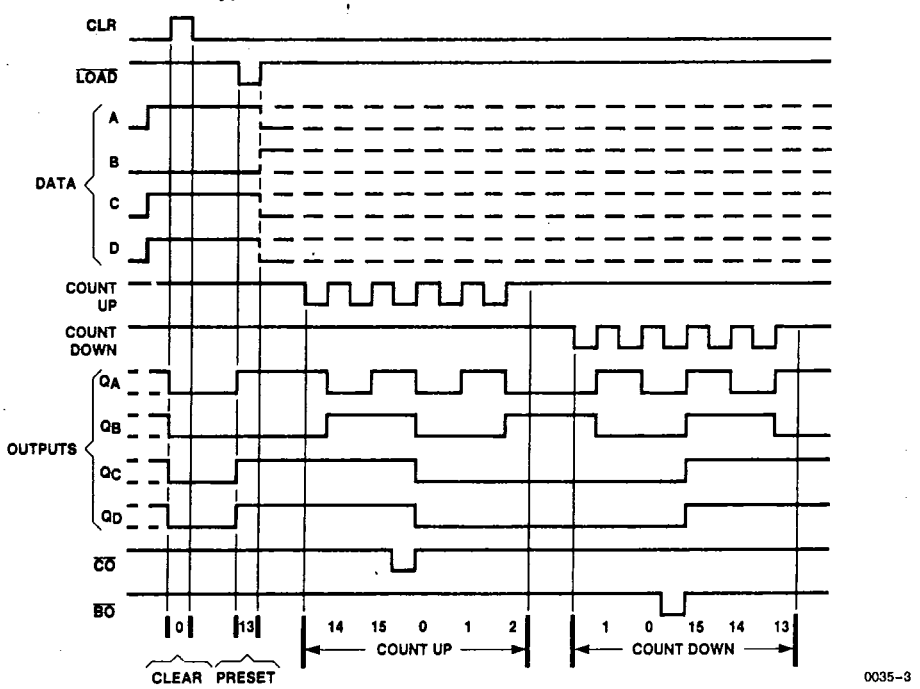
Typical Clear, Load, and Count Sequences



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Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

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Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} ..... −0.5V to 7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ..... ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ..... ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{STG} .. −65°C to +150°C
Power Dissipation Per Package, P_D† ..... 500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12 mW/°C from 65°C to 85°C
Ceramic Package (J): −12 mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature Range
ZX74AHCT: −40°C to +85°C
ZX54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics (V_{CC} = 5V ± 10% Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	T_A = 25°C	74AHCT T_A = −40°C to +85°C	54AHCT T_A = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\ \mu A$ $I_O = -4$ mA	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20\ \mu A$ $I_O = 4$ mA $I_O = 8$ mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$		8.0	80.0	160.0	μA

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AC Electrical Characteristics (Input t_r, $t_f \leq 2$ ns), AHCT193

Symbol	Parameter		Conditions†	$T_A = 25°C$ $V_{CC} = 5.0V$	74AHCT $T_A = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	54AHCT $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits		
f_{max}	Maximum Clock Frequency		$C_L = 50$ pF	50	30	25	MHz
t_{PLH}	Maximum Propagation Delay, UP to CO			12	19	23	ns
t_{PHL}				12	19	23	
t_{PLH}	Maximum Propagation Delay, DOWN to BO			11	18	22	ns
t_{PHL}				11	18	22	
t_{PLH}	Maximum Propagation Delay, UP or DOWN to any Q			18	30	36	ns
t_{PHL}				18	30	36	
t_{PLH}	Maximum Propagation Delay, $\overline{LOAD}$ to any Q			16	26	31	ns
t_{PHL}				16	26	31	
t_{PHL}	Maximum Propagation Delay, CLR to any Q			13	22	26	ns
t_w	Minimum Pulse Width	CLR High		6	10	15	ns
		$\overline{LOAD}$ Low		6	10	15	
		UP or DOWN High or Low		6	10	15	
t_{su}	Minimum Setup Width	Data before $\overline{LOAD}$ ↑		6	10	15	ns
		CLR Inactive before UP ↑ or DOWN ↑		6	10	15	
		$\overline{LOAD}$ Inactive before UP ↑ or DOWN ↑		6	10	15	
t_h	Minimum Hold Time	Data after $\overline{LOAD}$ ↑		0	0	0	ns
		UP High after DOWN ↑		0	0	0	
		DOWN High after UP ↑		0	0	0	
C_{IN}	Maximum Input Capacitance			5			pF
C_{PD}	Power Dissipation Capacitance*			80			pF

*C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
†For AC switching test circuits and timing waveforms see section 2.