TOSHIBA

# TMPR3907F 32-bit MIPS® RISC Microprocessor

## Description

The TMPR3907F is a 32-bit MIPS RISC microprocessor of the TX39 family. The TMPR3907F uses the TX39/H Processor Core as the CPU, which is a RISC CPU core Toshiba developed based on the MIPS® R3000A architecture. The TMPR3907F has built-in peripheral circuits such as a PCI Bus Controller, DRAM and ROM Memory Controllers, Serial Communication Ports, and Timer/Counter implementations.

The TX39/H core and added PCI Bus Controller features of this chip allow it to achieve high performance system interfacing.

## Microprocessor Features

- Built–in TX39 Processor Core
  - Developed based on the R3000A architecture
  - Instruction cache 4KB and Data cache 1KB
  - Built-in Debug Support Unit (DSU)
  - Five-stage pipeline: Fetch, Decode, Execute, Memory access, and Register write
  - Incorporates single cycle DSP function Multiply-Accumulate (MAC)
- Power Supply: $V_{DD}$ = 3.3V ± 0.3V
- Maximum Operating Frequency: 66MHz
- Package: 208 pin plastic QFP

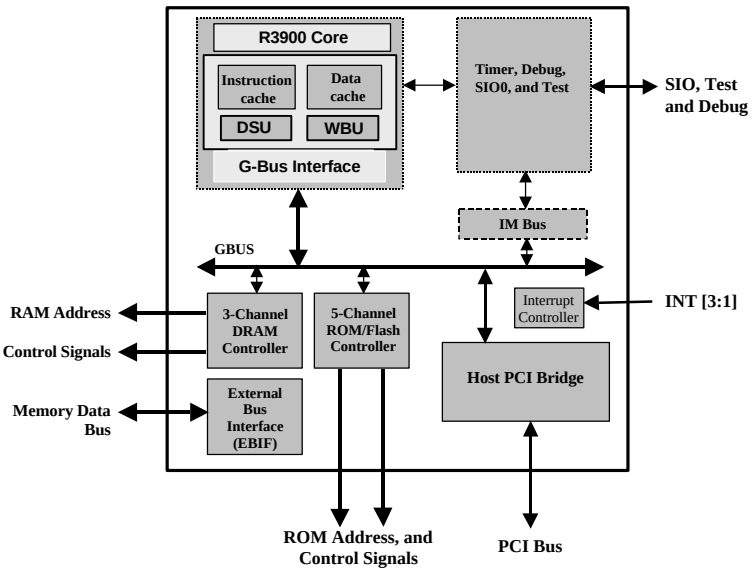


**Figure 1. TMPR3907F Block Diagram**

## Peripheral Features

- DRAM Controller
  - Supports 3 channels of DRAM memories
  - Each channel supports two banks of memory
  - Independent memory size and timing set-up for each channel
  - Support of 32/16-bit static bus sizing
  - Supports both fast and hyper page EDO modes
- ROM Controller
  - Supports 5 channels of ROM controller with a single chip select per channel
  - Supports simple-page-mode and interleaved-page-mode ROM
  - Supports various memory size of 1M/2M/4M/8M/16Mbyte per channel
  - Supports 32/16-bit static bus sizing and fast page read mode
  - Supports Mask ROM, EPROM, $E^2$PROM, SRAM, and Flash Memory
  - Supports 2-way interleaved ROM attachment on Channel 0
- Timer/Counter
  - 3-channel 24-bit up-counter
  - Interval and Watchdog timer modes
- Serial I/O Ports
  - One-channel UART
  - Baud rate generator and modem flow control
- Interrupt Controller
  - Priority process of 8 interrupt sources
  - Non-maskable Interrupt (NMI)
- PCI Controller
  - Full compliance with PCI Local Bus Specification Rev. 2.1
  - 32-bit PCI interface at 33MHz
  - Supports both target and initiator mode
  - Supports zero-wait-state read and write burst transfer for target and initiator
  - FIFO to minimize initial latency requirements to and from memory controller
  - Supports PIO mode transfer between local bus and PCI Core
  - Supports auto PCI bus to local bus address space mapping

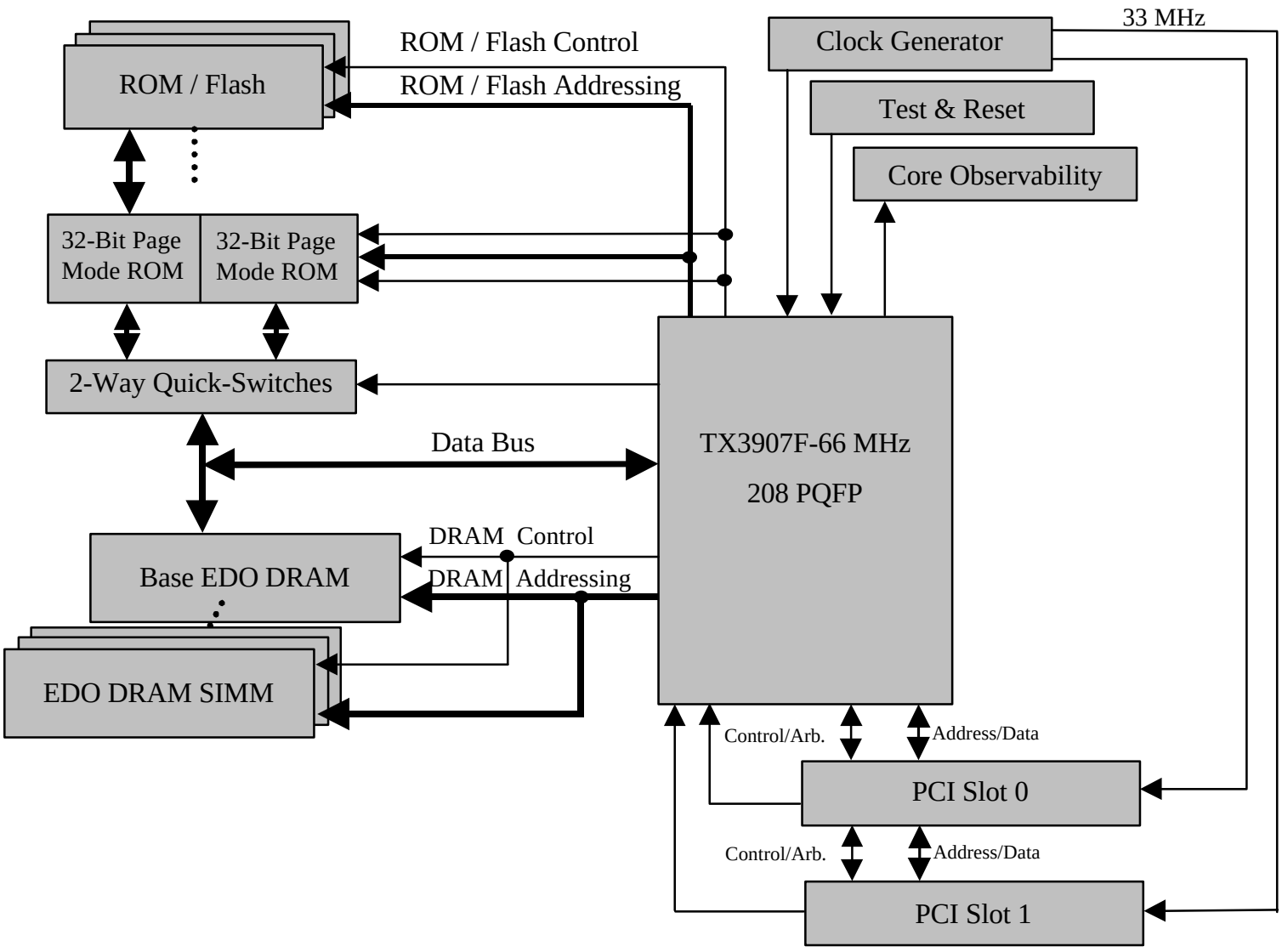


**Figure 2. Typical System Block Diagram**

**Table 1. Pin Assignment**

| Pin No. | Signal | Pin No. | Signal | Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|---|---|---|---|
| 1 | INT[1] | 29 | ROMAD[7] | 57 | D[17] | 85 | VDD |
| 2 | INT[0] | 30 | ROMAD[8] | 58 | D[25] | 86 | VSS |
| 3 | GNT_N[2] | 31 | ROMAD[9] | 59 | D[18] | 87 | DRAMA[7] |
| 4 | GNT_N[1] | 32 | OE* | 60 | VSS | 88 | DRAMA[11] |
| 5 | GNT_N[0] | 33 | SYSCLK | 61 | VDD | 89 | DRAMA[8] |
| 6 | ROMAD[23] | 34 | ACK* | 62 | VSS | 90 | DRAMA[9] |
| 7 | ROMAD[22] | 35 | LAST*/RD* | 63 | D[26] | 91 | DRAMA[12] |
| 8 | SCS[1]*/CE[4]* | 36 | VDD | 64 | D[19] | 92 | RAS0[0]* |
| 9 | VDD | 37 | VSS | 65 | D[27] | 93 | RAS0[1]* |
| 10 | VDD | 38 | VSS | 66 | DRAMA[0] | 94 | RAS1[0]* |
| 11 | VSS | 39 | ROMAD[10] | 67 | DRAMA[1] | 95 | RAS1[1]* |
| 12 | SCS[0]*/CE[3]* | 40 | ROMAD[11] | 68 | DRAMA[2] | 96 | VSS |
| 13 | CE[2]* | 41 | ROMAD[12] | 69 | DRAMA[3] | 97 | VDD |
| 14 | CE[1]* | 42 | ROMAD[13] | 70 | DRAMA[4] | 98 | RAS2[0]* |
| 15 | VSS | 43 | VDD | 71 | DRAMA[5] | 99 | RAS2[1]* |
| 16 | CE[0]* | 44 | ROMAD[14] | 72 | VSS | 100 | CAS[0]*/BE[0]* |
| 17 | SWE* | 45 | ROMAD[15] | 73 | VSS | 101 | CAS[1]*/BE[1]* |
| 18 | R/W* | 46 | ROMAD[16] | 74 | VDD | 102 | CAS[3]*/BE[3]* |
| 19 | SPADD[0] | 47 | ROMAD[17] | 75 | DRAMA[6] | 103 | CAS[2]*/BE[2]* |
| 20 | SPADD[1] | 48 | ROMAD[18] | 76 | DRAMA[10] | 104 | WE* |
| 21 | ROMAD[2] | 49 | ROMAD[19] | 77 | D[20] | 105 | D[0] |
| 22 | ROMAD[3] | 50 | VSS | 78 | D[28] | 106 | D[8] |
| 23 | ROMAD[4] | 51 | ROMAD[20] | 79 | D[21] | 107 | PLLOFF* |
| 24 | ROMAD[5] | 52 | ROMAD[21] | 80 | D[29] | 108 | PLL_VSS |
| 25 | VDD | 53 | ENLEAFA* | 81 | D[22] | 109 | VSS |
| 26 | VSS | 54 | ENLEAFB* | 82 | D[30] | 110 | XIN |
| 27 | VSS | 55 | D[16] | 83 | D[23] | 111 | XOUT |
| 28 | ROMAD[6] | 56 | D[24] | 84 | D[31] | 112 | VDD |

*Active-low signal

**Table 1. Pin Assignment (Continued)**

| Pin No. | Signal | Pin No. | Signal | Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|---|---|---|---|
| 113 | PLL_VDD | 137 | SDI* | 161 | PCIAD[11] | 185 | PCIAD[18] |
| 114 | VDD | 138 | DBGE* | 162 | PCIAD[12] | 186 | PCIAD[19] |
| 115 | D[1] | 139 | PCST[2] | 163 | PCIAD[13] | 187 | PCIAD[20] |
| 116 | D[9] | 140 | PCST[1] | 164 | VSS | 188 | PCIAD[21] |
| 117 | D[2] | 141 | PCST[0] | 165 | VDD | 189 | PCIAD[22] |
| 118 | D[10] | 142 | VSS | 166 | PCIAD[14] | 190 | PCIAD[23] |
| 119 | VSS | 143 | GDCLK | 167 | PCIAD[15] | 191 | ID_SEL |
| 120 | D[3] | 144 | PCI_CLK | 168 | C_BE[1] | 192 | VSS |
| 121 | D[11] | 145 | PCIAD[0] | 169 | PAR | 193 | C_BE[3] |
| 122 | D[4] | 146 | PCIAD[1] | 170 | SERR_N | 194 | PCIAD[24] |
| 123 | D[12] | 147 | VDD | 171 | PERR_N | 195 | PCIAD[25] |
| 124 | D[13] | 148 | PCIAD[2] | 172 | STOP_N | 196 | PCIAD[26] |
| 125 | D[5] | 149 | PCIAD[3] | 173 | VSS | 197 | PCIAD[27] |
| 126 | D[14] | 150 | PCIAD[4] | 174 | DEVSEL_N | 198 | PCIAD[28] |
| 127 | D[6] | 151 | PCIAD[5] | 175 | TRDY_N | 199 | PCIAD[29] |
| 128 | D[15] | 152 | PCIAD[6] | 176 | IRDY_N | 200 | VSS |
| 129 | D[7] | 153 | PCIAD[7] | 177 | FRAME_N | 201 | VDD |
| 130 | VSS | 154 | VDD | 178 | C_BE[2] | 202 | VSS |
| 131 | VSS | 155 | VSS | 179 | PCIAD[16] | 203 | PCIAD[30] |
| 132 | RESET* | 156 | VSS | 180 | PCIAD[17] | 204 | PCIAD[31] |
| 133 | TEST* | 157 | C_BE[0] | 181 | VDD | 205 | REQ_N[2] |
| 134 | NMI* | 158 | PCIAD[8] | 182 | VSS | 206 | REQ_N[1] |
| 135 | DSA0 | 159 | PCIAD[9] | 183 | VSS | 207 | REQ_N[0] |
| 136 | DRESET* | 160 | PCIAD[10] | 184 | VDD | 208 | INT[2] |

*Active-low signal



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