

**Silicon diffused power transistors****BU508AF; BU508DF**

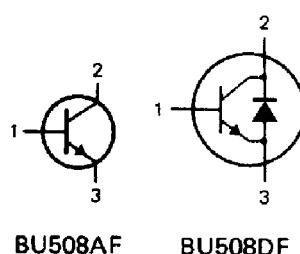
High-voltage, high-speed switching npn transistors in a fully isolated SOT199 envelope (with integrated efficiency diode for the BU508DF), primarily intended for use in horizontal deflection circuits of colour television receivers.

**QUICK REFERENCE DATA**

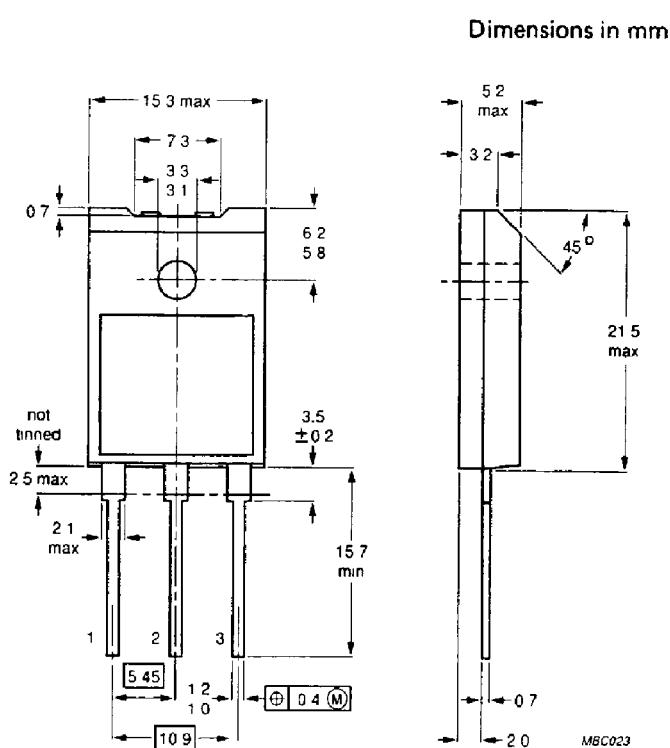
Collector-emitter voltage peak value; $V_{BE} = 0$ open base	$V_{CESM}$	max.	1500 V
	$V_{CEO}$	max.	700 V
Collector saturation current	$I_{Csat}$	max.	4,5 A
Collector current (DC)	$I_C$	max.	8 A
Collector current (peak value)	$I_{CM}$	max.	15 A
Total power dissipation up to $T_h = 25^\circ\text{C}$	$P_{tot}$	max.	34 W
Collector-emitter saturation voltage	$V_{CEsat}$	max.	1 V
Diode forward voltage $I_F = 4,5 \text{ A (BU508DF)}$	$V_F$	typ.	1,6 V
Fall time	$t_f$	typ.	0,7 $\mu\text{s}$

**MECHANICAL DATA**

Fig. 1 SOT199.



- 1 = base
- 2 = collector
- 3 = emitter
- Mounting base is electrically isolated from all terminals.



■ 7110826 0077474 140 ■

December 1991

69

## Silicon diffused power transistors

## BU508AF; BU508DF

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

## Collector-emitter voltage

peak value; $V_{BE} = 0$	$V_{CESM}$	max.	1500 V
open base	$V_{CEO}$	max.	700 V

## Collector current

DC	$I_C$	max.	8 A
peak value	$I_{CM}$	max.	15 A
saturation	$I_{Csat}$	max.	4,5 A

## Base current

DC	$I_B$	max.	4 A
peak value	$I_{BM}$	max.	6 A

## Total power dissipation

up to $T_h = 25^\circ\text{C}^*$	$P_{tot}$	max.	34 W
----------------------------------	-----------	------	------

## Storage temperature

## Junction temperature

 $T_{stg}$  $T_j$ max.  $150^\circ\text{C}$ max.  $150^\circ\text{C}$ **THERMAL RESISTANCE**

From junction to mounting base	$R_{thj-mb}$	=	1 K/W
From junction to external heatsink *	$R_{thj-h}$	=	3,7 K/W
From junction to external heatsink **	$R_{thj-h}$	=	2,8 K/W
From junction to ambient	$R_{thj-a}$	=	35 K/W

**ISOLATION**

Isolation voltage from all terminals to external heatsink (peak value)	$V_{isol}$	max.	1500 V
---	------------	------	--------

Isolation capacitance from collector to external heatsink	$C_{isol}$	typ.	21 pF
--	------------	------	-------

**CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

## Collector cut-off current

$V_{CE} = V_{CESmax}; V_{BE} = 0$	$I_{CES}$	max.	1 mA
$V_{CE} = V_{CESmax}; V_{BE} = 0; T_j = 125^\circ\text{C}$	$I_{CES}$	max.	2 mA

## Emitter cut-off current

$V_{EB} = 6 \text{ V}; I_C = 0$	$I_{EBO}$	max.	10 mA
---------------------------------	-----------	------	-------

## DC current gain

$I_C = 100 \text{ mA}; V_{CE} = 5 \text{ V}$	$h_{FE}$	min.	6
	$h_{FE}$	typ.	13
	$h_{FE}$	max.	30

\* Mounted without heatsink compound and  $30 \pm 5$  newtons pressure on centre of envelope.\*\* Mounted with heatsink compound and  $30 \pm 5$  newtons pressure on centre of envelope.

7110826 0077475 087

December 1991

70

## Silicon diffused power transistors

BU508AF; BU508DF

## Saturation voltages

$$I_C = I_{C\text{sat}}; I_B = 2 \text{ A}$$

$V_{CE\text{sat}}$	max.	1 V
$V_{BE\text{sat}}$	max.	1,3 V

## Diode forward voltage

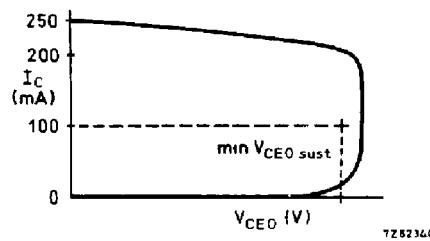
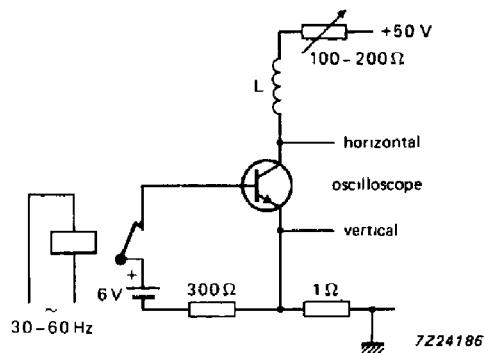
$$I_F = 4,5 \text{ A (BU508DF)}$$

$V_F$	max.	2 V
$V_F$	typ.	1,6 V

## Collector-emitter sustaining voltage

$$I_C = 0,1 \text{ A}; I_B = 0; L = 25 \text{ mH}$$

$V_{CEO\text{sus}}$	min.	700 V
---------------------	------	-------

Fig. 2 Oscilloscope display for  $V_{CEO\text{sus}}$ .Fig. 3 Test circuit for  $V_{CEO\text{sus}}$ .

## Second-breakdown current

$$V_{CE} = 120 \text{ V}; T = 200 \mu\text{s}$$

$I_{SB}$	min.	11 A
----------	------	------

Transition frequency at  $f = 5 \text{ MHz}$ 

$$I_C = 0,1 \text{ A}; V_{CE} = 5 \text{ V}$$

$f_T$	typ.	7 MHz
-------	------	-------

Collector capacitance at  $f = 1 \text{ MHz}$ 

$$I_E = i_e = 0; V_{CB} = 10 \text{ V}$$

$C_C$	typ.	125 pF
-------	------	--------

## Switching times in horizontal deflection circuit

$$-V_{IM} = 4 \text{ V}; L_B = 6 \mu\text{H}$$

$$I_C = I_{C\text{sat}}; I_B(\text{end}) = 1,4 \text{ A}$$

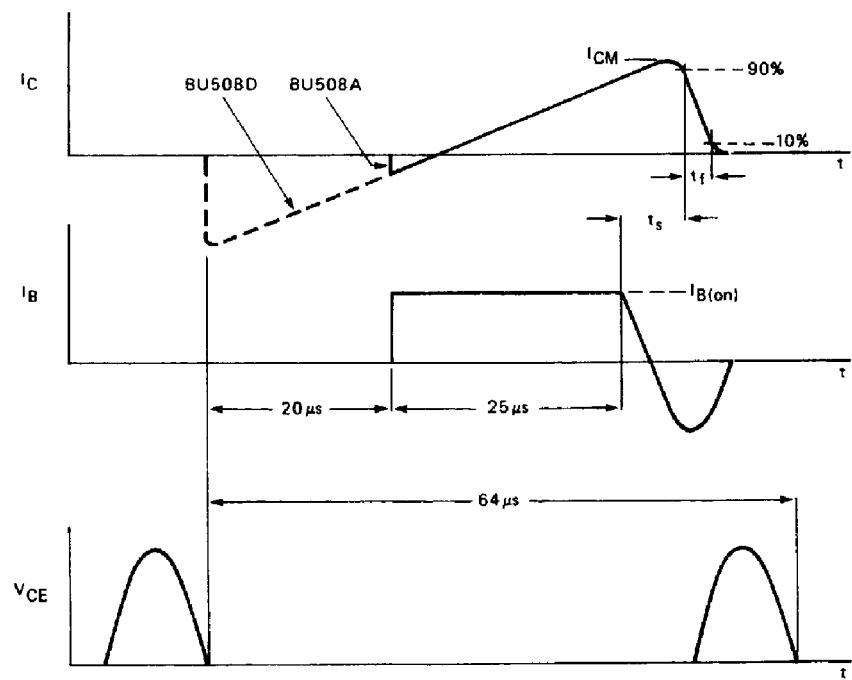
$$(-dI_B/dt = 0,6 \text{ A}/\mu\text{s})$$

$t_f$	typ.	0,7 $\mu\text{s}$
$t_s$	typ.	6,5 $\mu\text{s}$

■ 7110826 0077476 T13 ■

## Silicon diffused power transistors

BU508AF; BU508DF



7224366

Fig. 4 Switching times waveforms.

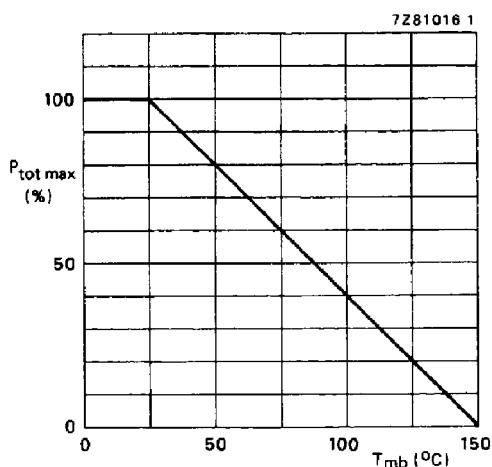


Fig. 5 Power derating curve.

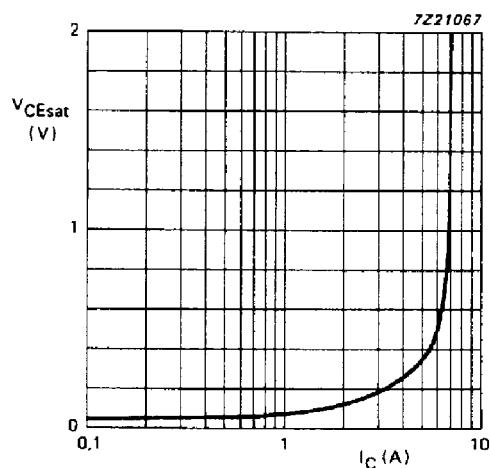
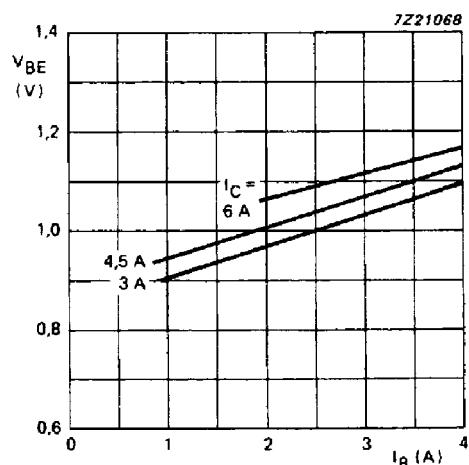
■ 7110826 0077477 95T ■

December 1991

72

## Silicon diffused power transistors

BU508AF; BU508DF

Fig. 6 Typical values  $I_C/I_B = 2$ ;  $T_j = 25$  °C.Fig. 7 Typical values base-emitter voltage at  $T_j = 25$  °C.

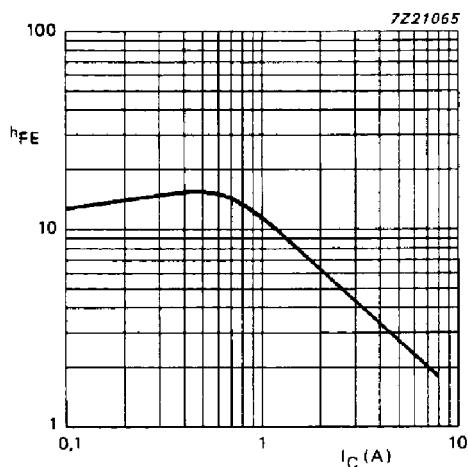
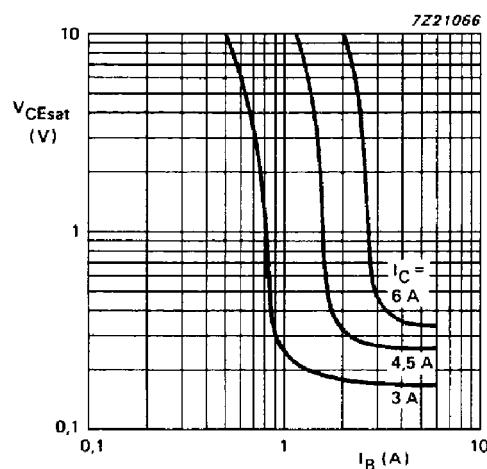
■ 7110826 0077478 896 ■

December 1991

73

## Silicon diffused power transistors

BU508AF; BU508DF

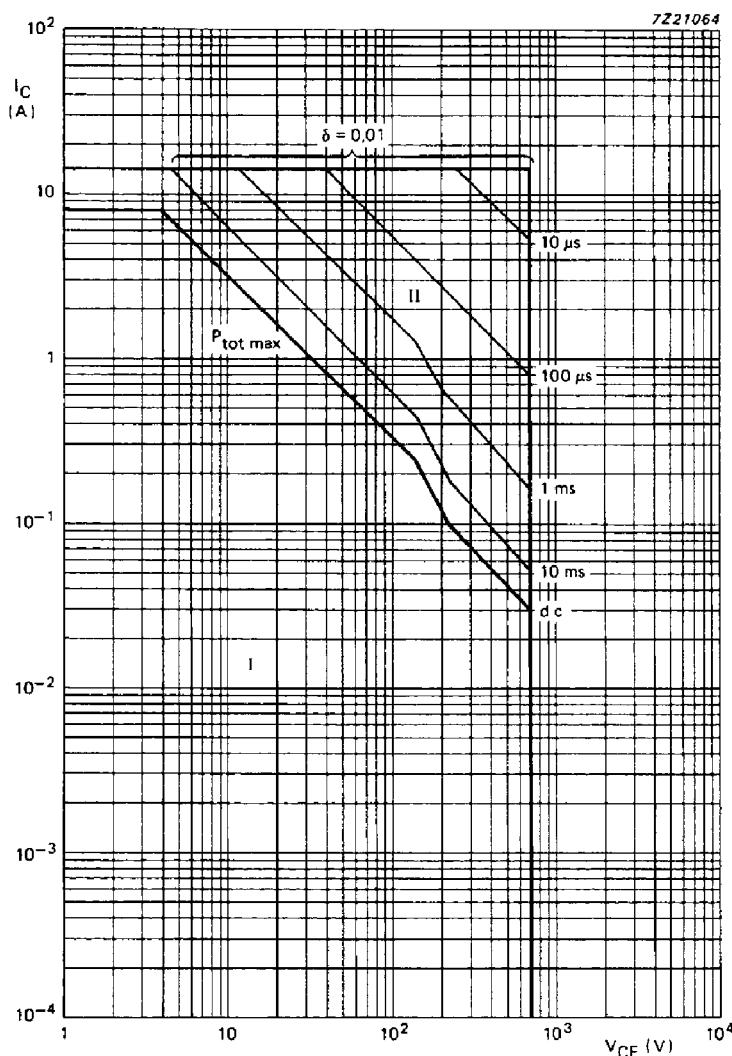
Fig. 8 Typical values DC current gain at  $V_{CE} = 5$  V;  $T_j = 25$  °C.Fig. 9 Typical values collector-emitter voltage at  $T_j = 25$  °C.

■ 7110826 0077479 722 ■

December 1991

## Silicon diffused power transistors

BU508AF; BU508DF



- I      Region of permissible DC operation.
  - II     Permissible extension for repetitive pulse operation.
- Note: Mounted without heatsink compound and  $30 \pm 5$  newtons pressure on the centre of the envelope.

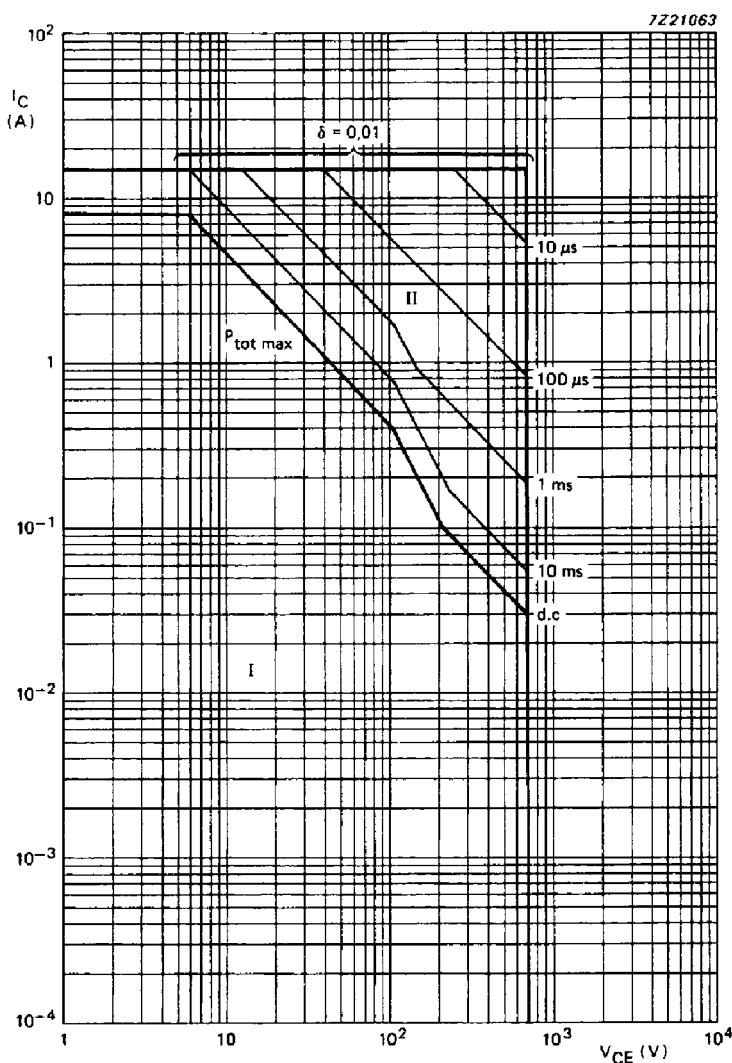
Fig. 10 Safe Operating Area;  $T_h = 25^\circ\text{C}$ .

■ 7110826 0077480 444 ■

December 1991

## Silicon diffused power transistors

BU508AF; BU508DF



I      Region of permissible DC operation.

II      Permissible extension for repetitive pulse operation.

Note: Mounted with heatsink compound and  $30 \pm 5$  newtons pressure on the centre of the envelope.

Fig. 11 Safe Operating Area;  $T_h = 25^\circ\text{C}$ .

■ 7110826 0077481 380 ■

December 1991

76