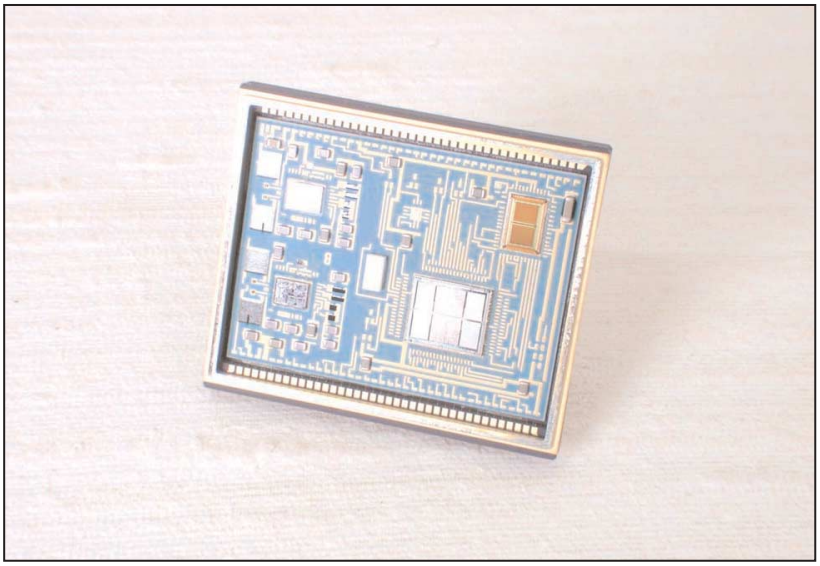
BU-61559 SERIES

MIL-STD-1553B NOTICE 2 AIM-HY'ER



DESCRIPTION

DDC's BU-61559 series of Advanced Integrated Mux Hybrids with enhanced RT Features (AIM-HY'er) comprise a complete interface between a microprocessor and a MIL-STD-1553B Notice 2 bus, implementing Bus Controller (BC), Remote Terminal (RT), and Monitor Terminal (MT) modes. Packaged in a single 78-pin DIP or flat package, the BU-61559 series contains dual low-power transceivers and encoder/decoders, complete BC/RT/MT protocol logic, memory management and interrupt logic, 8K x 16 of shared static RAM, and a direct, buffered interface to a host processor bus.

The BU-61559 includes a number of advanced features that support MIL-STD-1553B Notice 2 and STANAG 3838. Other salient features of the BU-61559 serve to provide the benefits of reduced board space requirements, enhanced software flexibility, and reduced host processor overhead.

The BU-61559 contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. Alternatively, the buffers may be operated in a fully transparent mode in order to interface to up to 64K words of external shared RAM and/or connect directly to a component set supporting the 20 MHz STANAG 3910 bus.

The memory management scheme for RT mode provides an option for separation of broadcast data, in compliance with 1553B Notice 2. A circular buffer option for RT message data blocks offloads the host processor for bulk data transfer applications.

The BU-61559 series hybrids operate over the full military temperature range of -55 to +125°C and MIL-PRF-38534 processing is available. The hybrids are ideal for demanding military and industrial microprocessor-to-1553 applications.

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FEATURES

- Complete Integrated 1553B Notice 2 Interface Terminal
- Direct Replacement for BUS-61559 AIM-HY'er Series
- Functional Superset of BUS-61553 AIM-HY Series
- Internal Address and Data Buffers for Direct Interface to Processor Bus
- RT Subaddress Circular Buffers to Support Bulk Data Transfers
- Optional Separation of RT Broadcast Data
- Internal Interrupt Status and Time Tag Registers
- Internal Command Illegalization
- MIL-PRF-38534 Processing Available
- Transmitter Inhibit Control for Individual Bus Channels

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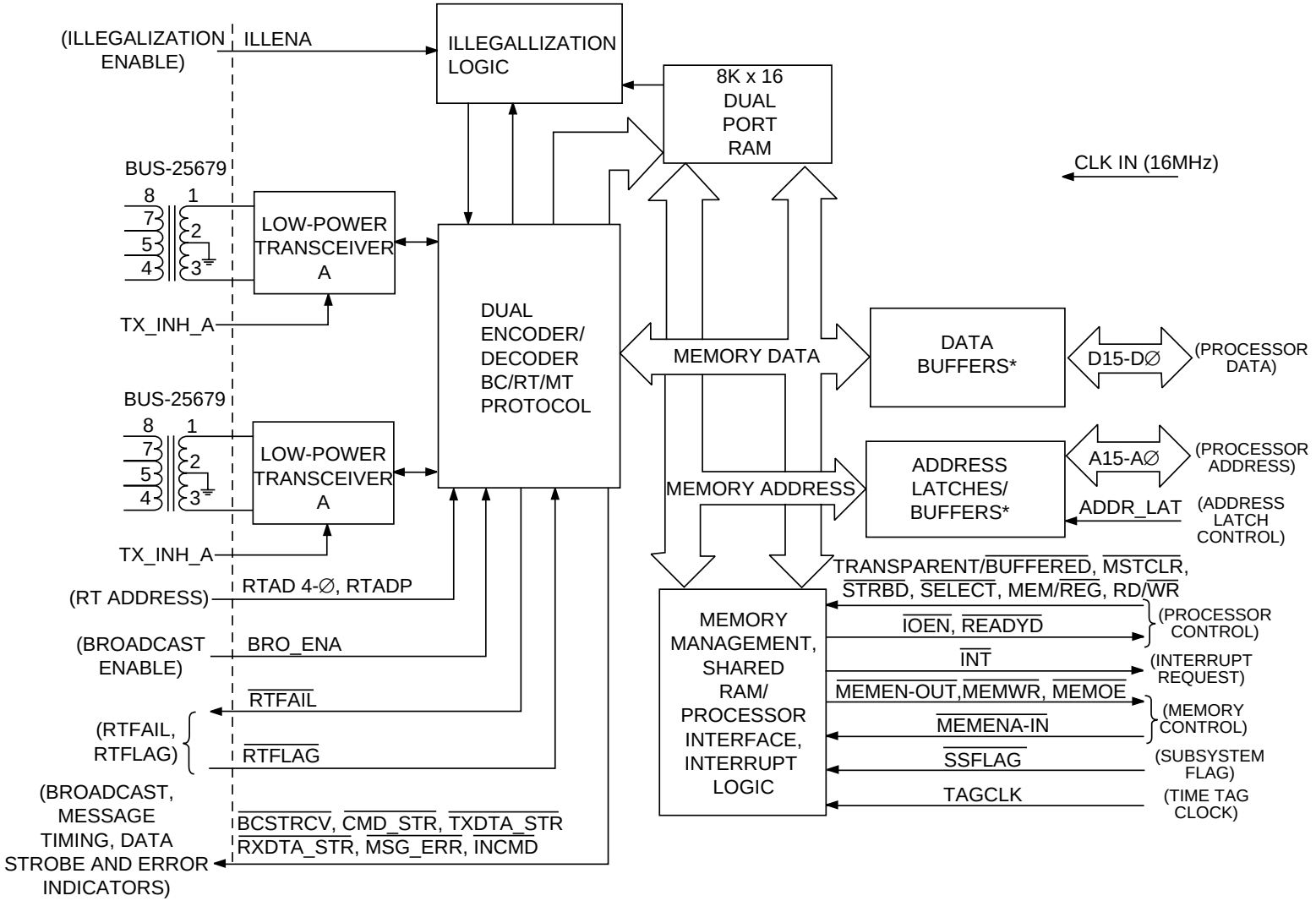


FIGURE 1. BU-61559 BLOCK DIAGRAM

TABLE 1. BU-61559 SPECIFICATIONS

PARAMETER	UNITS	VALUE
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage		
• Logic +5V	V	-0.5 to 7.0
• Transceiver +5V	V	-0.5 to 7.0
• -15V (BU-61559X1)	V	+0.3 to -18.0
• -12V (BU-61559X2)	V	+0.3 to -18.0
Receiver Differential Voltage	Vp-p	40 max
Logic		
• Voltage Input Range	V	-0.5 to 7.0
RECEIVER		
Differential Input Voltage	Vp-p	40 max
Differential Input Resistance (see notes 1-6)	k Ohms	11 min
Differential Input Capacitance (see notes 1-6)	pF	10 max
Threshold Voltage, Transformer coupled, measured on stub	Vp-p	0.70 min, 0.86 max
CMRR		
• (BU-61559X1, through BUS-25679 transformer at 1MHz)	dB	50 min
• (BU-61559X2, through BUS-29854 transformer at 1MHz)	dB	50 min
TRANSMITTER		
Differential Output Voltage		
• Direct coupled across 35 Ohms, measured on bus	Vp-p	6 min., 9 max
• Transformer coupled, measured on stub (for 20 Vp-p min. stub voltage, consult factory)	Vp-p	18 min, 20 typ, 27 max
For -601 Reliability Grade (note 7)	Vp-p	20 min, 21 typ, 27 max
Output noise, differential (direct coupled)	mVp-p, diff	10 max.
Output offset Voltage, direct coupled across 35 Ohms	V	±90 max
Rise/Fall time	ns	100 min, 150 typ, 300 max
LOGIC		
Vih	V	2.0 min
Vil	V	0.8 max
Iih (Vcc = 5.5V, Vih = 2.7V)		
• D15 through D0, A15 through A0, MEM/REG, STRBD, RD/WR, MSTCLR, SELECT, TX_INH_A, TX_INH_B, SSFLAG, TRANSPARENT/BUFFERED, ADDR_LAT, TAGCLK RTAD4 through RTAD0, RTADP BRO_ENA, RTFLAG, ILLENA MEMENA-IN, CLK_IN	µA	-346 min, -42 max
Iil (Vcc = 5.5V, Vil = 0.4V)		
• D15 through D0, A15 through A0, MEM/REG, STRBD, RD/WR, MSTCLR, SELECT, TX_INH_A, TX_INH_B, SSFLAG, TRANSPARENT/BUFFERED, ADDR_LAT, TAGCLK RTAD4 through RTAD0, RTADP BRO_ENA, RTFLAG, ILLENA MEMENA-IN, CLK_IN	µA	-397 min, -50 max

TABLE 1. BU-61559 SPECIFICATIONS (CONT)

PARAMETER	UNITS	VALUE
LOGIC (CONT)		
Voh (Vcc=4.5V, Vih=2.7V, Vil=0.4V)		
• (Ioh=-6.8 mA) D15 through D0, A15 through A0	V	3.7 min
• (Ioh=-3.4 mA) MEMOE, MEMENA-OUT, MEMWR, INT, IOEN, READYD	V	3.7 min
• (Ioh=-0.4 mA) RTFAIL, INCMD, BCSTRCV, MSG_ERR, CMD_STR, TXDTA_STR, RXDTA_STR	V	2.4 min
VoL (Vcc=4.5V, Vih=2.7V, Vil=0.4V)		
• (Iol=-6.8 mA) D15 through D0, A15 through A0	V	0.4 max
• (Iol=2.0 mA) RTFAIL, INCMD, BCSTRCV, MSG_ERR, CMD_STR	V	0.4 max
• (Iol=3.4 mA) MEMOE, MEMENA-OUT, MEMWR, INT, IOEN, READYD	V	0.4 max
• (Iol=4.0 mA) TXDTA_STR, RXDTA_STR	V	0.4 max
Ci (f=1 MHz)	pF	50 max
Co (f=1 MHz)	pF	10 max
Cio (f=1 MHz) D15 through D0, A15 through A0	pF	50 max
POWER SUPPLY REQUIREMENTS		(see note 7)
Voltages/Tolerances		
• +5V (Logic)	V	4.5 min, 5.5 max
• +5V (Ch A, Ch B)	V	4.5 min, 5.5 max
• -15V (BU-61559X1)	V	-15.75 min, -14.25 max
• -12V (BU-61559X2)	V	-12.6 min, -11.4 max
Current Drain		
• +5V	mA	85 typ, 170 max
• -15V (BU-61559X1)		
Idle	mA	5 min, 40 typ, 80 max
25% Duty Cycle	mA	25 min, 80 typ, 130 max
50% Duty Cycle	mA	45 min, 120 typ, 180 max
100% Duty Cycle	mA	85 min, 200 typ, 280 max
• -12V (BU-61559X2)		
Idle	mA	5 min, 40 typ, 80 max
25% Duty Cycle	mA	25 min, 90 typ, 135 max
50% Duty Cycle	mA	45 min, 135 typ, 185 max
100% Duty Cycle	mA	85 min, 230 typ, 305 max
POWER DISSIPATION		(see note 7)
Total Hybrid		
• BU-61559X1		
Idle	W	1.025 typ, 2.050 max
25% Duty Cycle	W	1.325 typ, 2.500 max
50% Duty Cycle	W	1.625 typ, 2.950 max
100% Duty Cycle	W	2.225 typ, 3.850 max
• BU-61559X2		
Idle	W	0.905 typ, 1.810 max
25% Duty Cycle	W	1.025 typ, 2.170 max
50% Duty Cycle	W	1.445 typ, 2.470 max
100% Duty Cycle	W	1.985 typ, 3.310 max

TABLE 1. BU-61559 SPECIFICATIONS (CONT)

PARAMETER	UNITS	VALUE
POWER DISSIPATION (CONT)		
Hottest Die		
• BU-61559X1		
Idle	W	0.45 typ, 0.68 max
25% Duty Cycle	W	0.65 typ, 1.06 max
50% Duty Cycle	W	0.875 typ, 1.45 max
100% Duty Cycle	W	1.30 typ, 2.23 max
• BU-61559X2		
Idle	W	0.39 typ, 0.59 max
25% Duty Cycle	W	0.60 typ, 0.98 max
50% Duty Cycle	W	0.81 typ, 1.36 max
100% Duty Cycle	W	1.30 typ, 2.16 max
CLOCK INPUT		
Frequency		
• Nominal Value	MHz	16.0
• Long Term Tolerance	%	±0.1
• Short Term Tolerance, 1 second	%	±0.01
• Duty Cycle	%	33 min, 67 max
1553 MESSAGE TIMING		
Completion of CPU Write (BC Start)-to Start of first BC Message	µS	5.85 min, 7.21 max
BC Intermessage Gap	µS	13.98 min, 17.82max.
BC Response Timeout	µS	17.5 min, 19.0 typ, 22.5 max
RT Response Time	µS	9.8 min, 10.9 typ, 11.7 max
Rt-to RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status)	µS	18.0 min, 18.75 typ, 19.5 max
Transmitter Watchdog Timeout	µS	768 typ
THERMAL		
Thermal Resistance, Junction-to-case, Hottest Die (θ_{JC})	°C/W	6.13
Thermal Resistance, Case-to-ambient, Hottest Die (θ_{CA})	°C/W	10.5
Operating Junction Temperature	°C	-55 to +160
Operating Case Temperature		
• -B, -M	°C	-55 to +125
• -(blank)	°C	0 to +70
Storage Temperature	°C	-65 to +150
Lead Temperature (soldering, 10 seconds)	°C	+300
PHYSICAL CHARACTERISTICS		
Size		
• 78-pin Ceramic QIP	in. (mm.)	1.80 x 2.10 x 0.21 (45.7 x 53.3 x 5.3)
• 78-pin Ceramic Flat Pack	in. (mm.)	1.80 x 2.10 x 0.21 (45.7 x 53.3 x 5.3)
• Weight	oz. (g)	1.7 (48.2)

Notes: The following notes are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:

(1) Specifications include both transmitter and receiver (tied together internally).
(2) Impedance parameters are specified directly between pins TX/RX A(B) and $\overline{TX/RX}$ A(B) of the BU-61559 hybrid.
(3) It is assumed that all power and ground inputs to the hybrid are connected and that the hybrid case is connected to ground for the impedance measurement.
(4) The specifications are applicable for both unpowered and powered conditions.
(5) The specifications assume a 2 Vrms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.
(6) Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.
(7) -601 Power Supply Requirements and Power Dissipation values will be higher.

FUNCTIONAL OVERVIEW

GENERAL (REFERENCE BLOCK DIAGRAM FIGURE 1)

The BU-61559 Advanced Integrated Multiplex Hybrid with enhanced RT features (AIM-HY'er) comprises a complete interface between a host microprocessor bus and a dual redundant MIL-STD-1553B Notice 2 bus. The hybrids are comprised of dual low-power transceivers and encoder/decoders, full BC/RT/MT protocol, memory management logic, 8K words of internal shared RAM, and a direct, internally buffered processor interface. The BU-61559 is packaged in a four square inch hybrid package and is available in both plug-in and surface mountable (flatpack) packages.

TRANSCEIVERS

The transceiver front end of the BU-61559 AIM-HY'er hybrids is implemented by means of low-power bipolar analog monolithic and thick-film hybrid technology. The transceiver requires +5 V and -15V or -12V only (no +15 V or +12V is required) and include voltage source transmitters. The voltage source transmitters provide superior line driving capability for long cables and heavy amounts of bus loading. In addition, the monolithic transceivers may be modified to provide a minimum stub voltage of 20Vp-p, as required for MIL-STD-1760 applications. Consult the factory for additional information.

The receiver sections of the BU-61559 are fully compliant with MIL-STD-1553B in terms of front end overvoltage protection, threshold, common mode rejection, and word error rate. In addition, the receiver filters have been designed for optimal operation with the BU-61559's 16 MHz Manchester II decoders.

MIL-STD-1553 PROTOCOL

The 1553 protocol section of the BU-61559 includes dual encoder/decoders and complete registers, word count, timing, and sequencing logic for Bus Controller (BC), Remote Terminal (RT), and Monitor Terminal (MT) modes. The dual Manchester II decoders utilize a 16 MHz sampling clock, providing superior performance in terms of word error rate and tolerance to zero-crossing distortion. The encoder section of the protocol logic includes a transmitter watchdog timer. The watchdog timer monitors the digital encoder outputs and serves to inhibit the transmitters after a period of 768 µs.

The BC protocol supports all MIL-STD-1553B formats, complete error detection, and multi-message frames of up to 64 unique messages.

Protocol for RT mode supports all message formats and dual redundant 1553B mode codes. The BU-61559 has passed the RT Validation Test Plan at SEAFAC; this test encompasses the dual transceiver and all of the RT protocol logic.

The Monitor (MT) protocol of the BU-61559 monitors both 1553 buses. For each word received from either bus, both the 16 bits of word data plus a 16-bit Identification Word (“Tag” Word) are stored in the AIM-HY'er memory space.

ADVANCED FEATURES

While maintaining functional and software compatibility to the previous generation BUS-61553 series AIM-HY hybrids, the BU-61559 incorporates a number of advanced features to support 1553B Notice 2. Other enhancements provided by the BU-61559 serve to provide the benefits of reduced board space requirements, expanded software flexibility, and reduced host processor overhead.

INTERNAL TRI-STATE BUFFERS

The BU-61559 contains internal address latches and bidirectional data buffers to provide a direct interface to either a multiplexed or a non-multiplexed processor bus. Alternatively, the latches and buffers may be operated in a fully transparent mode to interface to up to 64K words of external shared RAM and/or a component set supporting the STANAG 3910 20 MHz data bus.

MEMORY MANAGEMENT

The BU-61559 incorporates complete memory management and processor interface logic. The software interface to the host processor is implemented by means of eight internal registers plus a 64K word shared RAM address space, which generally includes the 8K words of internal RAM. For all three modes, a stack area of RAM is maintained. In BC mode, the stack allows for the scheduling of multi-message frames. For all three modes, the stack provides a real time chronology of all messages processed. In addition to the stack processing, the memory management logic performs storage, retrieval, and manipulation functions involving pointer and message data structures for all three modes.

The BU-61559 provides a number of programmable options for RT mode memory management. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, following error messages on a Tx/Rx/Bcst-subaddress basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary. In addition to interrupts for RT subaddress and circular buffer rollover conditions, the processor interface logic provides maskable interrupts and a 9-bit Interrupt Status Register for end of message, end of BC message list, erroneous messages, Status Set (BC mode), Time Tag Register Rollover, and RT Address Parity Error conditions. The Interrupt Status Register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

INTERNAL COMMAND ILLEGALIZATION

The BU-61559 implements internal command illegalization for RT mode. The internal illegalization eliminates the need for an external PROM, PLD, or RAM device. The illegalization architecture allows for any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. The BU-61559 illegalization scheme is under software control of the host processor. As a result, it is inherently self-testable.

INTERNAL TIME TAG

The BU-61559 includes an internal read/write Time Tag Register.

This register is a CPU read/write 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. The Time Tag Register may also be clocked from an external oscillator. Another option allows the Time Tag Register to be incremented under software control. This supports self-test for the Time Tag Register.

For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry (“TIME TAG WORD”) for both BC and RT modes.

Additional options are provided to clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command. Another option enables an interrupt request and a bit in the Interrupt Status Register to be set when the Time Tag Register rolls over from 0000 to FFFF. Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4-second time intervals for 64 µs/LSB resolution, down to 131 ms intervals for 2 µs/LSB resolution.

Another programmable option for RT mode is for the Service Request Status Word bit to be automatically cleared following the BU-61559's response to a Transmit Vector Word mode command.

INTERFACE TO STANAG 3910 20 MHZ FIBER OPTIC BUS

For applications requiring a higher rate of data transfer than MIL-STD-1553's 1 Mbps, it is possible to interface the BU-61559 directly to a component set supporting STANAG 3910. A STANAG 3910 bus operates as an adjunct to, and is controlled by, a MIL-STD-1553B Notice 2 (STANAG 3838) bus. The STANAG 3910 standard defines a Manchester II encoded serial data bus with a data rate of 20 Mbps, allowing for both electrical and fiber optic implementations. STANAG 3910 is intended for high-speed bulk data transfers, supporting message lengths of up to 4096 words.

CLOCK INPUT

The BU-61559 requires an external 16 MHz clock input. All internal timing is derived from this clock. Refer to FIGURE 1 for the short-term and long-term accuracy requirements of the input clock frequency.

INTERNAL REGISTERS, MEMORY MANAGEMENT, AND INTERRUPTS

The software interface of the BU-61559 to the host processor consists of eight internal registers plus 64K X 16 of shared memory address space. The BU-61559's 8K X 16 of internal RAM resides in this address space.

The address mapping and accessibility for the eight registers is defined as follows:

ADDRESS LINES			REGISTER
A2	A1	A0	DESCRIPTION/ACCESSIBILITY
0	0	0	Interrupt Mask Register (RD/WR)
0	0	1	Configuration Register # 1 (RD/WR)
0	1	0	Configuration Register # 2 (RD/WR)
0	1	1	Start/Reset Register (WR)
0	1	1	Stack Pointer Register (RD)
1	0	0	Subaddress Control Word Register (RD/WR)
1	0	1	Time Tag Register (RD/WR)
1	1	0	Interrupt Status Register (RD)
1	1	1	RESERVED

The Interrupt Mask Register is used to enable and disable interrupt requests for various conditions. Configuration Registers #1 and #2 are used to select the BU-61559's mode of operation as well as for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and other functions involving the Service Request Status bit, interrupts, and resolution and operation of the Time Tag Register.

The Start/Reset Register is used for “command” type functions, such as software reset and BC/MT Start as well as Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Stack Pointer Register allows the host CPU to determine the pointer location for the current or most recent message when the BU-61559 is in BC or RT modes.

The Subaddress Control Word Register allows the host processor access to the current or most recent Subaddress Control Word; the read/write accessibility of this register can be used to facilitate the testing of the BU-61559.

The 16-bit Time Tag Register maintains the value of a real time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Time Tag Register may also be clocked from an external oscillator. The current value of the Time Tag Register is written to the stack area of RAM during Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC and RT modes.

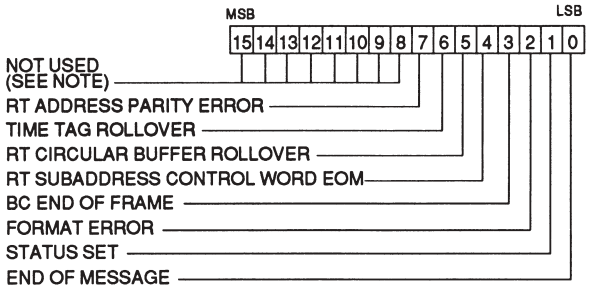
The Interrupt Status Register mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

The bit maps of the eight registers are defined in FIGURES 2 and 3.

BLOCK STATUS WORD

The Block Status Word is stored in the first location of the Message Block descriptor in the Stack area of the shared RAM for both BC and RT modes. It is updated by the 1553 memory management logic both at the beginning and at the end of the respective message. It contains information relating to whether the message is in progress or has been completed, what channel it was processed on, and whether or not there were any errors in the message.

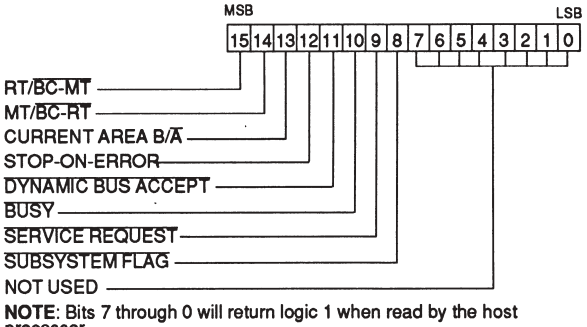
INTERRUPT MASK REGISTER
(Register Address 000; READ/WRITE)



NOTE: Bits 15 through 8 will return logic 1 when read by the host processor.

FIGURE 2. INTERRUPT MASK REGISTER

CONFIGURATION REGISTER #1
(Register Address 001; READ/WRITE)



NOTE: Bits 7 through 0 will return logic 1 when read by the host processor.

FIGURE 3. CONFIGURATION REGISTER #1

CONFIGURATION REGISTER #2
(Register Address 010; READ/WRITE)

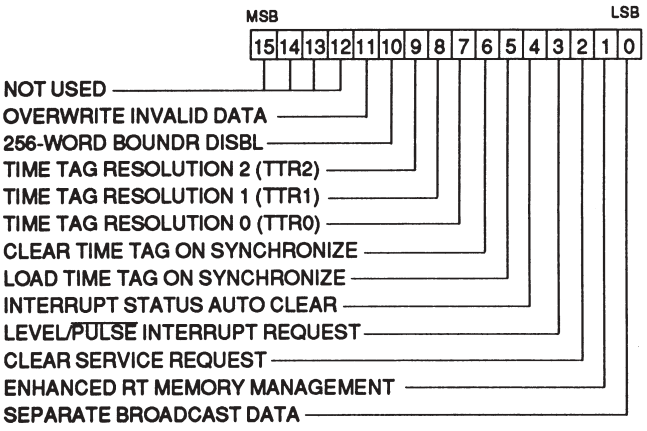
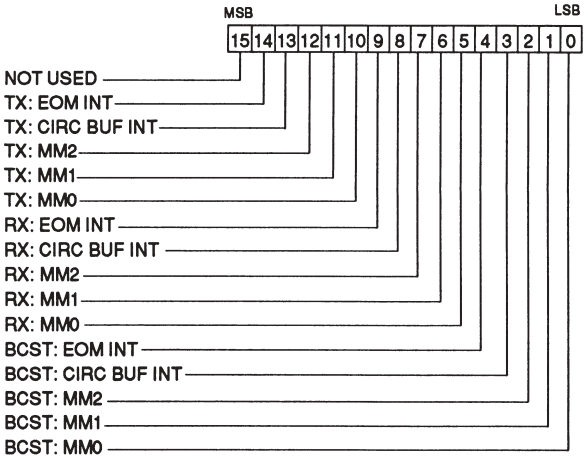


FIGURE 4. CONFIGURATION REGISTER #2

SUBADDRESS CONTROL WORD REGISTER *
(Register Address 100; Write Only)



* The BC Control Word/RT Subaddress Control Word Register cannot be written to when the BU-61559D1 is in RT mode, or during the time of a BC frame (following a BC Start command) in BC mode. The BU-61559D1's BC Control Word/RT Subaddress Control Word Register may be read at any time.

FIGURE 7. SUBADDRESS CONTROL WORD REGISTER

START/RESET REGISTER
(Register Address 011; WRITE ONLY)

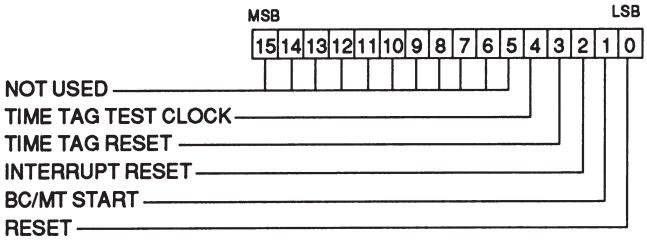


FIGURE 5. START/RESET REGISTER

TIME TAG REGISTER
(Register Address 101; READ/WRITE)

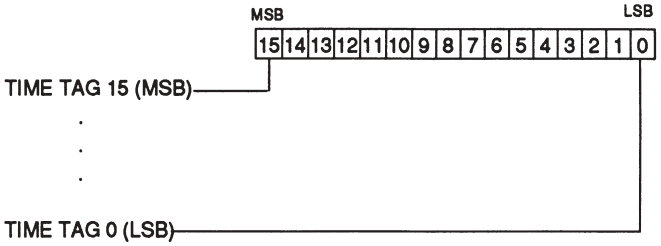


FIGURE 8. TIME TAG REGISTER

STACK POINTER REGISTER
(Register Address 011; Read Only)

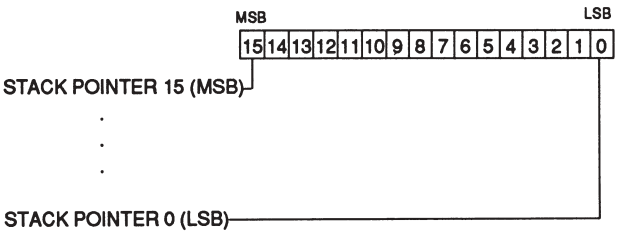


FIGURE 6. STACK POINTER REGISTER

INTERRUPT STATUS REGISTER
(Register Address 110; Read Only)

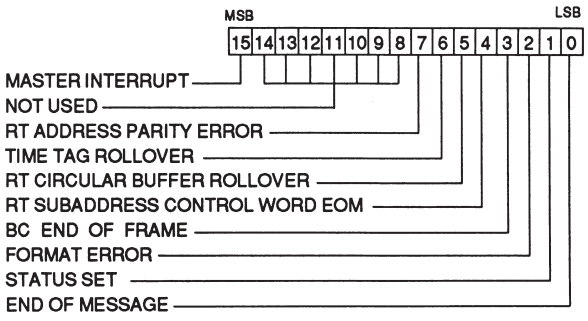
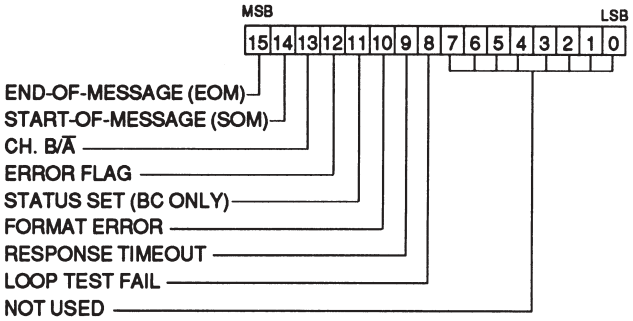


FIGURE 9. INTERRUPT STATUS REGISTER

TIME TAG

The second word of the Message Block Descriptor is the 16-bit Time Tag. The Time Tag value is written from the Time Tag Register during the BC SOM sequence. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, 64, or “External” (variable) µs/LSB. After the host processor has determined the message status by reading the message block descriptor, it may then read the results of the message from the respective message block. That is, it should read the received Loopback word, followed by the RT Status Word(s), and possibly Data words received from the responding RT.



Note: Bits 7 through 0 will read as FF (hex) after the Block Status Word has been written to shared RAM during a Start-of-Message (SOM) or End-of-Message (EOM) sequence.

FIGURE 10. BLOCK STATUS WORD

BC OPERATION

The BC protocol of the BU-61559 implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of individual BC Control Words and the T/$\overline{R}$ bit of the Command Word to be transmitted. In addition to message format, the BC Control Word allows bus channel, self-test, and Status Word masking to be specified on an individual message basis. The BC performs all error checking required by 1553B. This includes validation of sync type and encoding, Manchester II encoding, parity, bit count, word count, and Status Word RT Address field. RT response time is verified to be less than the BU-61559's response timeout value of 17.5 to 22.5 µs.

BC MEMORY ORGANIZATION

TABLE 2 illustrates a typical memory map for BC mode. It is important to note that the only fixed locations for the BU-61559 in BC mode are for the two Stack Pointers (address locations 0100 (hex) and 0104) and for the two Message Count locations (0101 and 0105). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K (8K internal) shared RAM address space.

For simplicity of illustration, 64 words are allocated for each BC message block in the typical BC memory map of TABLE 2. Note, however, that the actual maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). Therefore, it is possible to pack more messages into the shared RAM address space, particularly if the 256-word boundaries are disabled.

ACTIVE AREAS DOUBLE BUFFERING

The Active Area facility provides a global mechanism for dividing the shared RAM into “active” and “non-active” areas. At any point in time, only the various data structures within the “active” area are accessed by the internal 1553 memory management logic. It should be noted, however, that at any point in time, **both** the active and non-active areas are accessible by the host processor.

An overview of the BU-61559's memory management scheme for BC mode is illustrated in FIGURE 11. The BC may be programmed to transmit multi-message frames of up to 64 unique messages and up to 256 total messages per frame. The number of messages to be processed is programmable by means of a fixed Message Count location in the shared RAM. In addition, the host processor must initialize a second fixed location as the Stack Pointer. This RAM location contains a pointer that references the four-word message block descriptor (in the Stack area of shared RAM) for each message to be processed. Each message resides in a designated message block area of the shared RAM. The starting location for each message block is specified by a pointer that is stored in the fourth location of the block descriptor for the respective message. This pointer must be loaded by the host processor before the message is processed. The first word of each BC message block is the BC Control Word.

TABLE 2. TYPICAL BC MEMORY MAP (SHOWN FOR 8K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0104	Stack Pointer B (fixed location)
0105	Message Count B (fixed location)
• • •	• • •
0140-017F	Message Block 0
0180-01BF	Message Block 1
01C0-01FF	Message Block 2
• • •	• • •
1EC0-1EFF	Message Block 118
1F00-1FFF	Stack B

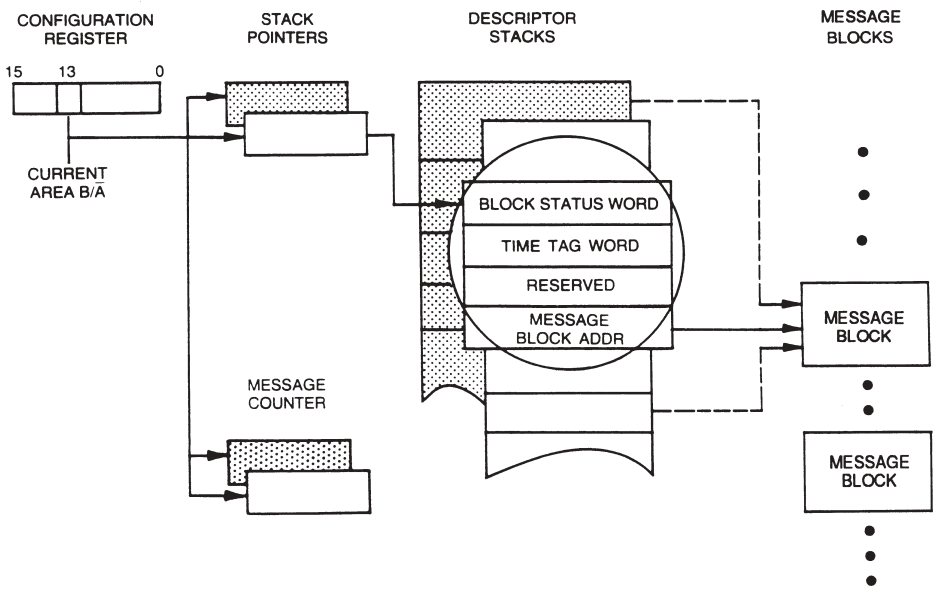


FIGURE 11. BC MEMORY MANAGEMENT

BC CONTROL WORD

For each of the BC Message Block formats, the first word in the block is the BC Control Word. The BC Control Word is **not** transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, and specifies the "expected value" of the BROADCAST COMMAND RECEIVED RT Status bit.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for an RT-to-RT transfer), followed by data words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The Loopback Word is an on-line self-test feature in which the received version of the last transmitted word is stored in the next location in the shared RAM. The subsequent locations after the Loopback Word are reserved for received Status Words and Data Words (for transmit messages).

The next word in RAM after the BC Control Word is the MIL-STD-1553B Command Word (for an RT-to-RT or RT-to-Broadcast transfer, it is the first of two Command Words). This word is read by the 1553 protocol logic and transmitted on the 1553 bus. The (first) Command Word is possibly followed by a second Command Word or Data Words to be read from RAM and transmitted. The location in RAM after the **last** transmitted word is reserved for the Loopback Word. Subsequent locations in the shared RAM are reserved for Status and possibly Data Words

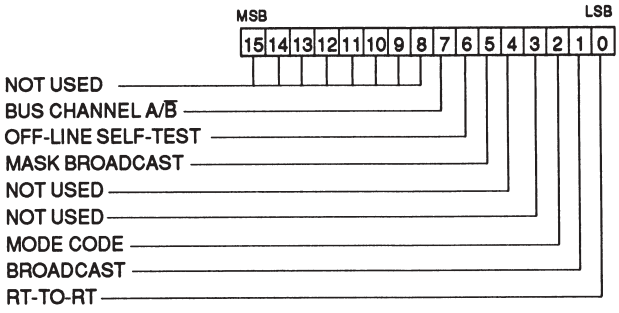


FIGURE 12. BC CONTROL WORD

anticipated to be received from the responding RT(s). Assuming that the RT responds before a BC response timeout occurs, these word(s) are stored in the allocated locations in the shared RAM. If the Loopback test passes, and the RT responds before the BC Response Timer times out with a "Correct" RT Status Word (correct RT address and the "expected value" for the lower 11 bits), followed by the correct number of valid data words, the Block Status Word will be written to indicate "End of Message, No Errors" during the BC End-of-Message sequence. Note that for an RT-to-RT transfer, the BU-61559 BC checks the Status Words from **both** the transmitting and receiving RTs.

BC MESSAGE BLOCK FORMATS

In BC mode, the BU-61559 supports all MIL-STD-1553B message formats. For each 1553B message format, the BU-61559 mandates a specific sequence of words within the BC Message Block. This includes locations for the Control, Command, and (transmitted) Data Words that are loaded by the host processor to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status, and Data Words. FIGURE 13 illustrates the organization of the BC message blocks for the various MIL-STD-1553B message formats. Note that for all of the message formats, the BC Control Word is located in the first location of the message block.

BC INTERRUPTS

In BC mode, the host processor may be interrupted after every BC message (EOM interrupt), after the entire message frame has been processed (BC END OF FRAME interrupt), after erroneous messages (FORMAT ERROR interrupt), after a Status Word address mismatch or "unexpected" Status Word bit values (STATUS SET interrupt) and/or after the Time Tag Register has rolled over. The user has the further option of programming the BC for stop-on-error operation. Alternatively, the host processor may determine if the current message frame has been completed by polling the contents of either the Interrupt Status Register or the Stack Pointer or Message Count RAM locations.

BC DESCRIPTOR STACK

The host processor may determine the status of individual messages by reading the first two locations of the respective descriptor block. The first location within the descriptor block contains the Block Status Word. In BC mode, the Block Status Word contains information relating to whether the message is in progress or has been completed, which bus channel it was transmitted on and whether there were any errors in the message.

The second location contains the Time Tag Word. The current value of the internal Time Tag Register is written to the Time Tag Word during both the BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences.

The third location of the BC Message Block Descriptor is RESERVED (not used). The fourth location is used to store the MESSAGE BLOCK ADDRESS Word. The MESSAGE BLOCK ADDRESS must be loaded by the host processor **before** the message is processed. It is then used as a pointer by the BU-61559 memory management logic for accessing the start of the respective Message Block.

The two other fixed locations in the shared RAM address space that must be initialized by the host processor for BC mode are the Stack Pointer and Message Counter locations. The Stack Pointers are located in address locations 0100 (for Area A) and 0104 (for Area B). The Stack Pointer should be initialized to point to the first word of the Message Block Descriptor (Block Status Word) for the first message to be processed. The Message Counters are located in addresses 0101 (for Area A) and 0105 (for Area B). The Active Area Message Counter must be preloaded by the host processor with the ones complement of the number of messages to be processed (e.g., FFFE represents a message count of 1). The Message Counter is incremented by one following each BC message processed.

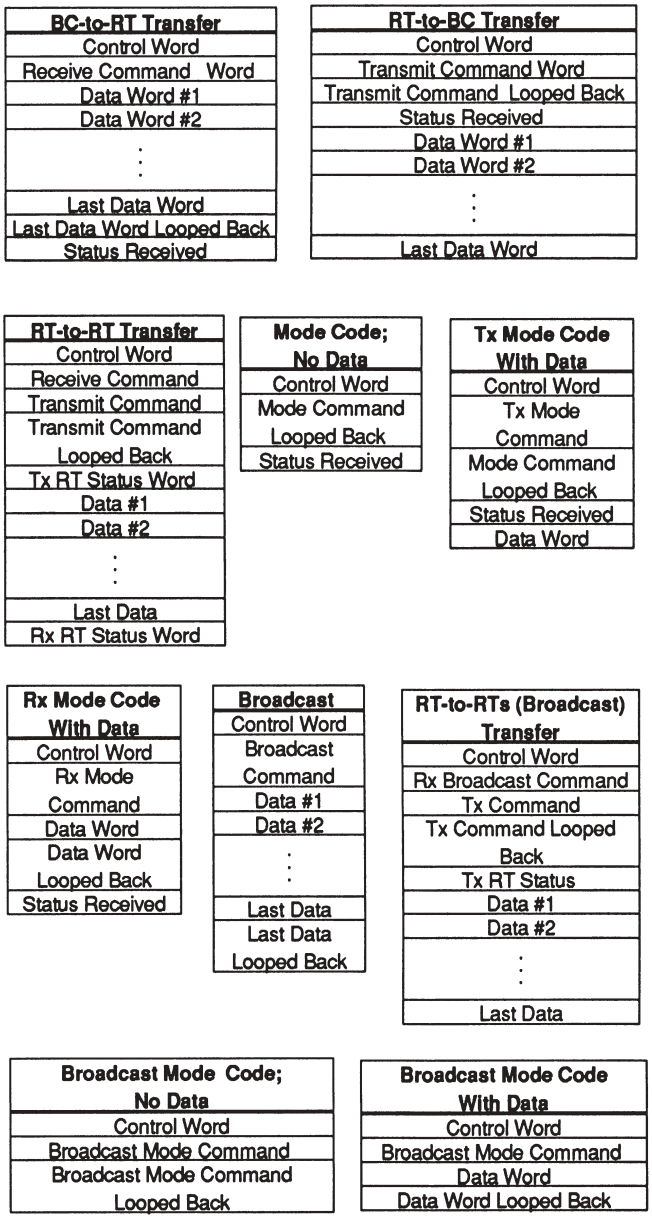


FIGURE 13. BC MESSAGE BLOCK FORMATS

RT OPERATION

Some of the principal features of the BU-61559 for Remote Terminal (RT) mode include implementation of all MIL-STD-1553B formats and dual redundant mode codes, internal command illegalizing, implementation of the “Busy” function, an internally formulated BIT Word, and comprehensive error checking, including RT-to-RT transfer errors.

Remote Terminal address for the BU-61559 is pin programmable. Six input pins, RTAD4 through RTAD0 plus RTADP, need to be correctly strapped for RT address and odd address parity to enable the BU-61559 to recognize and respond to its own discrete RT address. In addition, the upper two bits of Configuration Register #1 must be programmed for 1 and 0 respectively to configure the BU-61559 for RT mode. “Active Area” and the RT Status Word bits Subsystem Flag, Service Request, Busy, and Dynamic Bus Control Accept are also software programmable by means of Configuration Register #1.

The BU-61559's advanced RT features are selectable by means of Configuration Register #2. The two most important of these features are the ENHANCED RT MODE (bit 1) and the option for SEPARATION OF BROADCAST MESSAGES (bit 0). If the enhanced mode is not chosen, the BU-61559's memory management scheme defaults to that of the BUS-61553 AIM-HY. In this configuration, each T/R-subaddress is mapped to a single data block by means of its respective Lookup Table entry. In this mode, the data block for each T/R-subaddress is repeatedly overwritten or overread. If the enhanced mode is selected, the user has the option of selecting either the “single message” mode or making use of the circular buffer option, on a transmit/receive/broadcast-subaddress basis. The circular buffer option supports bulk data transfers by automatically accessing/storing multiple receive or transmit messages per T/R-subaddress, up to a maximum of 8192 words.

The BU-61559 includes an option for internal command illegalizing. If this option is utilized, 256 words of the BU-61559's 8K X 16 of internal dual port RAM may be dedicated for the command illegalization function. The BU-61559 allows any subset of the 4096 possible 1553 Command Words to be illegalized as a function of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code.

Other RT options controlled by Configuration Register #2 include automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command and capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands.

RT MEMORY ORGANIZATION

A typical memory map for the BU-61559 in RT mode is illustrated in TABLE 3. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, for RT mode there are three other areas of the AIM-HY'er address space that are designated as fixed locations. These are for the Area A and Area B Lookup Tables and for the optional section of the shared internal dual port RAM that may be selected for the use of command illegalizing. The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, are located in address range 0140 to 01BF for Area A and address range 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words as well as the individual Data Block Pointers. The Subaddress Control

TABLE 3A. TYPICAL RT MEMORY MAP (WITH THE COMMAND ILLEGALIZING OPTION SELECTED)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0104	Stack Pointer B (fixed location)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-025F	Data Block 0
0260-027F	Data Block 1
• • •	• • •
02E0-02FF	Data Block 6
0300-03FF	Command Illegalizing
0400-041F	Data Block 7
0420-043F	Data Block 8
• • •	• • •
1EE0-1EFF	Data Block 221
1F00-1FFF	Stack B

TABLE 3B. TYPICAL RT MEMORY MAP (WITH THE COMMAND ILLEGALIZING OPTION NOT SELECTED)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0104	Stack Pointer B (fixed location)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-025F	Data Block 0
0260-027F	Data Block 1
0280-029F	Data Block 2
02A0-02BF	Data Block 3
• • •	• • •
1EE0-1EFF	Data Block 229
1F00-1FFF	Stack B

Words are used to specify the RT memory management scheme for each Tx/Rx/Bcst-subaddresses. If used, address range 0300-03FF is dedicated as the illegalizing section of RAM. The actual Stack RAM area as well as the individual data blocks may be located in any of the non-fixed areas in the shared RAM address space.

TABLE 3A illustrates the RT memory map for the case where the internal illegalizing feature is used. By connecting the ILLENA input to logic 1 (+5V), address locations 0300-03FF (hex) are dedicated for the command illegalizing function. TABLE 3B illustrates the typical memory map for the case when the internal illegalization feature is **not** used. In this instance, ILLENA must be strapped to logic 0 (ground) so that address locations 0300-03FF (hex) may be used for storage of stack data or message data blocks.

ACTIVE AREA DOUBLE BUFFERING

The BU-61559 provides a global double buffering mechanism by means of bit 13, CURRENT AREA B/$\overline{A}$, of Configuration Register #1. At any point in time, this allows for one stack pointer, stack area, Lookup Table, and set of data blocks to be designated as “active” (used for the processing of 1553 messages) and the alternate set of respective data structures to be designated as “non-active”. **Both** the “active” and “non-active” RAM areas are **always accessible** by the host processor.

RT LOOKUP TABLES

Referring to TABLE 4, the RT Lookup tables are expanded beyond those of the BUS-61553. In the 61553, the Lookup Tables are 64 words each, containing the Lookup Table pointers for the 32 receive subaddresses and the 32 transmit subaddresses. For the BU-61559, there are an additional 64 words in each of the two Lookup Tables. Thirty two (32) of these words provide optional separation of broadcast messages. The last 32 words are subaddress control words, one appropriated for each RT subaddress.

SUBADDRESS CONTROL WORD

Referring to FIGURE 13.1 and TABLE 5, in the Enhanced RT Memory Management mode, each of the 32 Subaddress Control Words specifies the memory management and interrupt schemes for the respective subaddress. For each Subaddress Control Word, five bits control the memory management scheme and interrupts for each of transmit, receive, and broadcast messages.

For each transmit, receive, or broadcast subaddress, three bits are used to specify the memory management scheme. For each Tx/Rx/Bcst subaddress, the memory management scheme may be selected for either the “single message” mode or the “circular buffer” mode.

In the single message mode, a single data block is repeatedly overread (for transmit data) or overwritten (for receive or broadcast data). Alternatively, in the circular buffer mode, Data Words for successive messages to/from any particular Tx/Rx/Bcst subaddresses are read from or written to the **next** contiguous block of locations in the respective circular buffer.

The size of the circular buffer for each transmit, receive, or broadcast subaddress may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words. For each Tx/Rx/Bcst subaddress, two bits of the subaddress control word are used to enable interrupts. One of these bits will result in an interrupt following **every** message directed to the specific Tx/Rx/Bcst sub-

TABLE 4. RT LOOK-UP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140 • • • 015F	01C0 • • • 01DF	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Table
0160 • • • 017F	01E0 • • • 01FF	Tx SA0 • • • Tx SA31	Transmit Lookup Table
0180 • • • 019F	0200 • • • 021F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Table (Optional)
01A0 • • • 01BF	0220 • • • 023F	SACW SA0 • • • SACW SA31	Subaddress Control Word Lookup Table (Optional)

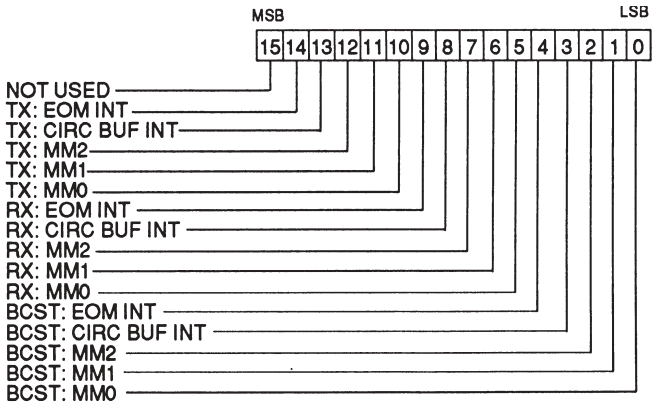


FIGURE 13.1 SUBADDRESS CONTROL WORD BIT MAP

address. The other of these two bits will result in an interrupt at the end of a message if the message resulted in the Lookup Table pointer for the respective Tx/Rx/Bcst-subaddress crossing the lower boundary of the circular buffer, rolling over to the top of the buffer.

SINGLE MESSAGE MODE

If bit 1 of Configuration Register #2 is logic 0, the BU-61559's memory management scheme assumes its default or non-enhanced mode. In the non-enhanced RT operation, the single message memory management mode is used for **all** receive, transmit, or broadcast subaddresses. In addition, under the enhanced RT memory management scheme, the single message mode may still be used for individual receive, transmit, and/or broadcast subaddresses. This is the case if the three applicable "memory management" bits in the respective Subaddress Control Word are set to logic 0.

The operation of the single message RT memory management mode is illustrated in FIGURE 14. In the single message mode, the Lookup Table must be loaded by the host processor. At the start of each message, the Lookup Table entry is stored in the third position of the respective message block descriptor in the Stack area of RAM. Received Data Words are written to or transmitted Data Words are read from the Data Block referenced by the respective Lookup Table Pointer. In the single message mode, the current Lookup Table pointer **is not** written to by the BU-61559 memory management logic at the end of a message. Therefore, if a subsequent message is processed for the same subaddress, the **same** Data Block will be overwritten or overread.

CIRCULAR BUFFER MODE

In the enhanced RT memory management mode, individual transmit, receive, and broadcast subaddresses may be programmed for either the single message or circular buffer modes.

TABLE 5. SUBADDRESS CONTROL WORD - MEMORY MANAGEMENT OPTIONS

MM2	MM1	MM0	DESCRIPTION	COMMENT
0	0	0	Single Buffer	Circular buffer of specified size.
0	0	1	128-Word	
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

The operation of the circular buffer RT memory management mode is illustrated in FIGURE 15. As in the non-enhanced mode, the individual Lookup Table entries are initially loaded by the host processor. At the start of each message, the Lookup Table entry is stored in the third position of the respective message block descriptor in the Stack area of RAM. Receive or Transmit Data Words are transferred to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

Under any of the following conditions, the location **after** the last address location accessed for the message will be stored into the respective Lookup Table pointer location following the end of a message: (1) If bit 11 of Configuration Register # 2 (OVERWRITE INVALID DATA) is logic 0, (2) following a transmit message, or (3) following a **valid** receive or broadcast message, if bit 11 of Configuration Register #2 is logic 1. In this way, data for the next message for the respective Tx/Rx/Bcst-subaddress will be accessed to/from the next lower contiguous block of address locations in the circular buffer.

If the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 is logic "1", the location **after** the last word accessed for the message is stored into the respective Lookup Table location **only following a valid received (or transmitted) message**. Assuming that the value of the Lookup Table pointer is updated, data for the **next** message for the respective Tx/Rx/Bcst subaddress will be accessed to/from the next lower contiguous block of locations in the circular buffer. If the OVERWRITE INVALID DATA bit is set, the Lookup Table pointer will **not** be updated at the end of the message if there was an error in the message. This allows failed messages in a bulk data transfer to be retried without disturbing the circular buffer data structure, and without intervention by the RT's host processor.

When the pointer reaches the lower boundary of the circular buffer (located at 128-, 256-, . . . 8192-word boundaries in the shared RAM address space), the pointer moves to the top boundary of the circular buffer, as shown in FIGURE 15.

It should be noted that the pointer to the start of the RT message block is stored in the third location of the message block descriptor (in the stack) for the single message mode as well as for the circular buffer mode.

RT STACK AND INTERRUPTS

In RT mode, the Stack area of RAM contains a real time chronology of all messages processed by the BU-61559. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the data block, and the 16-bit received Command Word. Prior to the processing of messages, the host processor should initialize the Stack Pointer. In some applications, it may also prove helpful to "zero out" the Stack area prior to receiving messages.

In RT mode, the host processor may determine that a message has been processed either by means of interrupts or by polling the Interrupt Status Register or the Stack Pointer.

The Stack Pointer increments by four (modulo 256) during the Start-of-Message sequence for each message processed. After processing a message, the host CPU should read the Block Status Word, Time Tag, data block starting address, and Command Word received from the Message Block Descriptor in the Stack. Assuming a valid message was received, it may then read the received data from the respective data block.

The BU-61559 offers a great deal of flexibility in terms of RT interrupt processing. In some systems, the transmission or reception of a message with a particular subaddress denotes the end of a complete set of consistent data. In this instance, the user should use the RT SUBADDRESS CONTROL WORD INTERRUPT in order to issue an interrupt request **only for a particular T/R-subaddress**, rather than following every message. One technique would then be for the host processor to switch the active area of shared RAM, by toggling bit 13 of Configuration Register #1 at this time. This allows the next group of messages comprising a consistent data set to be stored in the alternate area of the shared RAM address space.

IMPLEMENTING BULK DATA TRANSFERS

In systems involving bulk data transfers over the 1553 bus to/from the same subaddress, the host CPU should set the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 and enable the RT CIRCULAR BUFFER ROLLOVER interrupt request. By doing so, the routine transfer of multiple messages to the selected subaddress, **including errors and retries**, is transparent to the host processor. The BU-61559 will issue an interrupt request only after it has received the anticipated number of **valid** data words to the particular subaddress. The anticipated number of words to be received (or transmitted) is programmable up to 8192 words.

RT COMMAND ILLEGALIZATION

The BU-61559 provides an internal mechanism for RT Command Word illegalizing. The scheme utilizes a 256-word area in the BU-61559's internal dual port RAM. A benefit of this feature is reduced printed circuit board space requirements, by eliminating the need for an external PROM, PLD, or RAM device to perform the illegalizing function. The BU-61559's illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization scheme is that it is inherently self-testable.

In order to use the BU-61559's internal dual port RAM for RT command illegalizing, it is necessary to connect the input signal ILLENA to logic 1. By so doing, address locations 0300 through 03FF are dedicated for the message illegalizing function and **must not** be used for Stack or Data Block storage. The RT command illegalization option may be disabled by connecting ILLENA to logic 0. In this instance, the BU-61559 assumes all received Command Words are legal. If ILLENA is connected to logic 0, address locations 0300 through 03FF may be used for the storage of Stacks or Data Blocks.

It should be noted that the state of the ILLENA input has **no effect** for BC or Monitor (MT) modes.

If the command illegalizing feature is used, address locations 0300-03FF **must** be mapped to the respective locations in the BU-61559's 8K X 16 of **internal** shared RAM.

ADDRESSING THE ILLEGALIZATION TABLE

The addressing scheme of the illegalization RAM is illustrated by FIGURE 16. As shown, the base address of the illegalizing RAM is 0300 (hex). The index into the illegalizing RAM is formulated by means of $\overline{\text{BROADCAST}}$/OWN ADDRESS, T/$\overline{R}$ bit, Subaddress, and the MSB of the Word Count/Mode Code field (WC/MC4).

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from non-broadcast receive commands and mode commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a 2-word receive command to subaddress 1 may be illegalized.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per subaddress). The next 64 words refer to broadcast transmit commands. Since non-mode code broadcast transmit commands are by definition invalid, this section of the table (except for subaddresses 0 and 31) does **not** need to be initialized by the user. The next 64 words correspond to non-broadcast receive commands. The final 64 words refer to non-broadcast transmit commands. Messages with Word Count/Mode Code (WC/MC) fields between 0 and 15 may be illegalized by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

(1) To illegalize a particular word count for a given broadcast/own address-T/$\overline{R}$ subaddress, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a legal command. The BU-61559 will respond to an illegalized non-broadcast command with the Message Error bit set in its RT Status Word.

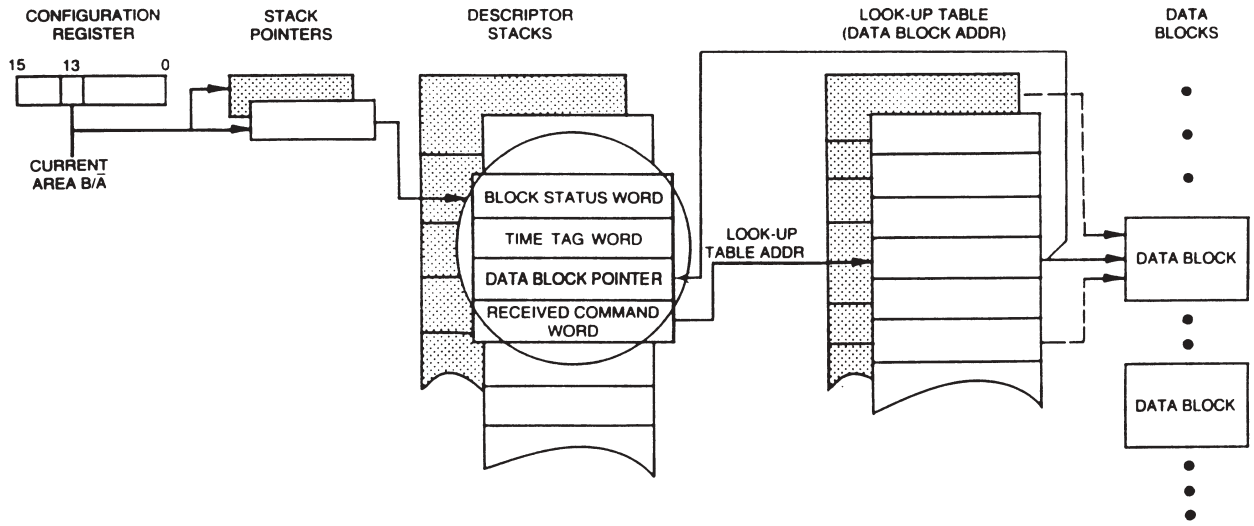


FIGURE 14. RT MEMORY MANAGEMENT - SINGLE MESSAGE MODE

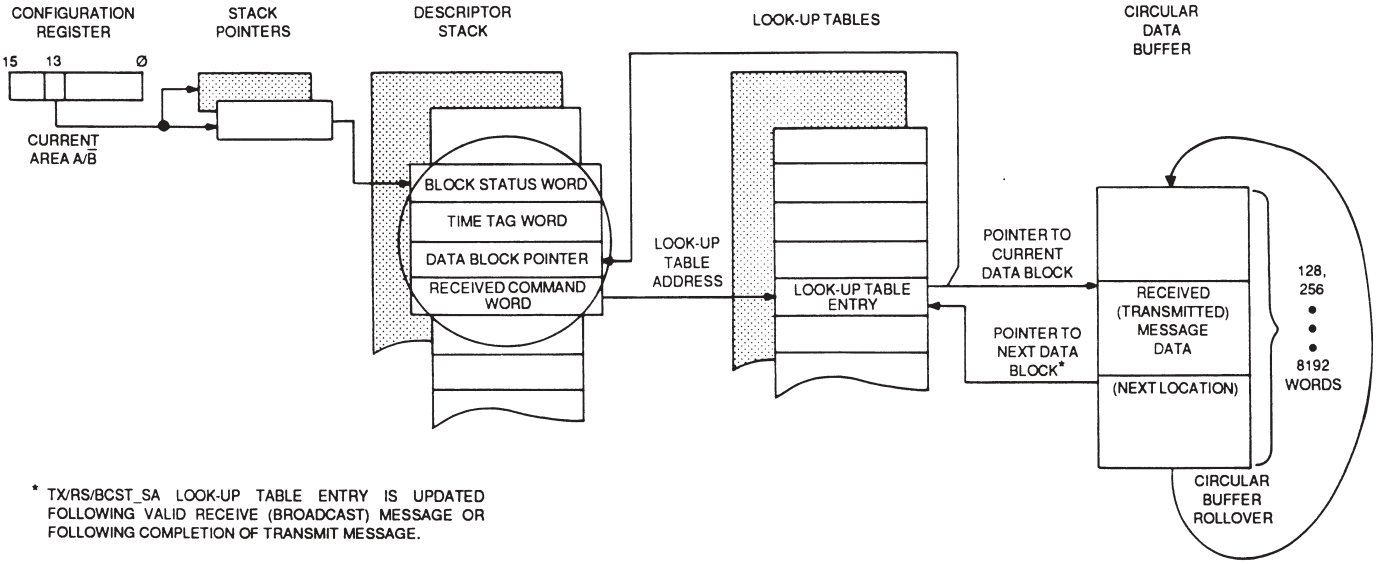


FIGURE 15. RT MEMORY MANAGEMENT - CIRCULAR BUFFER MODE

(2) For subaddresses 00001 through 11110, the “WC/MC” field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the “WC/MC” field specifies the Mode Code field of the respective Command Word.

(3) Since non-mode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The BU-61559 will **not** respond to a non-mode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not the corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the BU-61559 will respond with its Message Error bit set.

BROADCAST OPTION

In RT mode, the BU-61559 supports the use of broadcast messages as a pin-programmable option. If the input signal BRO_ENA is connected to logic 1 (+5V), the BU-61559 will recognize RT Address 31 as the broadcast address. If BRO_ENA is connected to logic 0 (ground), then RT Address 31 will not be recognized as the broadcast address and may be used as a discrete terminal address. MIL-STD-1553B stipulates that RT address 31 shall **not** be assigned as a discrete terminal address.

BUSY BIT

If the host CPU asserts the $\overline{\text{BUSY}}$ bit low in Configuration Register #1, the BU-61559 will respond with the BUSY bit set in its RT Status Word. For a receive command, words will be written to the data block in the shared RAM referenced by the respective Lookup Table location. For a transmit command, the AIM will respond with Status/BUSY, but no data words will be transmitted.

DYNAMIC BUS CONTROL ACCEPTANCE

The Dynamic Bus Control Acceptance bit in the RT Status Word will only be set if the $\overline{\text{DYNAMIC BUS ACCEPT}}$ bit in the Configuration Register is set to logic 0 **and** the RT is responding to a Dynamic Bus Control mode code. It should be noted that the BU-61559 will **not** automatically switch from RT to BC mode following reception (and acceptance) of a Dynamic Bus Control mode command.

SUBSYSTEM FLAG STATUS WORD BIT

The Subsystem Flag Status Word bit is controllable from the host processor by means of bit 8 of Configuration Register #1, $\overline{\text{SSFLAG}}$. The Subsystem Flag Status bit will be set if $\overline{\text{SSFLAG}}$ is programmed to logic “0”. In addition, the Subsystem Flag Status Word bit will also be set if a logic “0” is applied to the $\overline{\text{SSFLAG}}$ input pin. For some applications, the output of a CPU watchdog timer may be connected to the $\overline{\text{SSFLAG}}$ input pin. This provides a mechanism for the system bus controller to determine that the RT's host processor has failed.

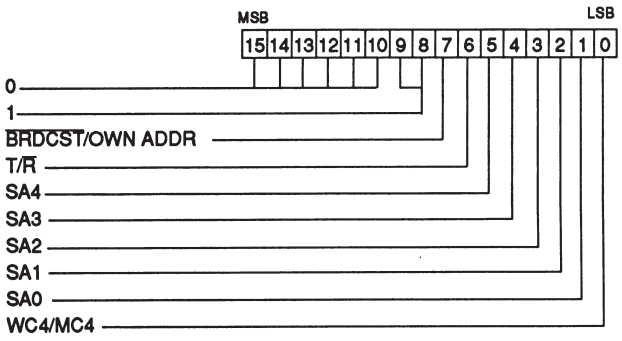


FIGURE 16. ILLEGALIZING RAM ADDRESS DEFINITION

RTFAIL, RTFLAG SIGNALS

The BU-61559 provides a degree of flexibility for the purposes of monitoring of the RT built-in self-test by the host processor as well as in formulation of the RT FLAG Status Word bit. This is accomplished by bringing out the $\overline{\text{RTFAIL}}$ output signal and the $\overline{\text{RTFLAG}}$ input signal.

The $\overline{\text{RTFAIL}}$ output is updated following every non-broadcast message processed by the BU-61559 in RT mode. $\overline{\text{RTFAIL}}$ will be asserted low following either a timeout of the Transmitter Failsafe timer (768 µs) and/or a failure of the looptest. A looptest failure indicates either a mismatch in the bit pattern and/or an invalid word for the received version of the last transmitted word.

The $\overline{\text{RTLAG}}$ input is used to control the RT Flag bit in the BU-61559's RT Status Word. It is sampled following the reception of all valid non-broadcast Command Words. In most applications, $\overline{\text{RTFAIL}}$ will be connected directly to $\overline{\text{RTFLAG}}$. In other instances, provisions may be implemented such that the host processor can control the $\overline{\text{RTFLAG}}$ input to the BU-61559. This allows the CPU to assert $\overline{\text{RTFLAG}}$ low following failure of a software-driven self-test of the BU-61559.

MONITOR OPERATION

To initialize the BU-61559 for Monitor (MT) mode, the host processor should program the upper two bits of Configuration Register #1 to 0 and 1 respectively. Next, the Stack Pointer for the active area should be loaded with the starting location of the monitor stack in the BU-61559 shared RAM address space. Finally, to start the monitor, a “Start” command should be issued by means of the Start/Reset Register.

In Monitor mode, the BU-61559 continuously monitors both 1553 bus channels, storing all words to the shared RAM in the order in which they are received. For each word received from the 1553 bus, the BU-61559 stores **two** 16-bit words to the shared RAM

address space. The first of the two words is the actual 16 bits of data from the received word. The second word is the Identification (ID) or “Tag” word.

The Monitor ID Word contains a Word Flag bit (always logic 1) plus information relating to bus channel, word validity, Command-Status/Data sync type, and inter-word gap time information. This latter field includes a “Contiguous Data” bit as well as an 8-bit gap time field, indicating 0 to 127 µs with a resolution of 0.5 µs per LSB.

To take the BU-61559 monitor off-line, the host CPU must issue a RESET command to the Start/Reset Register.

TABLE 6 illustrates a typical memory map for monitor mode. The BU-61559 Identification Word is defined in FIGURE 17.

SELF-TEST

The BU-61559 contains a number of self-test features. The internal registers and shared RAM are accessible to the host processor at all times. The inclusion of wraparound capability for the 1553 front end transceiver and encoder/decoder supports BC off-line and on-line self-test as well as RT on-line self-test.

The internal registers and shared RAM can be tested by means of host processor software routines to implement “checkerboard”, “walking zero”, and “walking one” patterns and/or by writing the address as the data to each RAM location and then reading back and verifying the contents of the entire RAM array.

A common element of all of the wraparound self-test features is the method by which loopback words are checked. In each case, the last word transmitted by the BC or RT is looped back into the active Manchester II decoder. The received version of this word is verified for: (1) Validity (sync field and Manchester II bit encoding, bit count, and parity), and (2) A bit-by-bit comparison to the transmitted version of the word. The loopback test is considered to have failed if **either** of these two criteria is not met.

In the BC off-line self-test, the 1553 transmitter is inhibited, and the encoder output is muxed directly into the respective decoder input. For both the BC off-line and on-line self-tests, the received version of the last transmitted word is stored in the next location of the shared RAM following the transmitted loopback word. For both the BC and RT loopback tests, the LOOPTEST FAIL bit in the message's Block Status Word will be set as a result of a failed loop test.

INTERFACE TO MIL-STD-1553 BUS

Interfacing the BU-61559 to a MIL-STD-1553 bus requires a pair of BUS-25679 or BUS-29854 pulse transformers. These transformers, or QPL equivalents, are available from Beta Transformer Technology Corporation, a subsidiary of DDC. The BU-61559 hybrid and Beta Transformers may be wired for either direct coupled or stub coupled configurations.

The interface between a BU-61559X1 or BU-61559X2 and a MIL-STD-1553 bus is illustrated in FIGURE 18.

BUFFERED PROCESSOR INTERFACE

As a means of reducing printed circuit board space requirements, 16-bit address and data buffers are incorporated into the BU-61559 AIM-HY'er.

As determined by the strapping of the input signal TRANSPARENT/BUFFERED, the BU-61559 processor interface may be configured for either of two modes. TRANSPARENT/BUFFERED should be strapped to logic “0” for buffered mode, logic “1” for transparent mode.

TABLE 6. TYPICAL MT MEMORY MAP

ADDRESS (HEX)	FUNCTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	•
0005	•
0006	•
•	•
•	•
0100	Stack Pointer (Fixed Location)
•	•
•	•
FFFF	•

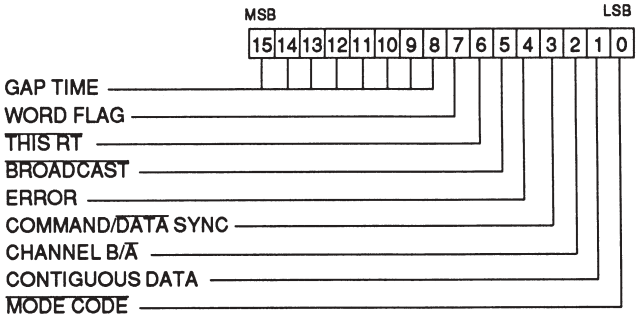


FIGURE 17. MONITOR IDENTIFICATION WORD

BUFFERED MODE

In the buffered mode (reference FIGURE 19), the processor data and address buses connect directly to the corresponding buses of the BU-61559. In this mode, the shared memory size is limited to the 8K X 16 of internal RAM. In the buffered mode, the internal address latches and data buffers serve to isolate the external processor address/data buses from the internal memory address/data buses.

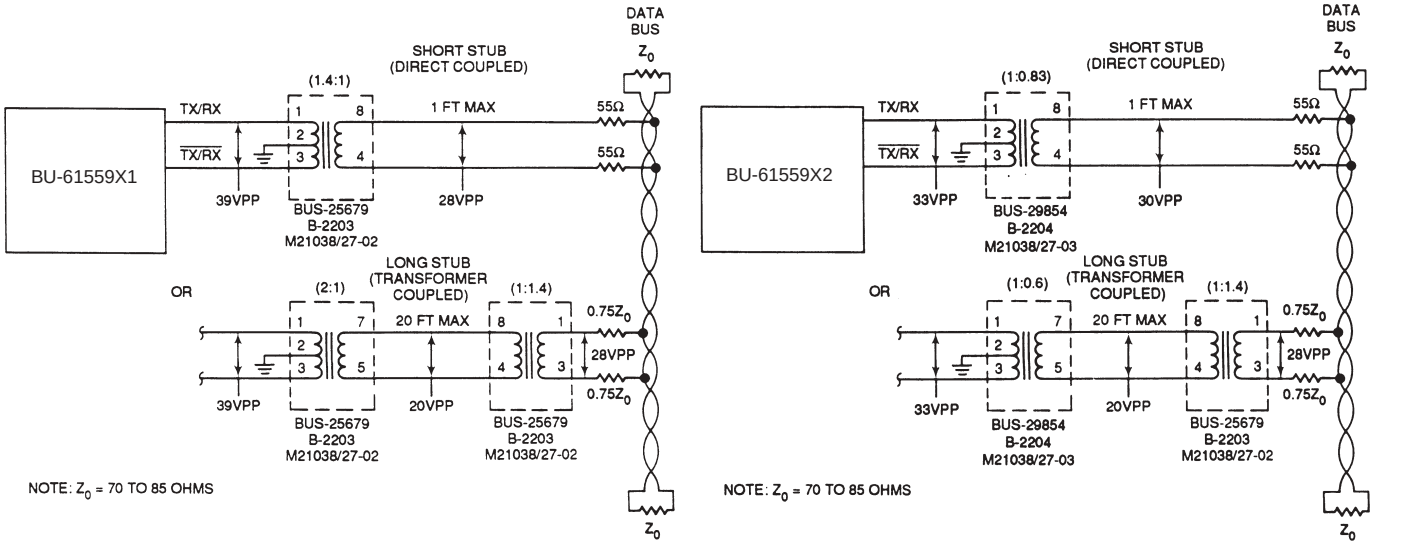
The BU-61559 supports a direct interface to a multiplexed processor bus by means of the input signal ADDR_LAT. When ADDR_LAT is high, the latch/buffers for A15-A0 are in their transparent mode. When ADDR_LAT is low, the latch/buffers for A15-A0 are in their latched mode. In the buffered mode, the address latch/buffers are directed inward for CPU accesses and are disabled for 1553 accesses. The bidirectional data buffers are directed inward for CPU write transfers, outward for CPU read transfers, and are disabled for 1553 transfers.

In the buffered mode, the output $\overline{\text{MEMENA-OUT}}$ **must** be connected to the input $\overline{\text{MEMENA-IN}}$.

TRANSPARENT MODE

The transparent mode (reference FIGURE 20) supports an interface to up to 64K words of external shared RAM and/or to a STANAG-3910 component set. In the transparent mode, the memory control signals $\overline{\text{MEMENA-OUT}}$, $\overline{\text{MEMOE}}$, and $\overline{\text{MEMWR}}$ are used to read and write data from/to external RAM. $\overline{\text{MEMENA-OUT}}$ is the BU-61559's Chip Select ($\overline{\text{CS}}$) output signal. For internal RAM accesses, the input $\overline{\text{MEMENA-IN}}$ should be asserted low. When there is no ongoing memory access, or for accesses to external RAM, $\overline{\text{MEMENA-IN}}$ should be presented as a logic 1.

In the transparent mode, the address buffers drive the CPU address onto the internal memory bus for CPU transfers; for 1553 transfers, the internal memory address is asserted on the external address bus. The data buffers are directed outward for



NOTES for FIGURE 18:
(1) Shown for one of two redundant buses that interface to the BU-61559/60 Series hybrid.
(2) Transmitted voltage level on 1553 bus is 6 Vp-p min, 7 Vp-p nominal, 9 Vp-p max.
(3) Required tolerance on isolation resistors is 2%. Instantaneous power dissipation (when transmitting) is approximately 0.5 W (typ), 0.8 W (max).
(4) Transformer pin numbering is correct for DDC BUS-25679 or BUS-29854 transformer. For the Beta transformer (e.g., B-2203) or the QPL-21038-31 transformer (e.g., M21038/27-02), the winding sense and turns ratio are mechanically the same, but the pin numbering is reversed. Therefore, it is necessary to reverse pins 8 and 4 or pins 7 and 5 in the diagram for the Beta or QPL transformers.

FIGURE 18. BU-61559X1, BU-61559X2 INTERFACE TO 1553 BUS

the CPU reading internal RAM (or registers), for 1553 write accesses, for 1553 read accesses from internal RAM, and for internal transfers of received Command Words in RT mode. The data buffers are directed inward (toward the memory data bus) for CPU write accesses to internal RAM (or registers) or for the 1553 reading external RAM.

It should be noted that A15 through A0 as well as D15 through D0 have internal pullup resistors to +5V. External pullup resistors **are not required**.

FIGURE 19 illustrates a generic interconnection of the BU-61559 in the buffered mode. In this configuration, only the 8K words of internal RAM are used. No external address or data buffers are required.

FIGURE 20 illustrates a generic interconnection of the BU-61559 in the transparent mode. This configuration supports up to 64k words of address space. This may optionally include the 8K words of internal RAM. In this configuration, external address and data buffers **are required**.

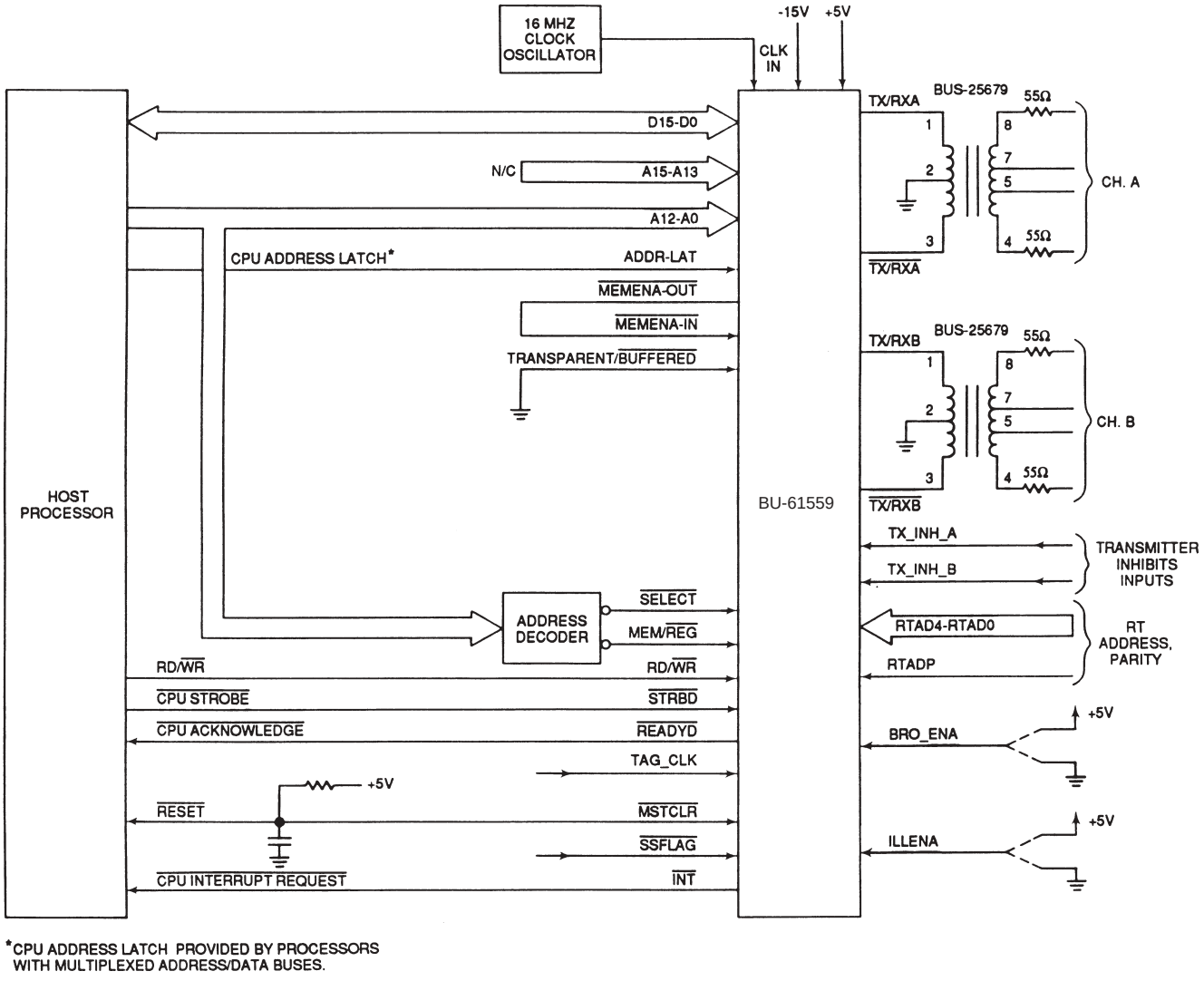


FIGURE 19. BU-61559 INTERCONNECTION DIAGRAM FOR BUFFERED MODE

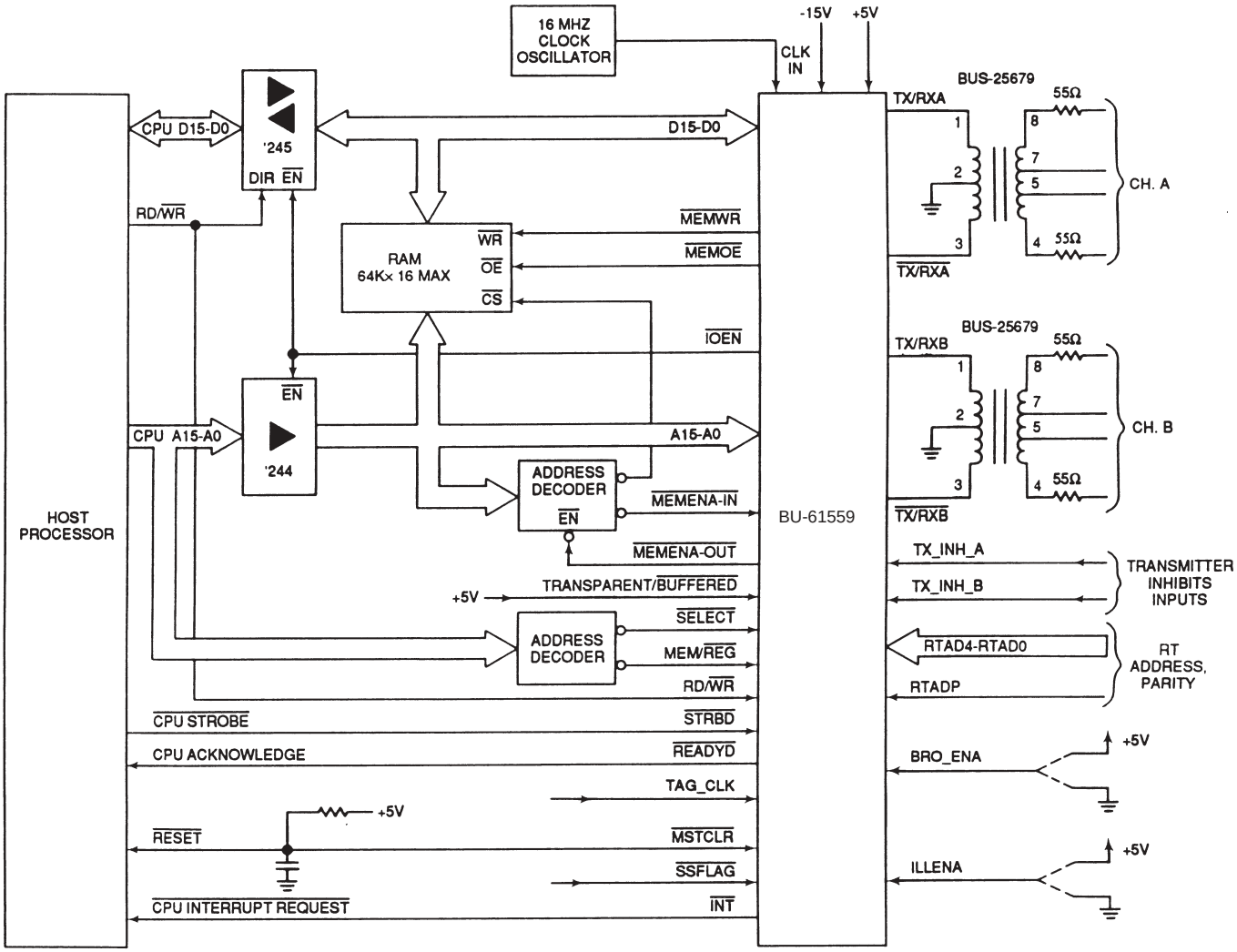
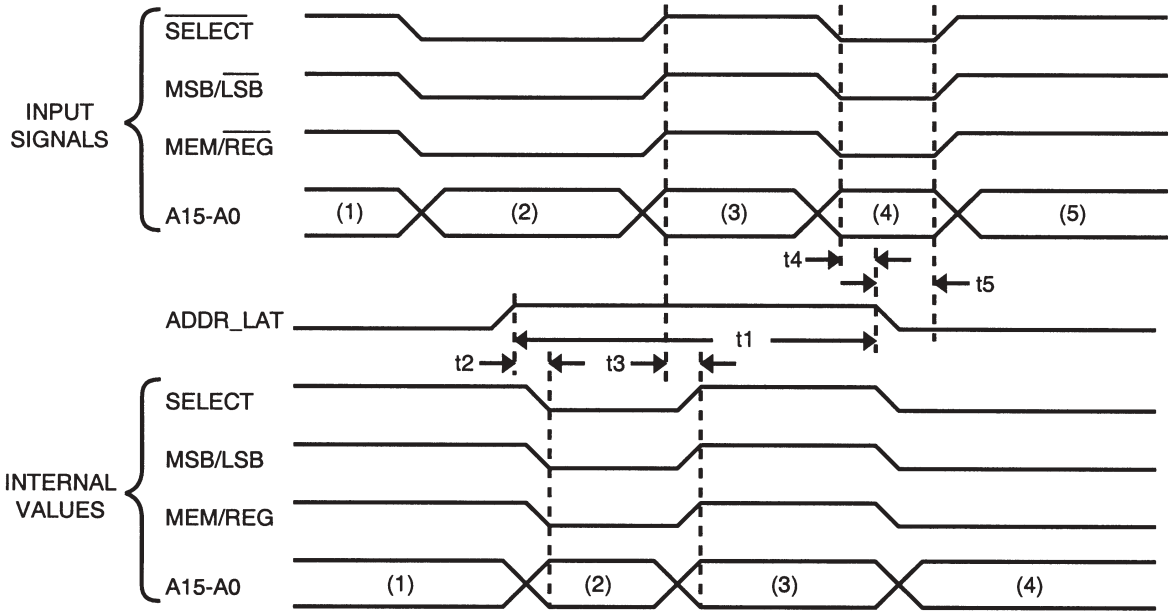


FIGURE 20. BU-61559 INTERCONNECTION DIAGRAM FOR TRANSPARENT MODE

ADDRESS LATCH TIMING (BUFFERED MODE)

FIGURE 21 illustrates the operation and timing of the address input latches for the buffered interface mode. In the transparent mode, the address buffers, and $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$ inputs are always transparent (MSB/$\overline{\text{LSB}}$ not applicable). Since the transparent mode requires the use of external buffers, external address latches would be required to demultiplex a multiplexed address bus. In the buffered mode however, the BU-61559's internal address may be used to perform the demultiplexing function.

The operation of the address latches is controlled by means of the ADDR_LAT input. When ADDR_LAT is high, the latch outputs, which drive the BU-61559's internal memory and control bus, transparently track the state of the address inputs A15 through A00, and the input signals $\overline{\text{SELECT}}$, MSB/$\overline{\text{LSB}}$, and MEM/$\overline{\text{REG}}$. When ADDR_LAT is low, the internal memory and control bus remain latched at the state of A15-A00, $\overline{\text{SELECT}}$, MSB/$\overline{\text{LSB}}$, and MEM/$\overline{\text{REG}}$ just prior to the falling edge of ADDR_LAT.



ADDRESS LATCH TIMING					
REF	DESCRIPTION	BU-61559			UNIT
		MIN	TYP	MAX	
t1	ADDR_LAT pulse width	20			ns
t2	ADDR_LAT high delay to internal signals valid			10	ns
t3	Propagation delay from external input signals to internal signals valid			10	ns
t4	Input setup time prior to falling edge of ADDR_LAT	10			ns
t5	Input hold time following falling edge of ADDR_LAT	20			ns

Notes for FIGURE 21:
1. Applicable to buffered mode only. Address, $\overline{\text{SELECT}}$, and MEM/$\overline{\text{REG}}$ latches are always transparent in the transparent mode of operation.
2. Latches are transparent when ADDR_LAT is high. Internal values do not update when ADDR_LAT is low.
3. MSB/LSB input signal is applicable to 8-bit mode only (16/8 input = logic "0"). MSB/LSB input is a "don't care" for 16-bit operation.

FIGURE 21. ADDRESS LATCH TIMING

PROCESSOR INTERFACE TIMING

FIGURES 22 and 23 illustrate the timing for the host processor to access the BU-61559's internal RAM in buffered mode. FIGURE 22 illustrates the buffered read cycle timing, while FIGURE 23 shows the buffered mode write cycle.

During a CPU transfer cycle, $\overline{\text{STRBD}}$ and $\overline{\text{SELECT}}$ must be sampled low for two consecutive clock cycles when the BU-61559 is **not** accessing the shared RAM. At this time, the output signals $\overline{\text{IOEN}}$ and $\overline{\text{MEMENA-OUT}}$ are asserted low. $\overline{\text{IOEN}}$ is used to enable external address and data tri-state buffers, if required.

$\overline{\text{MEMENA-IN}}$ is the Chip Select ($\overline{\text{CS}}$) input to the BU-61559's internal RAM. In the buffered mode, $\overline{\text{MEMENA-OUT}}$ must be connected directly to $\overline{\text{MEMENA-IN}}$. In the transparent mode, an external address decoder may be used to provide $\overline{\text{MEMENA-IN}}$, as shown in FIGURE 20.

For a read cycle in the transparent mode, the output signal $\overline{\text{MEMOE}}$ is asserted low one-half clock cycle after $\overline{\text{IOEN}}$ goes low. $\overline{\text{MEMOE}}$ will remain low until the end of the read transfer cycle. For a CPU write cycle in transparent mode, the output signal $\overline{\text{MEMWR}}$ is asserted low for one clock cycle (62.5 ns nominal), starting one clock cycle after $\overline{\text{IOEN}}$ is asserted low.

Three clock cycles (nominally 187.5 ns) after $\overline{\text{IOEN}}$ goes low, the BU-61559 will assert the handshake output $\overline{\text{READYD}}$ low. This informs the host processor that read data is available on D15-D0 or that write data has been stored. At this time, the CPU should bring $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ high, completing the transfer cycle.

With two exceptions, the BU-61559 processor interface operation for accessing registers and internal RAM is essentially the same for both the buffered and transparent interface modes. One difference is the operation of the address latch/buffers, as described under the preceding sub-heading. A second difference is that for CPU accesses to external RAM in the transparent mode, the data buffers remain in their high impedance state.

HARDWARE RESET (MSTCLR)

The $\overline{\text{MSTCLR}}$ control input to the BU-61559 provides a hardware reset capability. A negative pulse of 50 ns or more will reset all internal logic of the AIM-HY'er hybrid to its power turn-on or reset idle state. In most systems, $\overline{\text{MSTCLR}}$ is connected to the host processor's power turn-on RESET circuit.

BU-61559 INTERFACE TO STANAG 3910 HIGH-SPEED PROTOCOL CHIP

STANAG 3910 HIGH-SPEED PROTOCOL CHIP

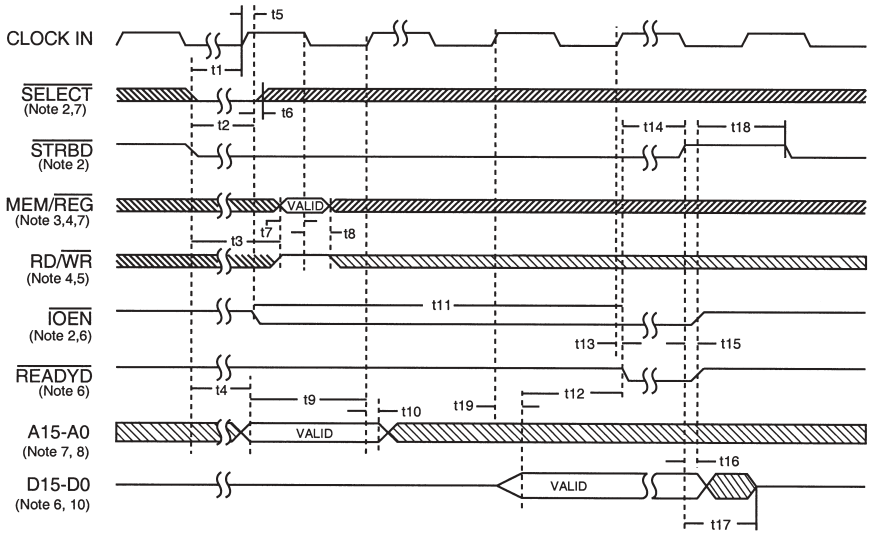
The 1553 BC/RT/MT is comprised of the DDC BU-61559 hybrid and the two BUS-25679 transformers. In this interface, the BU-61559 is configured in the transparent mode, interfacing to the host processor by means of external data and address buffers. This allows a STANAG 3910 High Speed Protocol Chip to monitor all 1553 words being transferred over the BU-61559's parallel data bus, D15-D00.

The STANAG 3910 remote terminal is comprised of a high-speed RT protocol chip, data retiming unit, a 20 MHz fiber optic transceiver, and RAM for high-speed messages. In some implementations, the data retiming unit and fiber optic transceiver may be one component.

In general, The High Speed Protocol Chip operates by monitoring the data bus, as well as various control signal outputs from the BU-61559. The BU-61559 control signals that may be monitored include $\overline{\text{BCSTRCV}}$, $\overline{\text{MSG\_ERROR}}$, $\overline{\text{CMD\_STR}}$, $\overline{\text{RXDTA\_STR}}$, $\overline{\text{TXDTA\_STR}}$, and $\overline{\text{MEMENA-OUT}}$. The High Speed Protocol Chip provides the $\overline{\text{MEMENA-IN}}$ input to the BU-61559.

In the transparent interface mode, Command Words and High-Speed Action Words may be monitored on the BU-61559's external address and data buses. The High Speed Protocol Chip performs all high-speed protocol operations, transmitting and receiving messages over the 3910 fiber optic bus by means of the data retiming unit and fiber optic transceiver.

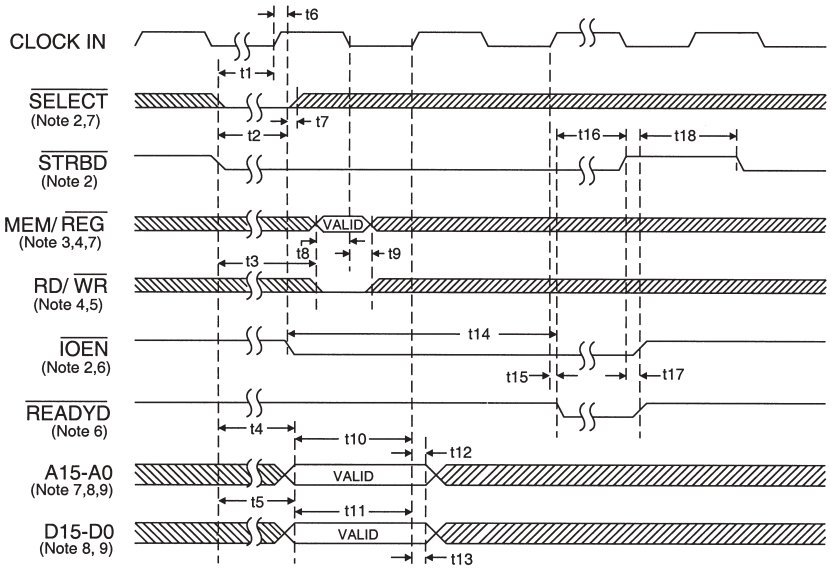
When the BU-61559 receives a transmit command to the High-Speed subaddress, the High Speed Protocol Chip captures the Command Word. The High Speed Protocol Chip is then enabled by the BU-61559's $\overline{\text{MEMENA-OUT}}$ and $\overline{\text{TXDTA\_STR}}$ outputs to provide the High-Speed Status, BIT, and Last Action words over the BU-61559's data bus. When it does this, the High Speed Protocol Chip presents the $\overline{\text{MEMENA-IN}}$ input to the BU-61559 high, de-selecting the BU-61559's internal (or possibly external) RAM. The BU-61559 then responds over the 1553 (3838) bus with the Data Words provided by the High Speed Protocol Chip.



CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE)						
REF	DESCRIPTION	BU-61559			UNIT
		MIN	TYP	MAX	
t1	SELECT and STRBD low setup time prior to clock rising edge (Note 2,10)	20			ns
t2	SELECT and STRBD low to IOEN low (uncontended access) (Notes 2,6) SELECT and STRBD low to IOEN low (contended access) (Notes 2,6)			107.5 2.8	ns ns
t3	MEM/REG and RD/WR setup time following SELECT and STRBD low (Notes 3,4,5,7)			10	ns
t4	Address valid setup time following SELECT and STRBD low.			30	ns
t5	CLOCK IN rising edge delay to IOEN falling edge (Note 6)			35	ns
t6	SELECT hold time following IOEN falling (Note 2)	0			ns
t7	MEM/REG, RD/WR setup time prior to CLOCK IN falling edge (Notes 3,4,5,7)	10			ns
t8	MEM/REG, RD/WR hold time following CLOCK IN falling edge (Notes 3,4,5,7)	30			ns
t9	Address valid setup time prior to CLOCK IN rising edge (Notes 7,8,9)	30			ns
t10	Address hold time following CLOCK IN rising edge (Notes 7,8,9,10)	30			ns
t11	IOEN falling delay to READYD falling (reading RAM) (Notes 6,10) IOEN falling delay to READYD falling (reading registers) (Notes 6,10)	170 170	187.5 187.5	205 205	ns ns
t12	Output Data valid prior to READYD falling (Note 6)	33			ns
t13	CLOCK IN rising edge delay to READYD falling (Note 6)			35	ns
t14	READYD falling to STRBD rising release time.			∞	ns
t15	STRBD rising edge delay to IOEN rising edge and READYD rising edge (Note 6)			30	ns
t16	Output Data hold time following STRBD rising edge.	0			ns
t17	STRBD rising delay to output Data tri-state			40	ns
t18	STRBD high hold time from READYD rising	0			ns
t19	CLOCK IN rising edge delay to Output data valid			60	ns

Notes for FIGURE 22:
1. For the 16-bit buffered nonzero wait configuration, TRANSPARENT/BUFFERED must be connected to logic "0". ZERO_WAIT and DTREQ/16/8 must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. SELECT and STRBD may be tied together. IOEN goes low on the first rising CLK edge when SELECT STRBD is sampled low (satisfying t1) and the BU-61559's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN goes low, starting the transfer cycle. After IOEN goes low, SELECT may be released high.
3. MEM/REG must be presented high for memory access, low for register access.
4. MEM/REG and RD/WR are buffered transparently until the first falling edge of CLK after IOEN goes low. After this CLK edge, MEM/REG and RD/WR become latched internally.
5. The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/WR must be asserted low to read.
6. The timing for IOEN, READYD and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN, READYD, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG and SELECT assumes ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13 through A0 for 61585, 61586, 61582 and 61583, A15 through A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after IOEN goes low. After this CLK edge, A15-A0 become latched internally.
10. Setup time given for use in worst case timing calculations. None of the input signals are required to be synchronized to the system clock. When SELECT and STRBD do not meet the setup time of t1, but occur during the setup window of an internal flip-flop, an additional clock cycle will be inserted between the falling clock edge that latches MEM/REG and RD/WR and the rising clock edge that latches the Address (A15-A0). When this occurs, the pulse width of IOEN falling to READYD falling (t11) increases by one clock cycle and the address hold time (t10) must be increased be one clock cycle.

FIGURE 22. CPU READING RAM (SHOWN FOR BUFFERED MODE)



CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE)					
REF	DESCRIPTION	BU-61559			UNIT
		MIN	TYP	MAX	
t1	SELECT and STRBD low setup time prior to clock rising edge (Note 2,10)	10			ns
t2	SELECT and STRBD low delay to IOEN low (uncontended access) (Notes 2,6) SELECT and STRBD low delay to IOEN low (contended access) (Notes 2,6)			107.5 2.8	ns ns
t3	MEM/REG and RD/WR setup time following SELECT and STRBD low (Notes 3,4,5,7)			10	ns
t4	Address valid setup time following SELECT and STRBD low.			30	ns
t5	Input Data Valid setup time following SELECT and STRBD low.			50	ns
t6	CLOCK IN rising edge delay to IOEN falling edge (Note 6)			35	ns
t7	SELECT hold time following IOEN falling (Note 2)	10			ns
t8	MEM/REG, RD/WR setup time prior to CLOCK IN falling edge (Notes 3,4,5,7)	30			ns
t9	MEM/REG, RD/WR hold time following CLOCK IN falling edge (Notes 3,4,5,7)	30			ns
t10	Address valid setup time prior to CLOCK IN rising edge (Notes 7,8,9)	30			ns
t11	Input Data valid setup time prior to CLOCK IN rising edge	10			ns
t12	Address valid hold time following CLOCK IN rising edge (Notes 7,8,9,10)	30			ns
t13	Input Data valid hold time following CLOCK IN rising edge (Notes 9,10)	30			ns
t14	IOEN falling delay to READYD falling (Notes 6,10)	170	187.5	205	ns
t15	CLOCK IN rising edge delay to READYD falling (Note 6)			35	ns
t16	READYD falling to STRBD rising release time.			∞	ns
t17	STRBD rising edge delay to IOEN rising edge and READYD rising edge (Note 6)			30	ns
t18	STRBD valid high hold time from READYD rising edge	0			ns

Notes for FIGURE 23:
1. For the 16-bit buffered nonzero wait configuration TRANSPARENT/BUFFERED must be connected to logic "0". ZERO_WAIT* and DTREQ/16/8 must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. SELECT and STRBD may be tied together. IOEN goes low on the first rising CLK edge when SELECT STRBD is sampled low (satisfying t1) and the BU-61559's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN goes low, starting the transfer cycle. After IOEN goes low, SELECT may be released high.
3. MEM/REG must be presented high for memory access, low for register access.
4. MEM/REG and RD/WR are buffered transparently until the first falling edge of CLK after IOEN goes low. After this CLK edge, MEM/REG and RD/WR become latched internally.
5. The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/WR must be asserted high to write.
6. The timing for IOEN and READYD outputs assumes a 50 pf load. For loading above 50 pf, the validity of IOEN and READYD is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG, and SELECT assumes ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13 through A0 for 61585, 61586, 61582, and 61583 and A15 through A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after IOEN goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.
10. Setup time given for use in worst case timing calculations. None of the input signals are required to be synchronized to the system clock. When SELECT and STRBD do not meet the setup time of t1, but occur during the setup time of an internal flip-flop, an additional clock cycle will be inserted between the falling clock edge that latches MEM/REG and RD/WR and the rising clock edge that latches the address (A15-A0) and data (D15-D0). When this occurs, the pulse width of IOEN falling to READYD falling (t14) increases by one clock cycle and the address and data hold time (t12+t13) must be increased by one clock cycle.

FIGURE 23. CPU WRITING RAM (SHOWN FOR BUFFERED MODE)

TABLE 7. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS

POWER AND GROUND (8)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
+5V Logic	14	27	Logic +5V Supply
Logic Gnd	21	78	Logic Ground
-15/-12VA	39	42	CH. A -15V/-12V Supply
+5VA	77	43	CH. A +5V Supply
GndA	38	44	CH. A Transceiver Ground
-15/-12VB	18	35	CH. B -15V/-12V Supply
+5VB	58	36	CH. B +5V Supply
GndB	19	37	CH. B Transceiver Ground

DATA BUS (16)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
D15 (MSB)	48	16	16-bit bidirectional data bus. This bus is used for interfacing the host processor to the internal registers and 8K words of RAM. In addition, in the transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K X 16 of external RAM. Most of the time, the outputs for D15 through D0 are in their high impedance state. They drive outward when the host CPU reads the internal RAM or registers, or when the protocol /memory management logic is accessing (either reading or writing) internal RAM or writing to external RAM when in the transparent mode. D15-D0 assume their high-impedance states following power turn-on reset.
D14	8	15	
D13	47	14	
D12	7	13	
D11	46	12	
D10	6	11	
D9	45	10	
D8	5	9	
D7	44	8	
D6	4	7	
D5	43	6	
D4	3	5	
D3	42	4	
D2	2	3	
D1	41	2	
D0 (LSB)	1	1	

ADDRESS BUS (16)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
A15 (MSB)	29	62	16-bit bidirectional address bus. In both the buffered and transparent modes, the host CPU accesses the BU-61559 registers and 8K words of internal RAM by means of A12 through A0. In the transparent mode, A15-A0 drive outward (towards the CPU) in order for the 1553 protocol/memory management logic to access up to 64K X 16 of external RAM. Most of the time, including immediately after power turn-on RESET, the A15-A0 outputs will be in their disabled (high impedance) state.
A14	67	63	
A13	28	64	
A12	66	65	
A11	27	66	
A10	65	67	
A9	26	68	
A8	64	69	
A7	25	70	
A6	63	71	
A5	24	72	
A4	62	73	
A3	23	74	
A2	61	75	
A1	22	76	
A0 (LSB)	60	77	

TABLE 7. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS (CONT)

PROCESSOR INTERFACE (8)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
TRANSPARENT/ BUFFERED	35	50	Used to select between the transparent (when strapped to logic 1) and buffered (when strapped to logic 0) modes for the host processor interface.
STRBD (I)	34	52	Strobe Data. Used in conjunction with SELECT to initiate and control the data transfer cycle between the host processor and the BU-61559.
SELECT (I)	74	49	Generally connected to a CPU address decoder output to select the BU-61559 for a transfer to/from either RAM or register. May be tied to STRBD.
MEM/REG (I)	33	54	Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access (MEM/REG = 1) or register access (MEM/REG = 0).
RD/WR (I)	36	48	Read/Write. For a host processor access, selects between reading (RD/WR = 1) and writing (RD/WR = 0).
IOEN (O)	73	51	Tri-state control for external address and data buffers. Generally not needed in the buffered mode. When low, external buffers should be enabled to allow the host processor access to the BUS-61669's RAM and registers.
READYD (O)	75	47	Handshake output to host processor. For a read access, signals that data is available to be read on D15 through D0. For a write cycle, signals that data has been transferred to a register or RAM location.
INT (O)	72	53	Interrupt request output. If the LEVEL/PULSE interrupt bit (bit 3) of Configuration Register #2 is low, a negative pulse of approximately 500 ns in width is output on INT. If bit 3 is high, a low level interrupt request output will be asserted on INT.

MEMORY INTERFACE AND ADDRESS LATCH CONTROL (4)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
MEMENA-OUT (O)	31	58	Asserted low during both host processor and 1553 protocol/memory management memory transfer cycles. Used as a memory chip select (CS) signal for external RAM in the transparent mode.
MEMENA-IN (I)	69	59	Chip Select (CS) input to 8K X 16 of internal shared RAM. If only internal RAM is used (always the case in the buffered mode), connect directly to MEMENA-OUT.
MEMOE (O)/ ADDR_LAT (I),	30	60	Memory Output Enable/Address Latch. In transparent mode, output used to enable data outputs for external RAM read cycles. In buffered mode, input used to configure the internal address buffers in latched mode (when low) or transparent mode (when high).
MEMWR (O)	68	61	Memory Write. Asserted low during memory write transfers to strobe data into internal or external RAM. Used in transparent mode.

1553 ISOLATION TRANSFORMER INTERFACE (4)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
TX/RX-A (I/O)	40	40	Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers.
TX/RX-A (I/O)	78	41	
TX/RX-B (I/O)	20	39	
TX/RX-B (I/O)	59	38	

RT ADDRESS (6)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
RTAD4 (MSB) (I)	11	21	Remote Terminal Address Inputs
RTAD3 (I)	49	18	
RTAD2 (I)	50	20	
RTAD1 (I)	9	17	
RTAD0 (MSB) (I)	10	19	
RTAD (I)	51	22	Remote Terminal Address Parity. Must provide odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands.

TABLE 7. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS (CONT)

MISCELLANEOUS (16)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
CLOCK IN (I)	32	56	16 MHz clock input.
$\overline{\text{MSTCLR}}$ (I)	71	55	Master Clear. Negative true Reset input, normally asserted low following power turn-on.
$\overline{\text{INCMD}}$ (O)	70	57	In Command. In BC mode, asserted low throughout processing cycle for each message. In RT mode, asserted low following receipt of Command Word and kept low until completion of current message sequence. In Monitor mode, goes low following MONITOR START command, kept low while monitor is on-line, goes high following RESET command.
TX_INH_A (I)	76	45	The 1553 Channel A and/or Channel B transmitters may be inhibited by asserting the respective TX_INH input(s) high. *
TX_INH_B (I)	57	34	
$\overline{\text{SSFLAG}}$ (I)	37	46	If this input is asserted low the Subsystem Flag bit will be set in the BU-61559's RT Status Word. A low on the $\overline{\text{SSFLAG}}$ input overrides a logic “1” of the respective bit (bit 8) of Configuration Register #1.
MSG_ERR (O)	12	23	In BC or RT modes, this output will be asserted as a low level following a word or format error and remain low until the start of the next message.
$\overline{\text{CMD\_STR}}$ (O)	13	25	In RT/transparent mode, this output will pulse low for nominally 62.5 ns (signal is one clock cycle wide) and occurs in the middle of the transfer cycle, coincident with the $\overline{\text{MEMWR}}$ pulse for writing the command word to RAM.
$\overline{\text{RX\_DTA\_STR}}$ (O)	52	24	In RT/transparent mode, this output will pulse low for nominally 62.5 ns (signal is one clock cycle wide) and occurs during the third of four clock cycles during a data word write cycle, in the same time frame that $\overline{\text{MEMWR}}$ writes the received data word to RAM.
$\overline{\text{TX\_DTA\_STR}}$ (O)	53	26	In RT/transparent mode, this output will pulse low for nominally 62.5 nsec (signal is one clock cycle wide) and occurs during the third of four clock cycles during a data word read cycle.

* The operation of the TX_INH_A/B inputs also effects the operation of the BC off-line self test. If the inhibit is high when an off-line BC self test is run, a “loop test” failure will occur.

MISCELLANEOUS (16) (CONT)			
SIGNAL NAME	PIN NO.		DESCRIPTION
	DIP	FLAT	
BRO_ENA (I)	54	28	Broadcast Enable. If connected to logic 1, the BU-61559 will recognize RT Address 31 as the broadcast address. If connected to logic 0, RT Address 31 may be used as a discrete RT address.
$\overline{\text{BCSTRCV}}$ (O)	16	31	Broadcast Command received is an active low signal that occurs 1.35 to 2.25 µs following the mid-parity bit crossing of a received broadcast command word that remains low until receipt of a subsequent command word to the BU-61559's own RT address.
ILLENA (I)	17	33	Illegalization Enable. If connected to logic 1, designates shared RAM addresses 0300-03FF to be dedicated for command illegalization in RT mode. If set to logic 0, illegalization is disabled and addresses 0300-03FF may be used for stack or message data. Has no effect in BC or MT modes.
TAG_CLK (I)	15	29	External Time Tag Clock input. For BC/RT modes. Use may be designated by means of Configuration Register # 2. If not used, should be connected to +5V or ground.
$\overline{\text{RT\_FAIL}}$ (O)	55	30	In RT mode, is updated following every valid, nonbroadcast message. Will be asserted low if the RT fails its loopback test (invalid or mismatch to last transmitted word) or if a 768 µs timeout condition occurs. Cleared by reset or as a result of next valid, non-broadcast message.
$\overline{\text{RTFLAG}}$ (I)	56	32	Active low input used to control $\overline{\text{RT FLAG}}$ bit in RT Status Word. If $\overline{\text{RTFAIL}}$ is low, the RT $\overline{\text{FLAG}}$ bit will be set. May be connected to $\overline{\text{RTFAIL}}$.

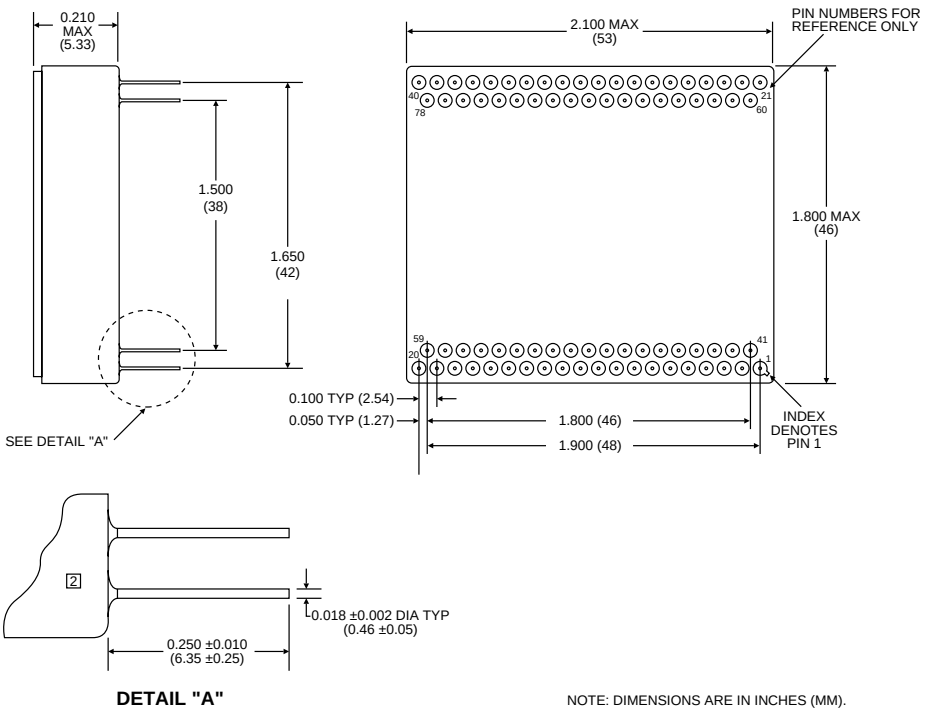


FIGURE 24. BU-61559D MECHANICAL OUTLINE (78-PIN CERAMIC DDIP)

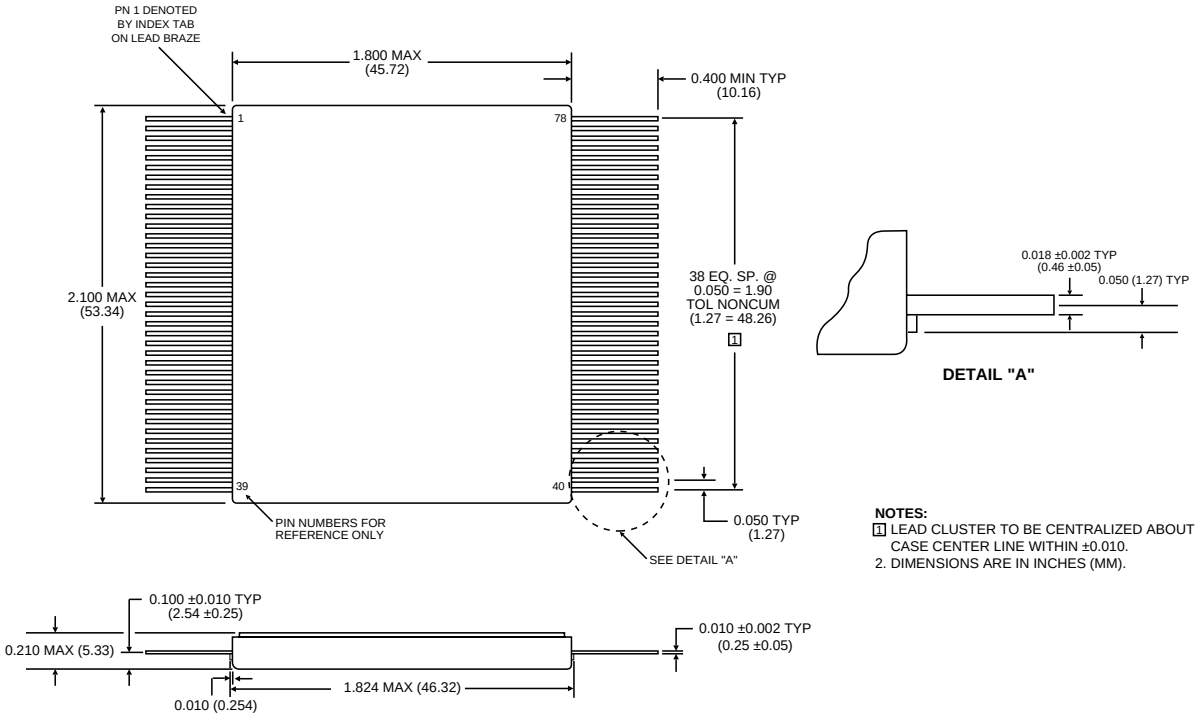


FIGURE 25. BU-61559F MECHANICAL OUTLINE (78-PIN CERAMIC FLAT PACK)

ORDERING INFORMATION

BU-61559XX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = Standard Testing

Process Requirements:
- 0 = Standard DDC practices, no Burn-In
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

Temperature Range/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 6 = Custom Part (Reserved)
- 7 = Custom Part (Reserved)
- 8 = 0°C to +70°C with Variables Test Data

Voltage Requirements:
- 1 = +5 Volts and -15 Volts
- 2 = +5 Volts and -12 Volts

Package:
- D = 78-pin Ceramic QIP
- F = 78-pin Ceramic Flat Pack

Product Type:
- BU-61559 = AIM HY'er

* Standard DDC processing with burn-in and full temperature test. See table below.

STANDARD DDC PROCESSING

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

NOTES:

NOTES:

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