Chapter 1

Introduction to the TMS370 Family Devices

This chapter discusses the key features and major components of the TMS370 family of microcontrollers. The chapter concludes with block diagrams for each device category.

This chapter covers the following topics:

Topic **Page**

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1.1 Overview

The TMS370 family consists of VLSI, 8-bit, CMOS microcontrollers with on-chip EEPROM storage and peripheral support functions. These devices offer superior performance in complex, real-time control applications in demanding environments and are available in mask-programmable ROM and EPROM. Moreover, you have a wide range of options to choose from in deciding the most economical and efficient manner for getting a product to market faster.

In an effort to continually improve its products, Texas Instruments has added new, more robust features to the TMS370 family of devices. These features are designed to enhance performance and enable new application technologies. The improved features include new watchdog modes and low-power modes for mask-ROM devices. And, all family members are software compatible, so you can run many existing applications on the improved devices without having to modify your software. (Refer to Appendix A for more information about compatibility.)

In expanding its powerful TMS370 family of microcontrollers, TI offers many new configurable devices for specific applications. As microcontrollers have evolved, TI has added multiple peripheral functions to chips that originally had only a CPU, memory, and I/O blocks. Now, with the high-performance, software-compatible TMS370 microcontrollers, you can choose from over 40 standard products. Or, you can use up to 16 function modules to configure your new device quickly, easily, and cost effectively for your application.

The TMS370 family is fully supported by TI development tools that facilitate simplified software development for quicker market introduction of new products. These tools include an assembler, an optimizing C compiler, a linker, a C source debugger, a design kit, and an EEPROM/EPROM programmer. All of these tools work together using a DOS-based personal computer (PC) as the host and central control element. This allows you to select the host computer and text management as well as editing tools according to your system requirements.

Additionally, the TMS370 in-circuit emulator (XDS—eXtended Development Support) allows you to immediately begin designing, testing, and debugging your system upon specification. The reason for this is straightforward: the emulator itself is modular and configurable, eliminating the need to produce a complete, new emulator for each TMS370 configuration.

Typical Applications

The TMS370 family of devices is the ideal choice for applications like these:

Application Area	Applications	
Automotive	Climate control systems Cruise control Entertainment systems Instrumentation	Navigational systems Engine control Antilock braking
Computer	Keyboards Peripheral interface control	Disk controllers Terminals
Industrial	Motor control Temperature controllers Process control	Meter control Medical instrumentation Security systems
Telecommunications	Modems Intelligent phones Intelligent line card control	Telecopiers Debit cards

Device Categories

The TMS370 family of devices is divided into five categories (see Table 1–1). Each category is supported by development tools that include the in-circuit emulators, a C compiler, an assembler, a linker, and a C source debugger.

Table 1–1. TMS370 Family Categories and Their Corresponding Devices

Category	Devices Included		
TMS370Cx1x	TMS370C010 TMS370C310	TMS370C311 TMS370C610	TMS370C710 SE370C710†
TMS370Cx2x	TMS370C020 TMS370C022 TMS370C320	TMS370C322 TMS370C622	TMS370C722 SE370C722†
TMS370Cx3x	TMS370C032 TMS370C332	TMS370C732 SE370C732†	
TMS370Cx4x	TMS370C040 TMS370C042 TMS370C340	TMS370C342 TMS370C642	TMS370C742 SE370C742†
TMS370Cx5x	TMS370C050 TMS370C150 TMS370C250 TMS370C350 TMS370C052 TMS370C352	TMS370C056 TMS370C156 TMS370C256 TMS370C356 TMS370C756	TMS370C058 TMS370C358 TMS370C758 SE370C756† SE370C758†

† These system evaluators and development tools are used only in a prototype environment. Their reliability has not been characterized.

1.2 Key Features

The TMS370 family of devices has the following key features:

- ❑ **Series of compatible devices** that supports software migration
- ❑ **CMOS EPROM technology** that provides EPROM for reprogrammable and OTP (one-time programmable) program memory to be used as prototypes and for small-volume or quick-turn production
- ❑ **CMOS EEPROM technology** that provides EEPROM programming with a single 5-volt supply
- ❑ **A/D technology** that converts analog signals to digital values
- ❑ **Static RAM/registers** that offer numerous memory options
- ❑ **Flexible operating features:**
  - Power reduction standby and halt modes
  - -40°C to 85°C operating temperature
  - 2-MHz to 20-MHz input clock frequency
  - 5V ±10%
- ❑ **Flexible interrupt handling** for design flexibility:
  - Two programmable interrupt levels
  - Programmable rising or falling edge detect
- ❑ **System integrity features** that increase flexibility during the software development phase with:
  - Oscillator fault detection
  - Privileged mode lockout
  - Watchdog timer
- ❑ **Memory-mapped ports** for easy addressing
- ❑ An **optimizing C compiler** that translates ANSI C programs into '370 assembly language source
- ❑ A **high-level language debugger** that lets you refine and correct code
- ❑ A **modular library** for quick turns to different configurations
- ❑ **Fourteen addressing modes** that use eight formats, including:
  - Register-to-register arithmetic
  - Indirect addressing
  - Indexed and indirect branches and calls
- ❑ **250-mA typical latch-up immunity at 25°C**
- ❑ **ESD protection** that exceeds 2,000 V per MIL-STD-883C method 3015

1.3 Major Components of the TMS370 Architecture

In addition to the features listed in Section 1.2, the TMS370 family members have the following architectural features, according to the device category.

CPU

The TMS370 8-bit CPU has a status register, program counter register, and stack pointer. The CPU uses the register file as working registers, accessed on the internal bus in one bus cycle. The 8-bit internal bus also allows access to memory and the peripheral interfaces. TMS370Cx5x devices allow external memory expansion through ports A, B, C, and D.

Refer to Chapter 3, *CPU and Memory Organization*, for more information about the CPU.

Register File

The register file is located at the beginning of the TMS370 memory map. Register-access instructions in the TMS370 instruction set allow access to any of the first 256 registers (if available) in one bus cycle. This segment of the memory map is used as general-purpose RAM and the stack.

Chapter 3, *CPU and Memory Organization*, provides additional information about the register file.

RAM

RAM modules other than those contained in the register file are mapped after the register file. The TMS370 accesses this RAM in two cycles.

Memory is discussed in full in Chapter 3, *CPU and Memory Organization.*

Data EEPROM

The data EEPROM modules provide in-circuit programmability and data retention in power-off mode. The modules contain 256 or 512 bytes of EEPROM. This memory is useful for constants and infrequently changed variables required by the application program. The EEPROM can be programmed and erased by using available EEPROM programmers or by the TMS370 itself under program control.

The data EEPROM modules are discussed in Chapter 6, *EPROM and EEPROM Modules.*

Program Memory

The program memory provides alternatives to meet the needs of your application. The program memory modules presently contain 2K, 4K, 8K, 16K, or 32K bytes of memory. The program memory in TMS370C7xx, TMS370C6xx, and SE370C7xx devices is EPROM. EPROM can be programmed, erased, and reprogrammed for prototyping (in a ceramic package). EPROM devices that do not have a window (in a plastic package) are one-time programmable (OTP) devices, used for small production runs. In TMS370C0xx and TMS370C3xx devices, the program memory is mask ROM programmed at the factory.

Program memory is discussed in Chapter 6, *EPROM and EEPROM Modules.*

Input/Output Ports

- **TMS370Cx1x** devices have two ports: ports A and D. Port A is an 8-bit wide port, while port D is a 5-bit wide port. Both of these ports can be programmed, bit by bit, to function as either a digital input or a digital output.
- **TMS370Cx2x** devices have four ports: ports A, B, C, and D. Ports A and B are 8-bit wide ports, port C is a 1-bit wide port, and port D is a 5-bit wide port. Each of these ports can be programmed, bit by bit, to function as either a digital input or a digital output.
- **TMS370Cx3x** devices have two ports: ports A and D. Port A is an 8-bit wide port, while port D is a 4-bit wide port. Both of these ports can be programmed, bit by bit, to function as either a digital input or a digital output.
- **TMS370Cx4x** devices have three ports: ports A, B, and D. Port A is an 8-bit wide port, port B is a 3-bit wide port, and port D is a 5-bit wide port. Each of these ports can be programmed, bit by bit, to function as either a digital input or a digital output.
- **TMS370Cx5x** devices have four 8-bit ports: ports A, B, C, and D (port D for the 64-pin devices has only 6 pins). These ports can be configured by the software as the data, control, and address lines for external memory. Any bits not needed for external memory can be programmed to be either a digital input or a digital output.

I/O ports are discussed in greater detail in Chapter 4, *System and Digital I/O Configuration.*

Timer 1 and Timer 2

Timers 1 and 2 are 16-bit timers that can be configured in the following ways:

- Programmable 8-bit prescaler that determines the independent clock sources for the general-purpose timer and the watchdog timer
- 16-bit event timer, to keep a cumulative total of the transitions

- ❑ 16-bit pulse accumulator, to measure the pulse input width
- ❑ 16-bit input-capture function that latches the counter value on the occurrence of an external input
- ❑ Two 16-bit compare registers that trigger when the counter matches the contents of a compare register
- ❑ Self-contained PWM (pulse-width modulated) output control function

The results of these operations can generate an interrupt to the CPU, set flag bits, reset the timer counter, toggle an I/O line, or generate PWM outputs. These timers provide up to 200 ns of resolution at 20 MHz.

Timers 1 and 2 are discussed fully in Chapters 7 and 8, respectively.

Watchdog Timer

The watchdog timer helps ensure system integrity. It can be programmed to generate a hardware reset when it times out. This function provides a hardware monitor over the software to avoid losing a program. If not needed as a watchdog, this timer can be used as a general-purpose timer.

For more information about the watchdog timer, refer to Section 7.7, page 7-17.

PACT (Programmable Acquisition and Control Timer)

The PACT module is a programmable timing module that uses some of the on-chip RAM to store its commands as well as the timer values. The module offers the following:

- ❑ Input capture on up to six pins, four of which may have a programmable prescaler
- ❑ One input capture pin that can drive an 8-bit event counter
- ❑ Up to 8 timer-driven outputs
- ❑ Timer capability of up to 20 bits
- ❑ Interaction between event counter and timer activity
- ❑ Eighteen independent interrupt vectors to allow better servicing of events
- ❑ Watchdog with selectable time-out period
- ❑ Mini-SCI (serial communications interface), which works as a full duplex UART (universal asynchronous receiver transmitter)

Once set up, the PACT requires no CPU overhead, except to service interrupts. The PACT module is discussed in full in Chapter 12, *Programmable Acquisition and Control Timer (PACT).*

SCI (Serial Communications Interface)

The SCI module is a built-in serial interface that offers the following features:

- Programmable to be asynchronous (up to 156K bits/s) or isosynchronous (up to 2.5 Mbits/s)
- Full duplex, double-buffered Rx and Tx
- Programmable format with error-checking capabilities

The SCI module programs and controls all timing, data format, and protocol factors. The CPU takes no part in the serial communications except to write data transmitted to registers in the SCI and to read received data from registers in the SCI when interrupted.

The SCI module is described fully in Chapter 9, *Serial Communications Interface (SCI) Module.*

SPI (Serial Peripheral Interface)

The SPI module is a built-in serial interface that facilitates communication between the network master, slave CPUs, and external peripheral devices. It provides synchronous data transmission up to 2.5 Mbits/s. Like the SCI, the SPI is set up by software. After that, the CPU takes no part in timing, data format, or protocol. Also, like the SCI, the CPU reads and writes to memory-mapped registers to receive and transmit data. An SPI interrupt alerts the CPU when received data is ready.

The SPI module is described fully in Chapter 10, *Serial Peripheral Interface (SPI) Module.*

A/D (Analog-to-Digital) Converter

The 8-bit analog-to-digital converter module performs successive approximation and offers four channels in 40-pin packages and eight channels in 44-pin, 64-pin, and 68-pin packages. The reference source and input channel are selectable. You can program the conversion result to be the ratio of the input voltage to the reference voltage or the ratio of one analog input to another. Input lines that are not required for A/D conversion can be programmed to be digital input lines.

The A/D converter module is described in greater detail in Chapter 11, *Analog-to-Digital Converter Module.*

1.4 Summary of Components by Device

The major components of the TMS370 family devices (discussed in Section 1.3) are summarized in Table 1–2 by device.

Table 1–2. TMS370 Family Architecture Summary

Type	Device	Program Memory (bytes)		Data Memory (bytes)		Off-Chip Memory Expansion (bytes)	Serial Interface Modules†	Timer Modules‡	A/D Channels
		ROM	EPROM	EEPROM	RAM				
ROM	TMS370C010	4K	—	256	128	—	SPI	T1	—
	TMS370C020	4K	—	256	256	—	SPI/SCI	T1	—
	TMS370C040	4K	—	256	256	—	SCI	T1/T2	4/8§
	TMS370C050	4K	—	256	256	112K	SPI/SCI	T1/T2	8
	TMS370C022	8K	—	256	256	—	SPI/SCI	T1	—
	TMS370C032	8K	—	256	256	—	PACT/SCI	PACT	8
	TMS370C042	8K	—	256	256	—	SCI	T1/T2	4/8§
	TMS370C052	8K	—	256	256	112K	SPI/SCI	T1/T2	8
	TMS370C056	16K	—	512	512	112K	SPI/SCI	T1/T2	8
	TMS370C058	32K	—	256	1K	—	SPI/SCI	T1/T2	8
	TMS370C311	2K	—	—	128	—	SPI	T1	—
	TMS370C310	4K	—	—	128	—	SPI	T1	—
	TMS370C320	4K	—	—	256	—	SPI/SCI	T1	—
	TMS370C340	4K	—	—	256	—	SCI	T1/T2	4/8§
	TMS370C350	4K	—	—	256	112K	SPI/SCI	T1/T2	8
	TMS370C322	8K	—	—	256	—	SPI/SCI	T1	—
	TMS370C332	8K	—	—	256	—	PACT/SCI	PACT	8
	TMS370C342	8K	—	—	256	—	SCI	T1/T2	4/8§
	TMS370C352	8K	—	—	256	112K	SPI/SCI	T1/T2	8
	TMS370C356	16K	—	—	512	112K	SPI/SCI	T1/T2	8
	TMS370C358	32K	—	—	1K	—	SPI/SCI	T1/T2	8
ROM-less¶	TMS370C150	—	—	—	256	56K	SPI/SCI	T1/T2	8
	TMS370C250	—	—	256	256	56K	SPI/SCI	T1/T2	8
	TMS370C156	—	—	—	512	56K	SPI/SCI	T1/T2	8
	TMS370C256	—	—	512	512	56K	SPI/SCI	T1/T2	8
OTP#	TMS370C610	—	4K	—	128	—	SPI	T1	—
	TMS370C622	—	8K	—	256	—	SPI/SCI	T1	—
	TMS370C642	—	8K	—	256	—	SCI	T1/T2	4/8§
	TMS370C710	—	4K	256	128	—	SPI	T1	—
	TMS370C722	—	8K	256	256	—	SPI/SCI	T1	—
	TMS370C732	—	8K	256	256	—	PACT/SCI	PACT	8
	TMS370C742	—	8K	256	256	—	SCI	T1/T2	4/8§
	TMS370C756	—	16K	512	512	112K	SPI/SCI	T1/T2	8
	TMS370C758	—	32K	256	1K	—	SPI/SCI	T1/T2	8
SE*	SE370C710	—	4K	256	128	—	SPI	T1	—
	SE370C722	—	8K	256	256	—	SPI/SCI	T1	—
	SE370C732	—	8K	256	256	—	PACT/SCI	PACT	8
	SE370C742	—	8K	256	256	—	SCI	T1/T2	4/8§
	SE370C756	—	16K	512	512	112K	SPI/SCI	T1/T2	8
	SE370C758	—	32K	256	1K	—	SPI/SCI	T1/T2	8

† PACT module has a mini-SCI port.
‡ Timer module includes a watchdog timer that you can program to serve as a general-purpose 16-bit timer. The PACT module includes a watchdog timer.
§ Eight channels for 44-pin device or four channels for 40-pin device.
¶ In ROMless (microprocessor) mode, all address, data, and control lines are fixed as their function.
# For OTP (PLCC) availability information, contact your local TI sales office or distributor.
* System evaluator (reprogrammable EPROM)—for use in prototype environment only.

Table 1–2. TMS370 Family Architecture Summary (Continued)

Type	Device	Interrupts/Reset			I/O Pins	No. of Pins/Package◊□
		External	Vectors Total	Sources Total		
ROM	TMS370C010	4	6	13	22	28 DIP/PLCC
	TMS370C020	4	8	16	34	40 DIP/SDIP I 44 PLCC
	TMS370C040	4	9	22	32/36	40 DIP/SDIP I 44 PLCC
	TMS370C050	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C022	4	8	16	34	40 DIP/SDIP I 44 PLCC
	TMS370C032	4	23	25	36	44 PLCC
	TMS370C042	4	9	22	32/36	40 DIP/SDIP I 44 PLCC
	TMS370C052	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C056	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C058	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C311	4	6	13	22	28 DIP/PLCC
	TMS370C310	4	6	13	22	28 DIP/PLCC
	TMS370C320	4	8	16	34	40 DIP/SDIP I 44 PLCC
	TMS370C340	4	9	16	32/36	40 DIP/SDIP I 44 PLCC
	TMS370C350	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C322	4	8	16	34	40 DIP/SDIP I 44 PLCC
	TMS370C332	4	23	25	36	44 PLCC
	TMS370C342	4	9	22	32/36	40 DIP/SDIP I 44 PLCC
	TMS370C352	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C356	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C358	4	10	23	55/53	68 PLCC I 64 SDIP
ROM-less¶	TMS370C150	4	10	23	55	68 PLCC
	TMS370C250	4	10	23	55	68 PLCC
	TMS370C156	4	10	23	55	68 PLCC
	TMS370C256	4	10	23	55	68 PLCC
OTP#	TMS370C610	4	6	13	22	28 DIP/PLCC
	TMS370C622	4	8	16	34	40 DIP/SDIP I 44 PLCC
	TMS370C642	4	9	22	32/36	40 DIP/SDIP I 44 PLCC
	TMS370C710	4	6	13	22	28 DIP/PLCC
	TMS370C722	4	8	16	34	40 DIP/SDIP I 44 PLCC
	TMS370C732	4	23	25	36	44 PLCC
	TMS370C742	4	9	22	32/36	40 DIP/SDIP I 44 PLCC
	TMS370C756	4	10	23	55/53	68 PLCC I 64 SDIP
	TMS370C758	4	10	23	55/53	68 PLCC I 64 SDIP
SE☆	SE370C710	4	6	13	22	28 CDIP/CLCC
	SE370C722	4	8	16	34	40 CSDIP/CDIP I 44 CLCC
	SE370C732	4	23	25	36	44 CLCC
	SE370C742	4	9	22	32/36	40 CSDIP/CDIP I 44 CLCC
	SE370C756	4	10	23	55/53	68 CLCC I 64 CSDIP
	SE370C758	4	10	23	55/53	68 CLCC I 64 CSDIP

¶ In ROM-less (microprocessor) mode, all address, data, and control lines are fixed as their function.
# For OTP (PLCC) availability information, contact your local TI sales office or distributor.
☆ System evaluator (reprogrammable EPROM)—for use in prototype environment only.
□ Refer to Table 17–1, page 17-6 for package type acronyms.
◊ 64-pin devices do not support off-chip memory expansion.

1.5 Device Block Diagrams

The TMS370 family is based on a register-to-register architecture, which allows access to a register file (up to 256 bytes) in a single bus cycle. On-chip memory includes program memory (mask ROM or EPROM), static RAM, and data EEPROM.

The versatile on-chip peripheral functions include (depending on the specific member of the series) an analog-to-digital converter (A/D), a serial communications interface (SCI), a serial peripheral interface (SPI), three different timer modules, and up to 55 digital input/output pins.

Figure 1–1 is a block diagram of the TMS370Cx1x devices, showing the major functional blocks.

Figure 1–1. TMS370Cx1x Block Diagram

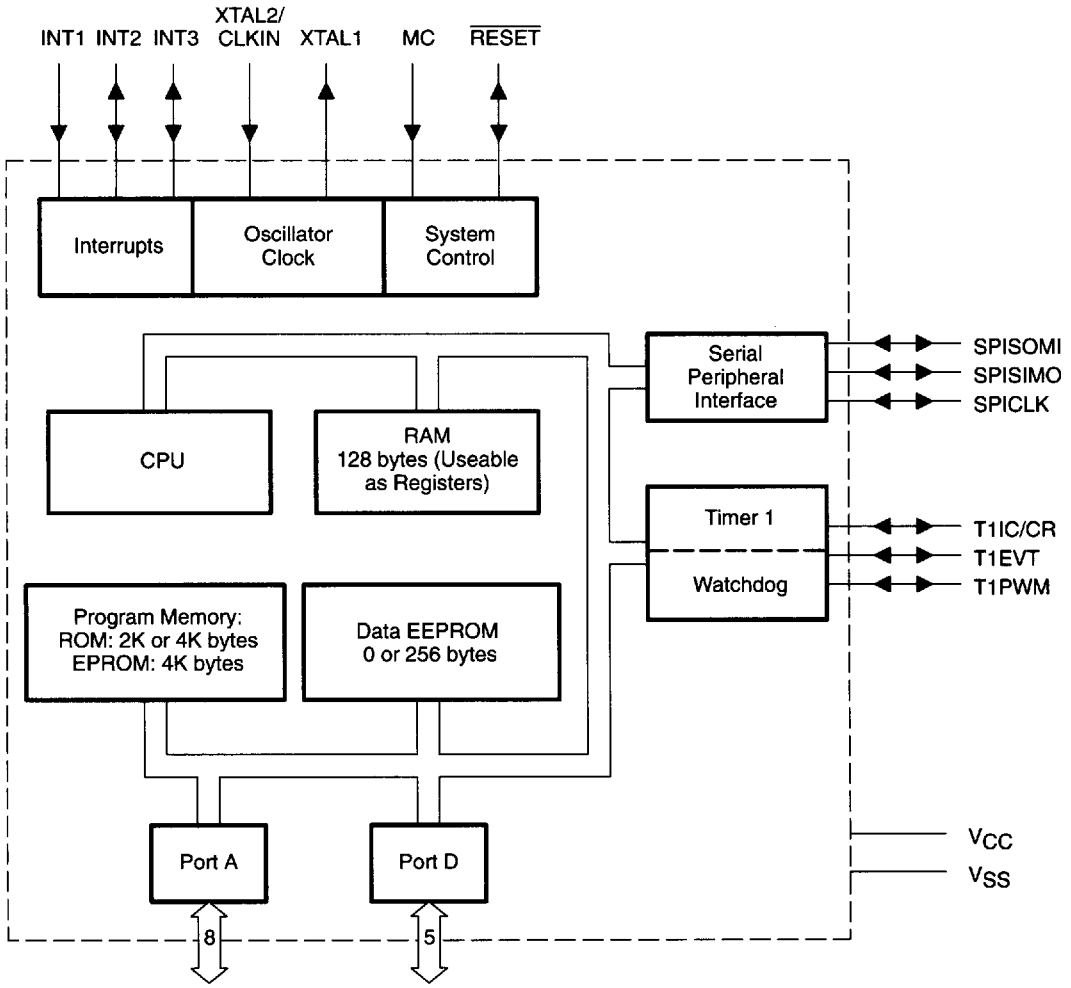


Figure 1–2 is a block diagram of the TMS370Cx2x devices, showing the major functional blocks.

Figure 1–2. TMS370Cx2x Block Diagram

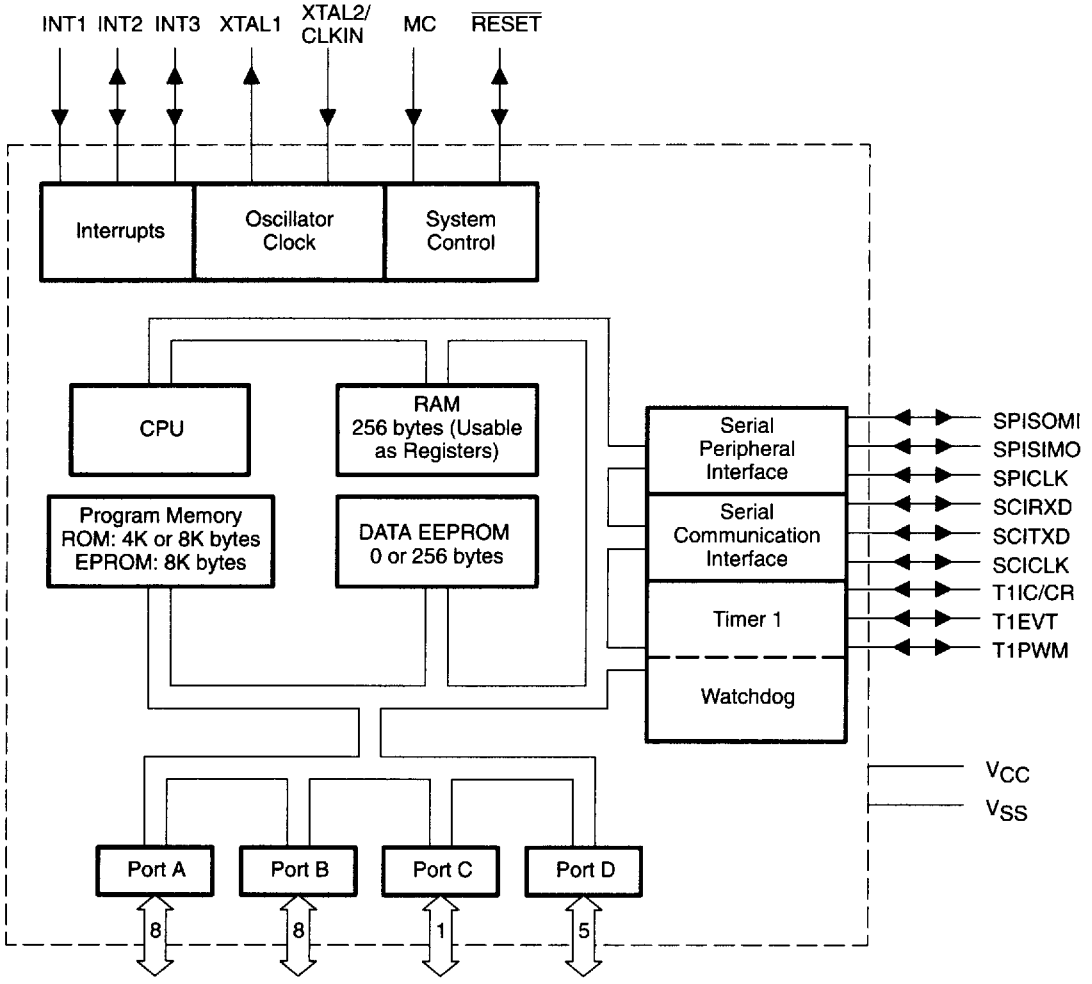
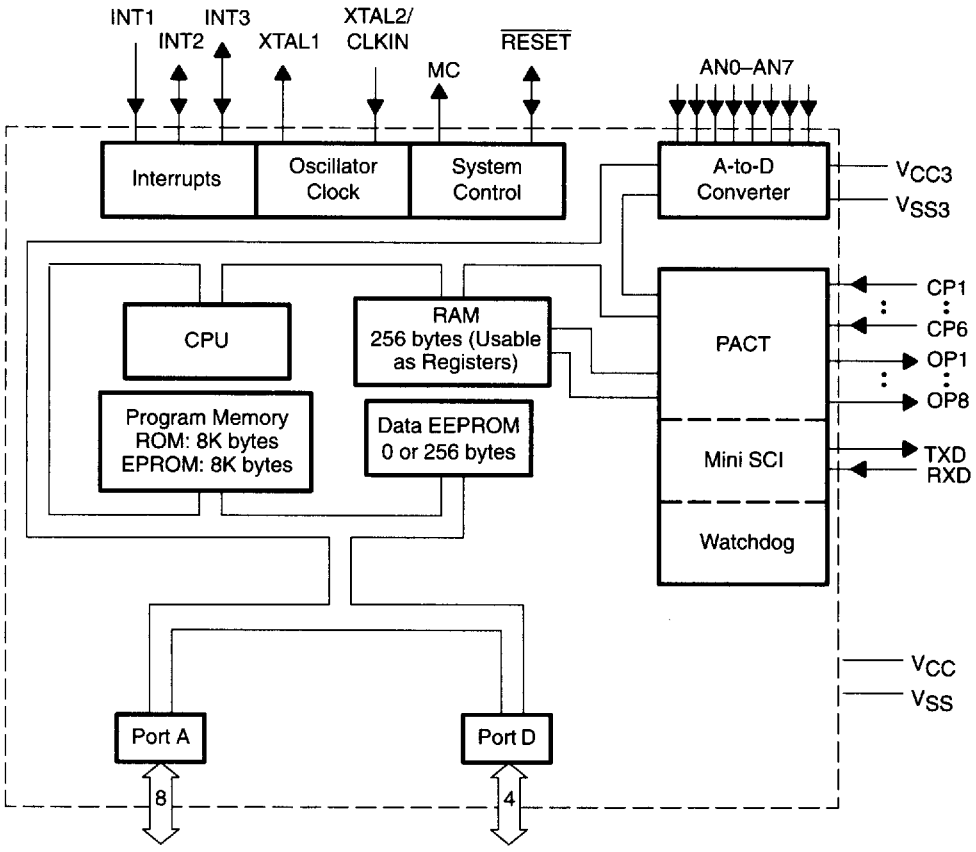


Figure 1–3 is a block diagram of the TMS370Cx3x devices, showing the major functional blocks.

Figure 1–3. TMS370Cx3x Block Diagram



Note: Three of port D's four I/O buffers (D4, D6, and D7) are internally connected to three of the PACT module's inputs (CP3, CP4, and CP5). This gives the actual pins of D4/CP3, D6/CP4, and D7/CP5.

Figure 1–4 is a block diagram of the TMS370Cx4x devices, showing the major functional blocks.

Figure 1–4. TMS370Cx4x Block Diagram

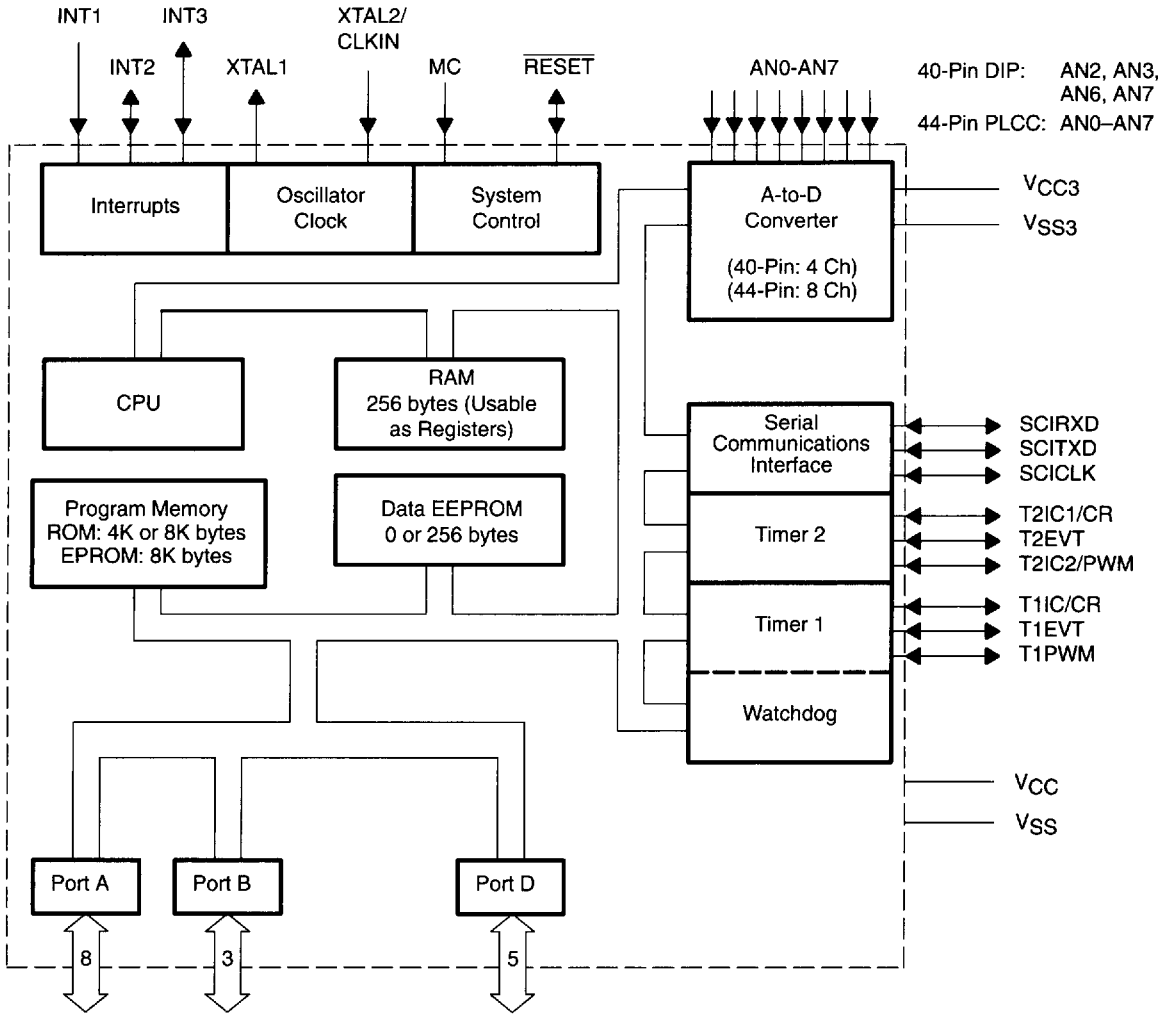
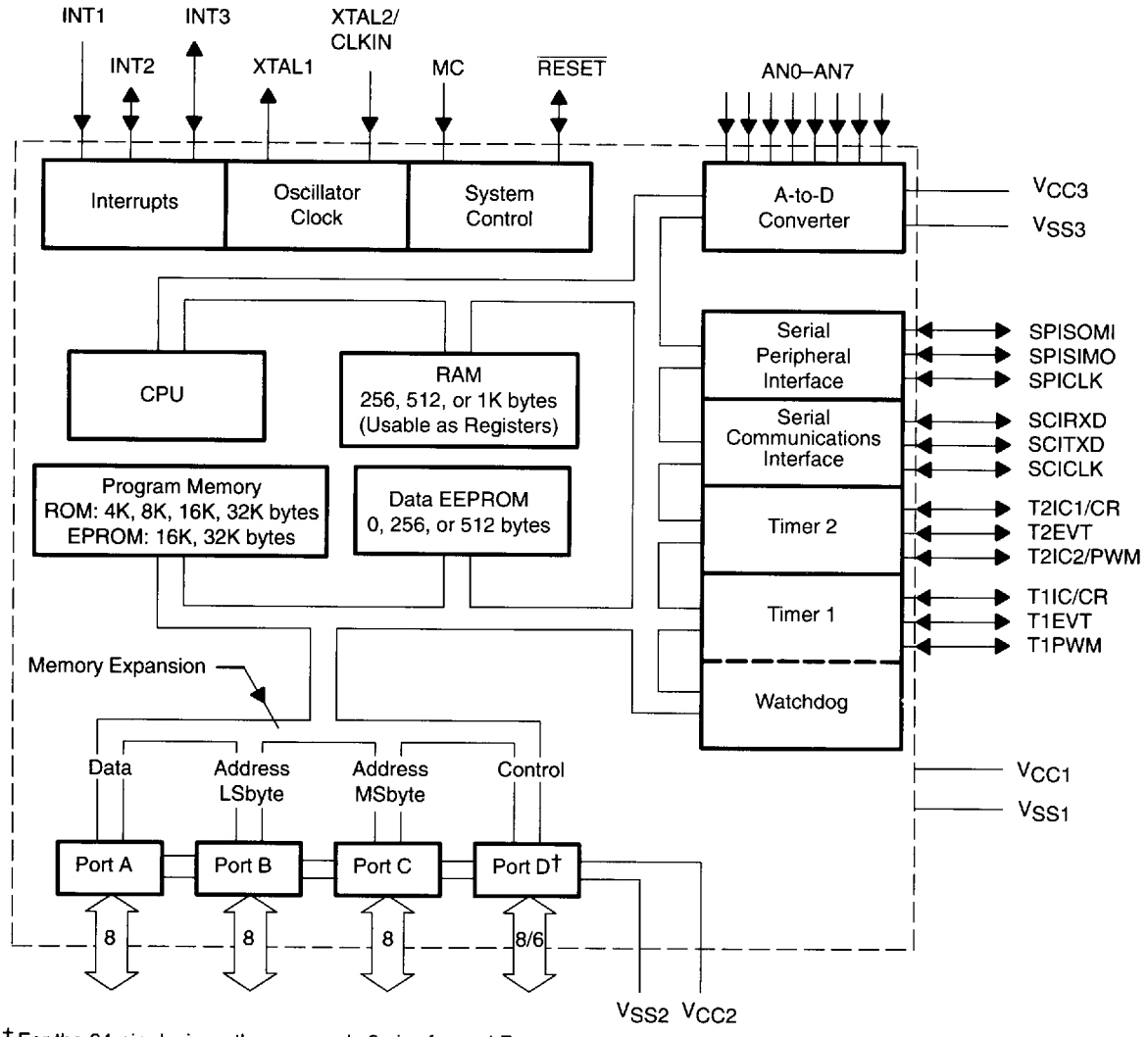


Figure 1–5 is a block diagram of the TMS370Cx5x devices, showing the major functional blocks.

Figure 1–5. TMS370Cx5x Block Diagram



† For the 64-pin devices, there are only 6 pins for port D.