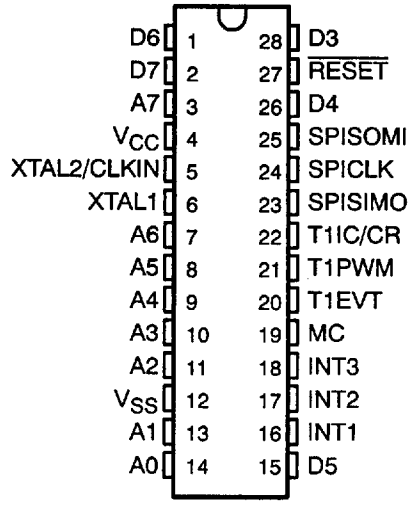
TMS370Cx10
8-BIT MICROCONTROLLERS

SPNS012B — MAY 1987 — REVISED DECEMBER 1990

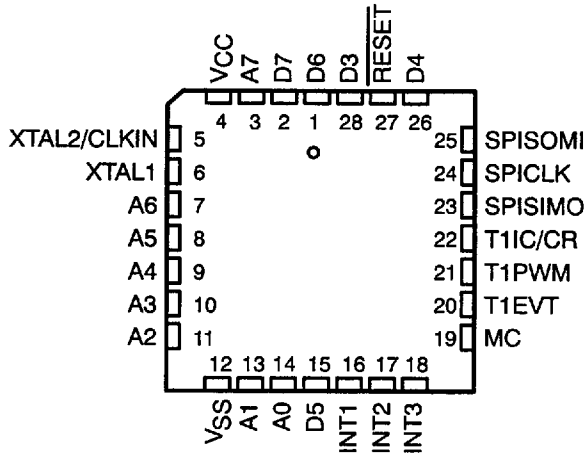
T-49-19-01

- CMOS/EEPROM/EPROM Technologies on a Single Device
  - — Form Factor Emulator (FFE) Devices for Prototyping Purposes
  - — One-Time Programmable (OTP) Devices for Low Volume Production
  - — Mask ROM Devices for High Volume Production
- Flexible Operating Features
  - — Power Reduction STANDBY and HALT Modes
  - — Commercial and Industrial Temperature Range
  - — Input Clock Frequency 2 MHz to 20 MHz
  - — Voltage (V_{CC}) 5 V ± 10%
- Internal System Memory Configurations
  - — 4K-Byte On-Chip Program Memory
  - — Mask ROM (TMS370C010 and TMS370C310) or
  - — EPROM (TMS370C710 and TMS370C610)
  - — Data EEPROM, 256 Bytes (TMS370C010 and TMS370C710)
  - — Static RAM, 128 Bytes Usable as Registers
- 16-Bit General Purpose Timer
  - — Software Configurable for a 16-Bit Event Counter, or a 16-Bit Pulse Accumulator, or a 16-Bit Input Capture Function, or Two Compare Registers, or a Self-Contained PWM Output Function
  - — Software Programmable Input Polarity
  - — 8-Bit Prescaler, Providing a 24-Bit Real-time Timer
- On-Chip 24-Bit Watchdog Timer
- Serial Peripheral Interface (SPI)
  - — Variable-Length High-Speed Shift Register
  - — Synchronous Master/Slave Operation
- Flexible Interrupt Handling
  - — Two S/W Programmable Interrupt Levels
  - — Global and Individual Interrupt Masking
  - — Programmable Rising or Falling Edge Detect
- 22 CMOS/TTL Compatible I/O Pins
  - — All Peripheral Function Pins Software Configurable for Digital I/O
  - — 21 Bidirectional Pins, 1 Input Pin

J and N Packages
(Top View)



FZ and FN Packages
(Top View)



- 28-Pin Packages
  - — Plastic DIP – ROM or OTP (N Suffix)
  - — Ceramic DIP – FFE (J Suffix)
  - — Plastic PLCC – ROM or OTP (FN Suffix)
  - — Ceramic CLCC – FFE (FZ Suffix)
- TMS370 Series Compatibility
  - — Register-to-Register Architecture
  - — 128 General-Purpose Registers
  - — 14 Powerful Addressing Modes
- PC-Based Workstation Development Support Emphasizes Productivity, Featuring:
  - — Realtime In-Circuit Emulation
  - — Symbolic Debug
  - — Extensive Breakpoint/Trace Capability
  - — C-Compiler Support
  - — Multi-Window User Interface
  - — EEPROM/EPROM Programming

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description

The TMS370C010, TMS370C310, TMS370C610, and TMS370C710 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. The TMS370 family provides cost-effective realtime system control through VLSI integration of advanced on-chip memory and peripheral function modules.

The TMS370 family is implemented using high-performance silicon-gate CMOS technology. The low operating power, wide operating temperature range, and high noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx10 devices attractive in system designs for automotive electronics, industrial control, computer peripheral control, and telecommunications.

Unless otherwise noted, the term TMS370Cx10 refers to the TMS370C010, TMS370C310, TMS370610, and the TMS370C710 for all peripheral function modules available on those devices. All TMS370Cx10 devices contain the following modules:

- 4 K bytes Program memory.
- 128 bytes Ram (usable as registers).
- Serial Peripheral Interface (SPI).
- Timer1-16-bit general-purpose timer with Watchdog

The following table provides a memory configuration overview of the TMS370Cx10 devices.

DEVICE	PROGRAM MEMORY	DATA EEPROM	PACKAGE
TMS370C010	4K Bytes ROM	256 Bytes	N – DIP FN – PLCC
TMS370C310	4K Bytes ROM	None	N – DIP FN – PLCC
TMS370C610	4K Bytes EPROM	None	N – DIP FN – PLCC
TMS370C710	4K Bytes EPROM	256 Bytes	N – DIP FN – PLCC
SE370C710†	4K Bytes EPROM	256 Bytes	J – CDIP FZ – CLCC

† System evaluators and development tools are for use only in a prototype environment and their reliability has not been characterized.

The 4K bytes of mask-programmable ROM in the TMS370C010 and TMS370C310 are replaced in the TMS370C710 and TMS370C610 with 4K bytes of EPROM while all other available memory and on-chip peripherals are identical, with the exception of no Data EEPROM on the TMS370C310 and TMS370C610 devices. The TMS370C610 and TMS370C710 OTP devices allow customers to change code without reordering a MASK ROM device. The OTP devices reduce manufacturing design times for new code and are excellent low volume production alternatives.

The windowed ceramic FFE devices, SE370C710 FZ, J, offer reprogramming capabilities for prototyping requirements.

The TMS370Cx10 provides two power reduction modes (STANDBY and HALT) for applications where low power consumption is critical. Both modes stop all CPU activity (i.e., no instructions are executed). In the STANDBY mode the internal oscillator and the general purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both powerdown modes.

The TMS370Cx10 features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (e.g., ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx10 instruction set is fully compatible with other TMS370 family members, allowing easy transition between members.

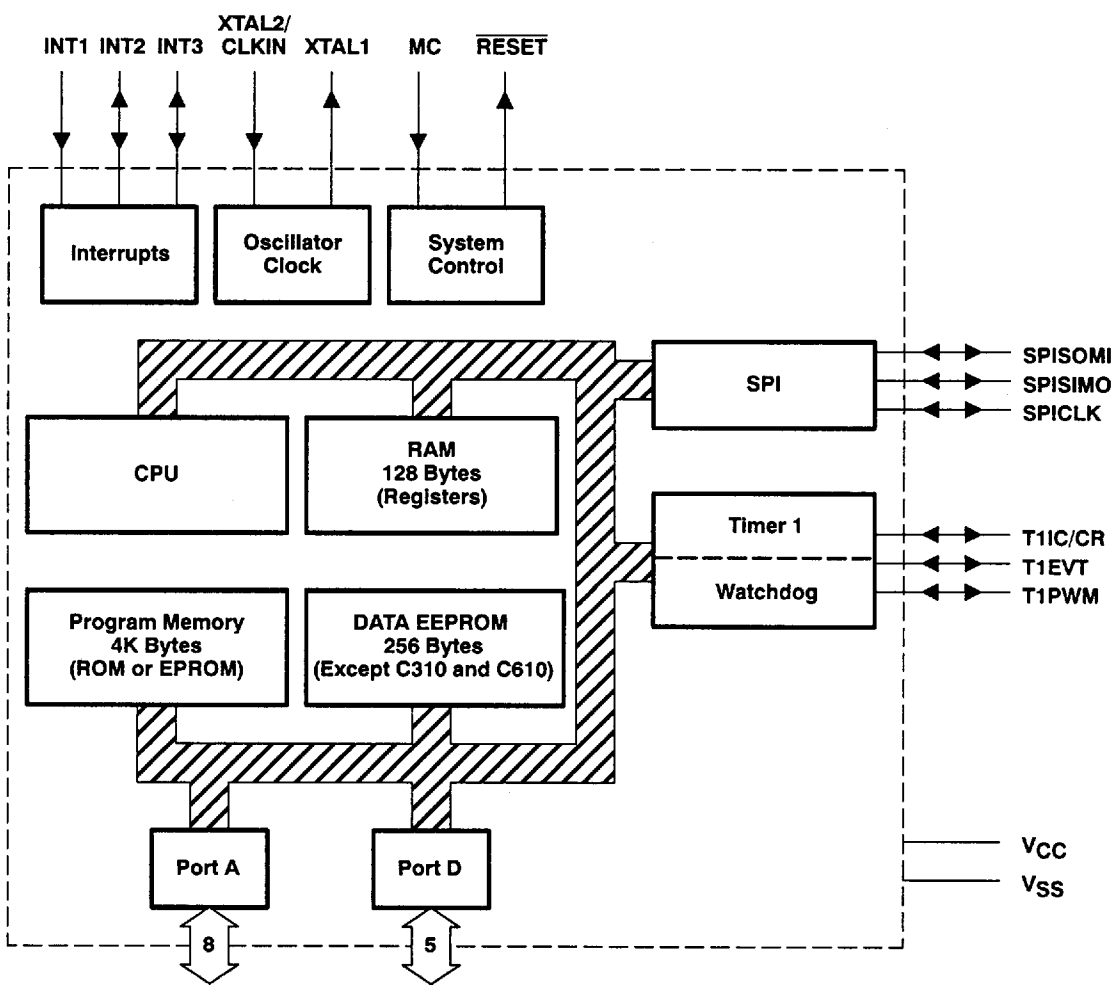
The SPI gives a convenient method of serial interaction for high speed communications between simpler shift register type devices, such as display drivers, A/D converters, PLL, I/O expansion, or other microcontrollers in the system.

T-49-19-01

The TMS370 family provides the system designer with an economical, efficient solution to realtime control applications. The TMS370 family eXtended Development System (XDS) solves the challenge of efficiently developing the software and hardware required to design the TMS370 into an ever-increasing number of complex applications. The application source code modules can be written in Assembly and/or C language and the output code can be generated by the linker. The TMS370 family XDS communicates via a standard RS-232-C interface with an existing personal computer to form a PC-DOS hosted workstation, using the PC's editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer can begin developing software with minimum training. Precise realtime in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market.

The TMS370Cx10 mask ROM devices, the TMS370x10 OTP devices, together with the TMS370 family XDS for applications development, the SE370C710 EPROM devices, and comprehensive product documentation and customer support provide a complete solution to the low end needs of the systems designer. Other TMS370 family members are available with additional memory, I/O and peripheral functions such as SCI and A/D to meet more complex system requirements.

functional block diagram



pin descriptions

PIN NAME	PIN NO.	I/O	DESCRIPTION
A0	14	I/O	Port A is a general purpose bidirectional port.
A1	13	I/O	
A2	11	I/O	
A3	10	I/O	
A4	9	I/O	
A5	8	I/O	
A6	7	I/O	
A7	3	I/O	
D3	28	I/O	General purpose bidirectional pin. Also configurable as CLKOUT.
D4	26	I/O	General purpose bidirectional pin.
D5	15	I/O	General purpose bidirectional pin.
D6	1	I/O	General purpose bidirectional pin.
D7	2	I/O	General purpose bidirectional pin.
INT1	16	I	External interrupt non-maskable or maskable interrupt / general purpose input pin.
INT2	17	I/O	External maskable interrupt input/general purpose bidirectional pin.
INT3	18	I/O	External maskable interrupt input/general purpose bidirectional pin.
T1IC/CR	22	I/O	Timer 1 Input Capture/Counter Reset input pin/general purpose bidirectional pin.
T1PWM	21	I/O	Timer 1 PWM output pin/general purpose bidirectional pin.
T1EVT	20	I/O	Timer 1 External Event input pin/general purpose bidirectional pin.
SPISOMI	25	I/O	SPI Slave Output pin, Master Input pin/general purpose bidirectional pin.
SPISIMO	23	I/O	SPI Slave Input pin, Master Output pin/general purpose bidirectional pin.
SPICLK	24	I/O	SPI bidirectional Serial Clock pin/general purpose bidirectional pin.
$\overline{\text{RESET}}$	27	I/O	System reset bidirectional pin. As an input, it initializes microcontroller. As open-drain output it indicates an internal failure was detected by the Watchdog or Oscillator Fault circuit.
MC	19	I	Mode control input pin; enables EEPROM Write Protection Override (WPO) mode. Normal operation = 0 V, WPO = 12 V. V_{PP} supply for EPROM programming.
XTAL2/ CLKIN	5	I	Internal oscillator crystal input/external clock source input.
XTAL1	6	O	Internal oscillator output for crystal.
V_{CC}	4		Positive supply voltage.
V_{SS}	12		Ground reference.

NOTE 1: Each pin associated with Interrupt 2, Interrupt 3, Timer 1, and SPI functional blocks may be individually programmed as a general purpose bidirectional pin if it is not used for its primary block function.

T-49-19-01

memory map

The TMS370 family architecture is based on the Von Neumann architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 1, the TMS370 provides memory-mapped RAM, ROM, EEPROM, EPROM, input/output pins, and peripheral functions.

The peripheral file contains all input/output port control, peripheral status and control, EEPROM memory programming, and system-wide control functions. The peripheral file is located from 1010h to 104Fh and is logically divided into 5 Peripheral File Frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx10 has its peripherals and system control assigned to Peripheral File Frames 1 through 4, addresses 1010h through 104Fh.

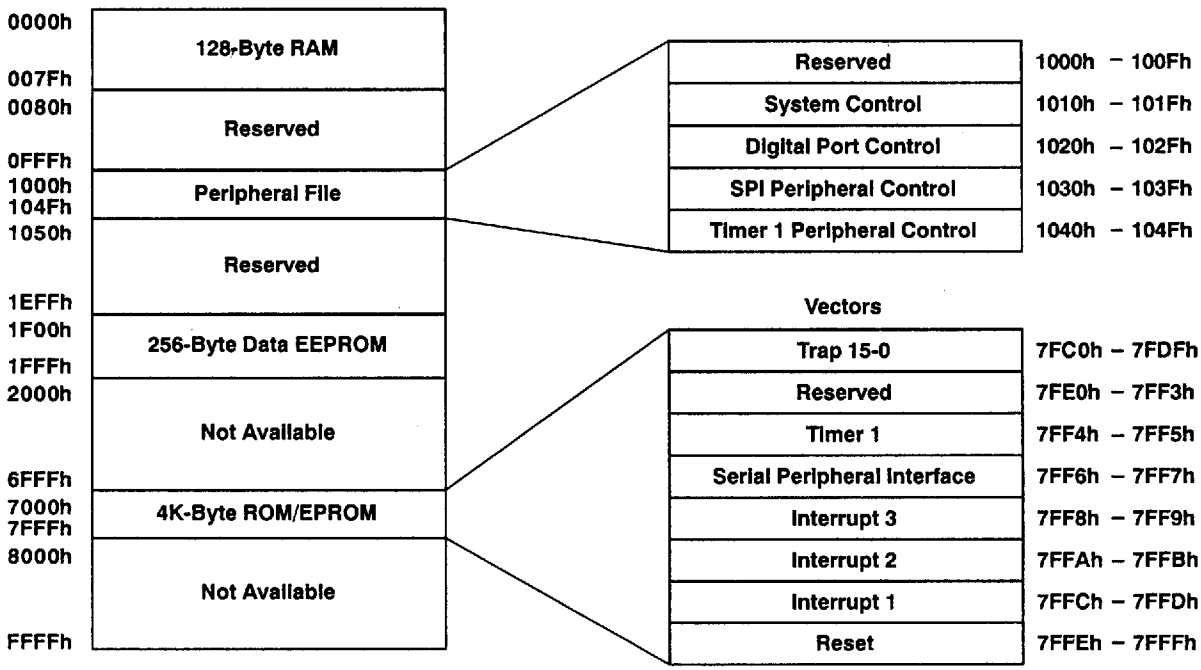


Figure 1. TMS370Cx10 Memory Map

memories

RAM/register file

The TMS370Cx10 has 128 bytes of static RAM, which serve as both the CPU register file and general-purpose memory. The RAM is treated as registers by the instruction set and is referenced as R0 through R127. The first two registers, R0 and R1, are also called the A and B registers, respectively. The stack is located in the RAM, and operates as a last-in first-out read/write memory. It is used to store the return address on subroutine calls and the status register during interrupts. Accessing this memory as registers is performed in one system clock cycle (t_c), while general-purpose memory access is performed in two system clock cycles.

data EEPROM

The TMS370C010 and TMS370C710 have 256 bytes of on-chip Electrically Erasable Programmable ROM (EEPROM), addressed as 256 consecutive bytes mapped from locations 1F00h to 1FFFh. The Data EEPROM provides nonvolatile programmable storage for items such as calibration constants and configuration information for personalization of a generic algorithm for use in specific end applications. The Data EEPROM supports bit, byte, and block write/erase modes. Instructions may be executed from Data EEPROM, providing additional program space and the ability to patch algorithms by placing a branch table for volatile routines in Data EEPROM.

The Data EEPROM uses the 5-V V_{CC} supply voltage and provides the programming voltage via an internal dedicated generator, eliminating the need for an external high-voltage programming source. The dedicated voltage generator optimizes the programming voltage characteristics, increasing the reliability as well as extending the write/erase endurance of the array.

Programming control and status monitoring are performed through the Data EEPROM control register (DEECTL) in the peripheral file. An EEPROM write/erase operation is performed in the following sequence:

1. Perform normal memory write to the target EEPROM location.
2. Write to DEECTL control register to select WRITE1/WRITE0 and set the EXECUTE (EXE) bit to 1.
3. Wait for program time to elapse [$t_{w(PGM)B}$ or $t_{w(PGM)AR}$].
4. Write to DEECTL control register to set the EXECUTE (EXE) bit to 0.

The WRITE1/WRITE0 control bit selects whether the zeros or the ones in the data byte are to be programmed into the selected EEPROM location. For example, a WRITE1 operation will program ones into all bit positions within the EEPROM byte that have ones in the data byte, while bits that are zero in the data byte will not affect the EEPROM contents. The WRITE1 operation effectively performs a logical OR of the information previously stored on the EEPROM byte with the data byte. The WRITE0 operation effectively performs a logical AND between these two bytes. Single bit programming within an EEPROM byte is performed by writing only the zeros or ones of the data byte. The EEPROM programming algorithm may use this bit-programming capability to optimize the life of the EEPROM.

When a data value cannot be achieved by writing only zeros or only ones into the EEPROM byte, a WRITE1 followed by a WRITE0 will program any data value into the EEPROM byte, regardless of the previous data stored at that location.

All unprotected bytes within the Data EEPROM array may be programmed during a single EEPROM programming cycle by setting the ARRAY PROG bit of DEECTL to 1 at the start of the programming cycle.

Data EEPROM read accesses are performed as normal memory read operations in two system clock cycles. A memory read cycle to any EEPROM location while EXE = 1 returns the value currently being written to the EEPROM. Following an EEPROM write operation, the EEPROM voltages must stabilize prior to performing an EEPROM read operation. The BUSY FLAG indicates the status of the EEPROM voltage. When set, the EEPROM is not ready for a read operation. The BUSY flag is reset to 0 by the EEPROM control logic when 128

system clock cycles have elapsed following the EXE bit being set to 0. If an EEPROM read operation is performed while BUSY = 1, automatic WAIT states will be generated until BUSY = 0, and then the read operation will be performed.

Bytes within the Data EEPROM may be protected from inadvertent overwriting of critical information. As shown in Figure 2, the 8-bit Write Protect Register (WPR), located at 1F00h within the data EEPROM, provides write protection for the 256-byte Data EEPROM, segmenting the array into eight blocks of 32 bytes each. Each of these 32-byte blocks may be individually write- and erase-protected by setting the corresponding bit to 1 in the WPR. Since the WPR resides in the array in BLK0, the WPR may also be write-protected, thereby increasing the system reliability by preventing bytes from being reprogrammed. Bytes left unprotected may be written to by the normal EEPROM programming sequence. The Write Protection Override (WPO) mode overrides the write protection of all blocks in the Data EEPROM, and enables data to be written to any location in the Data EEPROM, regardless of the WPR contents. Enter the WPO mode by placing 12-V on the MC pin. The WPO mode is typically used in a service environment to update the protected EEPROM contents. The 12-V input level on the MC pin to enter the WPO mode is not normally present in an application except in a service environment; therefore, the data integrity of the program is ensured during normal operation.

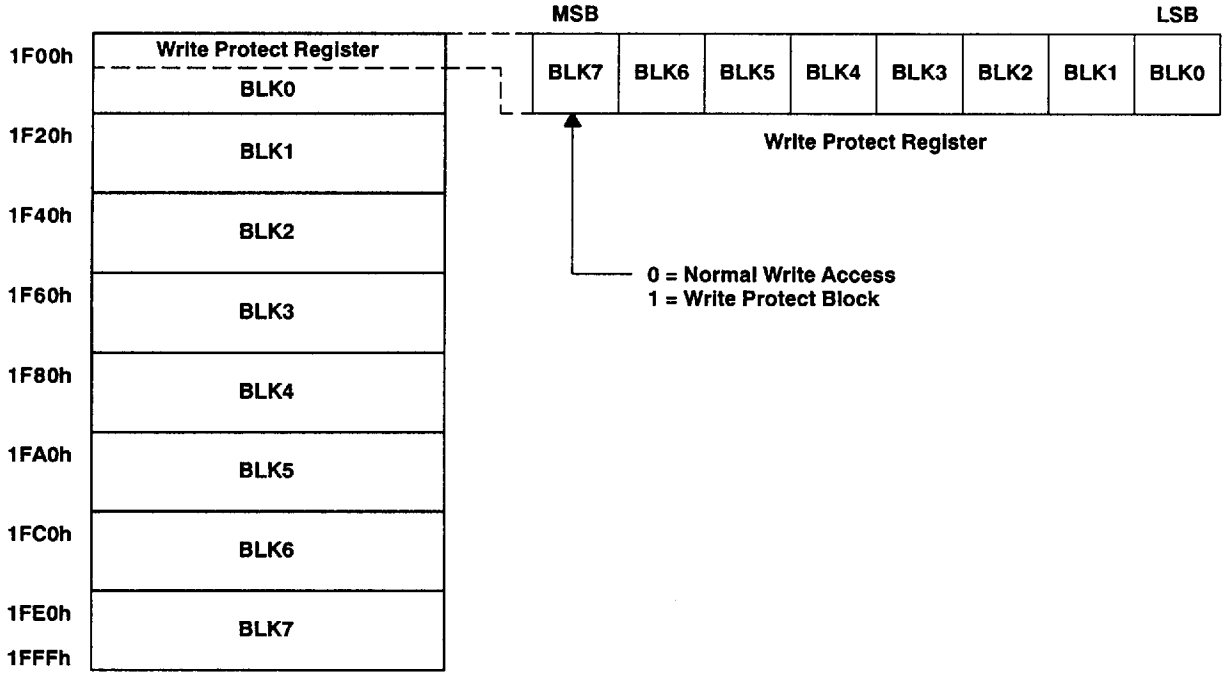


Figure 2. Write Protect Register

program ROM

The Program ROM consists of 4K bytes of mask programmable read-only memory. The Program ROM is used for permanent storage of data and instructions, with read operations performed in two system clock cycles. Memory addresses 7FF4h through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Programming of the mask ROM is performed at the time of device fabrication.

program EPROM

The Program EPROM of the TMS370C610 and TMS370C710 is a 4K ultraviolet-light-erasable, electrically programmable read-only memory, addressed as 4K consecutive bytes mapped form location 7000h to 7FFFh. It provides application performance identical to the TMS370Cx10 mask ROM devices with up to 4K bytes. Program instructions are read from the Program EPROM in two system clock cycles, providing the prototyping capability of the Mask Program ROM.

An external supply (V_{PP}) is needed at the MC pin to provide the necessary voltage (V_{PP}) for programming. Programming is controlled through the EPCTL register (P01C) in the peripheral file.

Before programming, the SE370C710's EPROM must be erased by exposing the device through the transparent window to high-intensity ultraviolet light (wavelength 2537Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15- W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, the entire array is in a logic high state. A programmed low can be erased only by exposure to ultraviolet light. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SE370C710, the window should be covered with an opaque label. All devices are erased to logical high when delivered from the factory.

CAUTION

Exposing the EPROM module to ultraviolet light may also cause erasure in any EEPROM module. Any useful data stored in the EEPROM must be reprogrammed after exposure to UV light.

Programming lows into the EPROM is controlled by the EPCTL register via the EXE bit and the VPPS bit. The EXE bit initiates EPROM programming when set and disables programming when cleared. The VPPS bit connects the programming voltage V_{PP} at the MC pin to the EPROM module. VPPS (EPCTL.6) and EXE (EPCTL.0) should be set separately, and the VPPS bit should be set at least two microseconds before the EXE bit is set. After programming, the application programming should wait for four microseconds before any read attempt is made. The programming operation (see Figure 3) is performed in the following recommended sequence:

1. Supply the programming voltage to the MC pin.
2. Write to EPCTL register to set the VPPS bit to 1 (high).
3. Perform normal memory write register to the target EPROM location.
4. Write to EPCTL register to set the EXE bit register to 1 (high). (Wait at least two microseconds after step 2.
5. Wait for program time to elapse (one millisecond).
6. Write to EPCTL register to clear the EXE bit (leave VPPS bit set to 1 (high)).
7. Read the byte being programmed; if correct data is not read, repeat steps 4 through 6 up to a maximum X of 25.
8. Write to EPCTL register to set the EXE bit to 1 (high) for Final programming.
9. Wait for program time to elapse (3X milliseconds duration).
10. Write to EPCTL register to clear the EXE and VPPS bits.

T-49-19-01

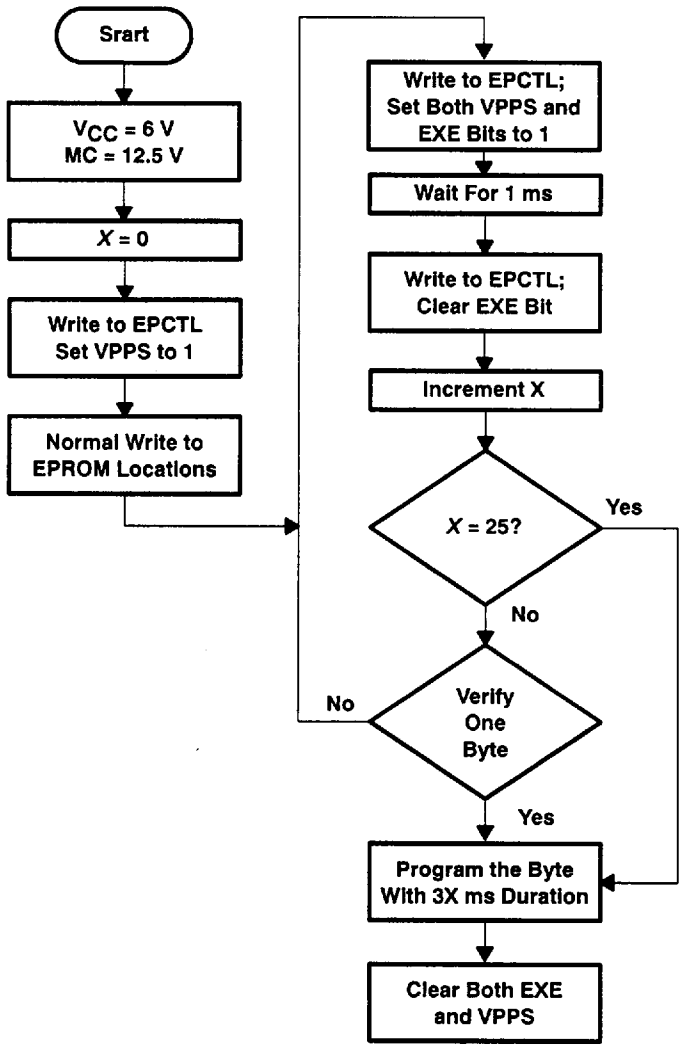


Figure 3. EPROM Programming Operation

An external power supply at V_{PP}, I_{PP} (30 mA), is required for programming operation. Programming voltage V_{PP} is supplied via the MC pin. This also automatically puts the microcontroller in the Write Protection Override (WPO) mode. Programming voltage may be applied via the MC pin anytime after reset and remain at V_{PP} after programming (after the EXE bit is cleared). Applying programming voltage while $\overline{\text{RESET}}$ is active will put the microcontroller in a reserved mode, where programming operation is inhibited.

write protect of program EPROM

To override the EPROM write protection, the V_{PP} voltage must be applied to the MC pin and the VPPS bit (EPCTL.6) must be set. This dual requirement ensures that the program EPROM will not accidentally be overwritten during the Data EEPROM operations when V_{PP} is applied to the MC pin. The Data EEPROM may be programmed when the VPPS bit is set.

central processing unit

The central processing unit (CPU) of the TMS370 series is an enhanced version of the TMS7000 Family CPU. The enhancements include additional user instructions such as integer divide, conditional jump instructions based on the overflow status bit, and addressing modes such as stack-pointer-relative addressing for subroutine parameter passing. The efficient register-to-register architecture of the TMS7000 family has been carried over to the TMS370 family, which avoids the conventional accumulator bottleneck. The complete TMS370 family instruction set is summarized in the TI *TMS370 INSTRUCTION SET SUMMARY* beginning on page 28.

In addition to the interpretation and execution of the user program, the CPU performs the functions of bus protocol generation and interrupt priority arbitration. While the CPU is implemented independent of the memory, input/output, and peripheral modules, it performs the central system control function through communications with these on-chip modules.

The TMS370 family CPU registers accessible to the programmer are shown in Figure 4. The register file consists of 128 general purpose registers, R0 through R127 implemented in on-chip RAM, and is used by the CPU for general purpose 8- and 16-bit source and destination operands, index registers, and indirect addressing. The first two registers, R0 and R1, are also called registers A and B and are used by the CPU as general purpose registers or for implied operands. The program counter (PC) contains the address of the next instruction to be executed. The stack pointer (SP) contains the address of the last or top entry on the stack, which is located in the on-chip RAM. The status register (ST) contains four bits that reflect the outcome of the instruction just executed, and two bits that control the masking of the interrupt priority chains.

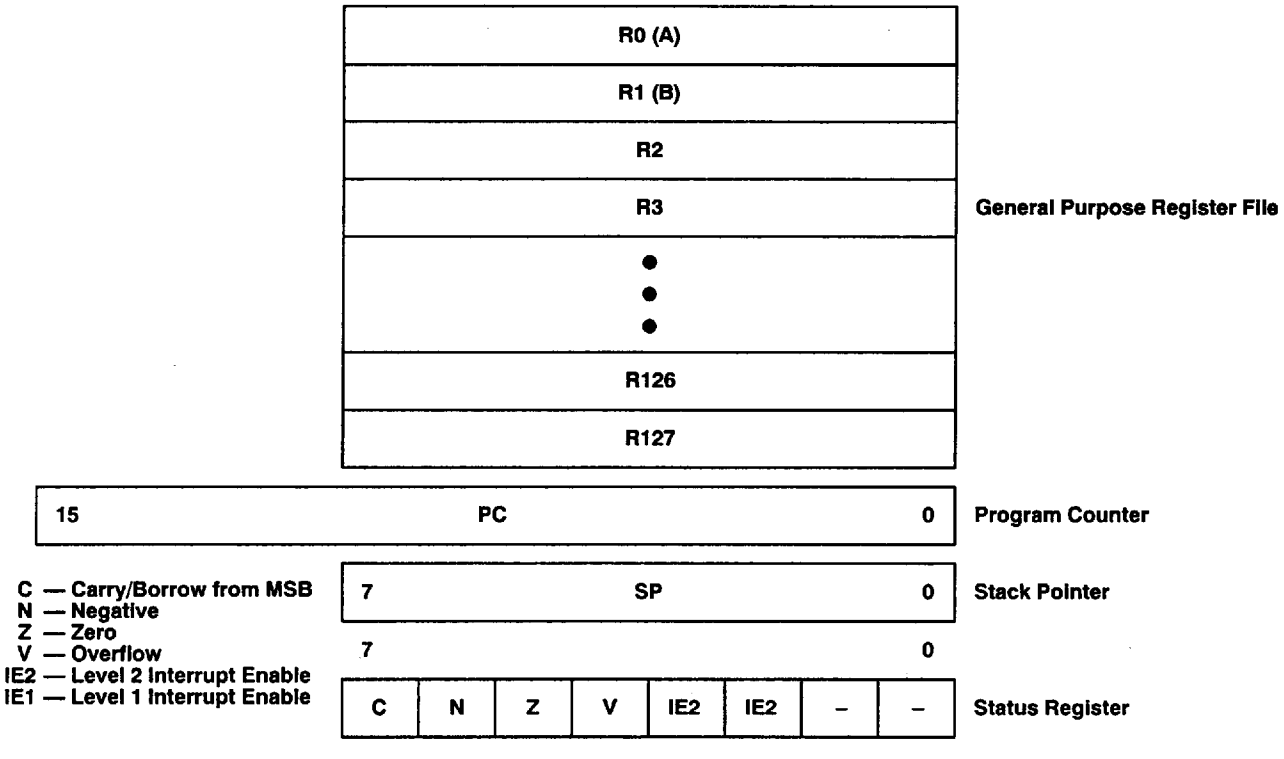


Figure 4. CPU Registers

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system resets

The TMS370Cx10 has three possible reset sources: a low input to the $\overline{\text{RESET}}$ pin, a programmable watchdog timer timeout, or a programmable oscillator fault failure. The $\overline{\text{RESET}}$ pin, an input/output pin, initiates TMS370Cx10 hardware initialization and ensures an orderly software startup. A minimum 50-ns low level input initiates the reset sequence. The microcontroller is held in reset until the $\overline{\text{RESET}}$ pin goes inactive (high). If the $\overline{\text{RESET}}$ input signal is low for less than eight system clock cycles, the TMS370Cx10 will hold the external $\overline{\text{RESET}}$ pin low for eight system clock cycles to reset external system components. The $\overline{\text{RESET}}$ should be released only after stable oscillation and valid V_{CC}. The $\overline{\text{RESET}}$ pin must be activated by the application at power-up, which can be accomplished by an external input or an RC power-up reset circuit. In addition, the application must activate $\overline{\text{RESET}}$ when V_{CC} goes out of spec to prevent corruption of data and erroneous operation. The $\overline{\text{RESET}}$ pin can be asserted at any time during operation, resulting in an immediate initiation of the reset sequence.

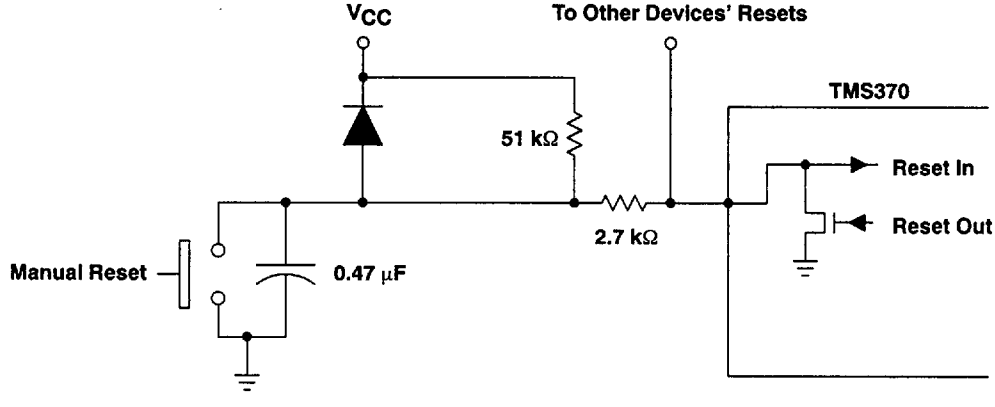


Figure 5. Typical Reset Circuit

The watchdog timer provides system integrity by detecting a program that has become lost or is not executing as expected. A system reset is generated if the watchdog timer is not properly re-initialized by a specific software sequence, or if the re-initialization does not occur before the watchdog timer times out. The watchdog timer timeout initiates the TMS370Cx10 reset sequence and drives the external $\overline{\text{RESET}}$ pin low for eight system clock cycles to reset external system components. The Watchdog reset function is enabled by setting WD OVRFL RST ENA bit of T1CTL2 to 1. Once the software enables the watchdog reset function, subsequent writes to the WD OVRFL RST ENA bit are ignored. Watchdog control bits can be initialized only following a power-up reset. The timer section discusses additional information on the watchdog timer and its configurations.

The oscillator fault circuit provides the means to monitor failures of the oscillator input signal (XTAL2/CLKIN). If the oscillator input signal frequency remains above the 90% point of the minimum operating frequency (CLKIN), the oscillator input will not to be activated. However, if the oscillator input is lost or its frequency falls below 20 kHz and the oscillator fault reset has not been disabled, the TMS370Cx10 is reset and the external $\overline{\text{RESET}}$ pin is driven low.

When an oscillator input failure occurs, the internal clocks are stopped and $\overline{\text{RESET}}$ is held active until the oscillator input frequency is greater than 100 kHz typical. The reset action can be disabled by clearing the OSC FLT RST ENA bit (P012.5). Oscillator fault detection can be disabled by setting the OSC FLT DISABLE bit (P012.2). Since operation is unpredictable with slow or intermittent clocks, neither of these actions is recommended. During the HALT mode the oscillator fault circuitry is disabled.

Reset puts the address at 7FFEh and 7FFFh (lsb) into the PC and then clears Registers A and B and the status register. The Stack Pointer is set to 01h during reset. A reset when the device is already running will not affect the other RAM registers.

Control Bit States Following Reset

REGISTER	CONTROL BIT	POWER-UP	WARM RESET
SCCR0	µP/µC MODE	0	0
SCCR0	MC PIN DATA	0	0
SCCR0	COLD START	1	†
SCCR0	OSC FLT FLAG	0	†
T1CTL2	WD OVRFL FLAG	0	†

† Status bit corresponding to active reset source is set to 1.

interrupts

The TMS370 family software-programmable interrupt structure supports flexible on-chip and external interrupt configurations to meet realtime interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be independently enabled by the global interrupt enable bits (IE1 and IE2) of the Status Register.

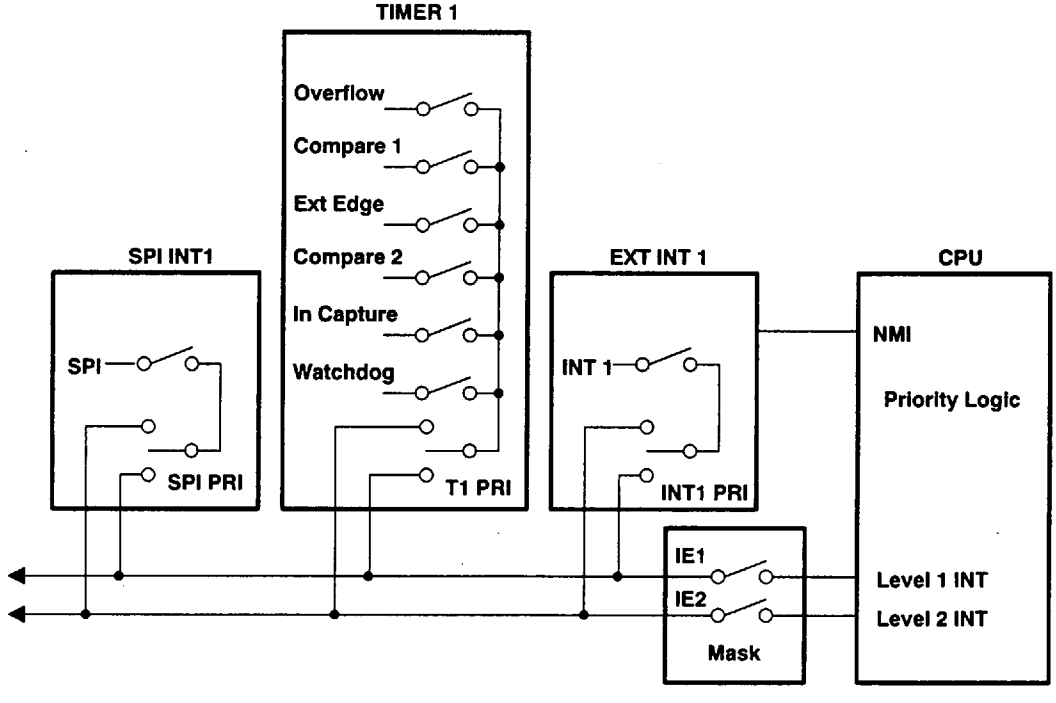


Figure 6. Interrupt Control

Each system interrupt is independently configured on either the high or low priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high or low priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx10 has six hardware system interrupts as shown in the following table. Each system interrupt has a dedicated interrupt vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All of the interrupt sources are

individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or to determine which interrupt source generated the associated system interrupt.

Two of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual or global mask bits. Recall that the INT1 NMI bit is protected during nonprivileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR INTERRUPT	PRIORITY§
External Reset Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}$†	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1†	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2†	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3†	7FF8h, 7FF9h	4
SPI RX/TX Complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 Overlfow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC INT FLAG WD OVRFL INT FLAG	T1INT‡	7FF4h, 7FF5h	6

† Releases microcontroller from STANDBY and HALT low power modes.
‡ Releases microcontroller from STANDBY low power mode.
§ Relative priority within an interrupt level.

privileged operation and EEPROM write protection override

The TMS370Cx10 family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The non-privileged mode of operation ensures the integrity of the system configuration once defined for an end application. Following a hardware reset, the TMS370Cx10 operates in the privileged mode, where all peripheral file registers have unrestricted read/write access and the application program will configure the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGED MODE bit of SCCR3 will be set to 1, entering the non-privileged mode and disabling write operations to specific configuration control bits within the peripheral file. The following system configuration bits are write-protected during the non-privileged mode and must be configured by software prior to exiting the privileged mode:

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.6	OSC POWER
SCCR2	P012.0	PRIVILEGED MODE
SCCR2	P012.6	PWRDWN/IDLE
SCCR2	P012.7	HALT/STANDBY
SCCR2	P012.1	INT1 NMI
SCCR2	P012.2	OSC FLT DISABLE
SCCR2	P012.5	OSC FLT RST ENA
SPIPRI	P03F.6	SPI PRIORITY
T1PRI	P04F.6	T1 PRIORITY

† Identified by name and bit location within the register

The privileged bits are shown in a **bold typeface** in the following Peripheral File Frame sections.

The EPROM can only be written to when V_{PP} is applied to the MC pin and the VPPS (EPCTL.6) bit is set. When V_{PP} is applied to the MC pin all on-chip EEPROM is in the Write Protect Override (WPO) mode regardless of the state of the VPPS bit. This allows the EPROM to be protected while the EEPROM is in WPO.

low-power operating modes

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the POWERDOWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY=0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and Timer 1 remain active. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on INT1, INT2, or INT3, or a Timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY=1), the TMS370x10 is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$ or external interrupt on INT1, INT2, or INT3) is detected. The powerdown mode selection bits are summarized in the following table:

POWERDOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	Standby
1	1	Halt

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. All CPU instruction processing is stopped during the STANDBY and HALT modes, and clocking of the watchdog timer is inhibited.

T-49-19-01

peripheral file frame 1

Peripheral File Frame 1 contains system configuration and control functions and registers for controlling EPROM and EEPROM programming. The privileged bits are shown in a **bold typeface** in the Peripheral File Frames.

Peripheral File Frame 1: System Configuration and Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
1010h	P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	µP/µC MODE	SCCR0
1011h	P011	—	—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
1012h	P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	**OSC FLT RST ENA**	**BUS STEST**	**CPU STEST**	**OSC FLT DISABLE**	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
1013h to 1016h	P013 to P016	RESERVED								
1017h	P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
1018h	P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
1019h	P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
101Ah	P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
101Bh	P01B	RESERVED								
101Ch	P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL

peripheral file frame 2

Peripheral File Frame 2 contains the digital I/O pin configuration and control registers. The following figure details the specific addresses, registers, and control bits within this Peripheral File Frame.

Peripheral File Frame 2: Digital Port Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
1020h	P020	RESERVED								APORT1
1021h	P021	Port A Control Register 2 (must be 0)								APORT2
1022h	P022	Port A Data								ADATA
1023h	P023	Port A Direction								ADIR
1024h to 102Bh	P024 to P02B	RESERVED								
102Ch	P02C	Port D Control Register 1 (must be 0)					X	X	X	DPORT1
102Dh	P02D	Port D Control Register 2 (must be 0)†					X	X	X	DPORT2
102Eh	P02E	Port D Data					X	X	X	DDATA
102Fh	P02F	Port D Direction					X	X	X	DDIR

† To configure pin D3 as CLKOUT, set Port D Control Register 2 equal to 08h.

Port Configuration Registers Set-up

PORT	PIN	abcd 00x0	abcd 00q1
A	0 — 7	Data In	Out q
D	3 — 7	Data In	Out q
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

NOTES: 2. Each bit controls the corresponding pin; for example, bit 6 controls Port pin 6. Each pin is individually configurable.
3. Only register combination 00xx is defined for TMS370Cx10.

T-49-19-01

programmable timers

The programmable timer module of the TMS370Cx10 provides the designer with the enhanced timer resources required to perform realtime system control. The Timer 1 module contains the general-purpose T1 and the watchdog timer WD. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (realtime, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. These timers provide the capabilities for:

System Requirements	Timer Resource
Realtime System Control	Interval Timers with Interrupts
Input Pulse Width Measurement	Pulse Accumulate or Input Capture Functions
External Event Synchronization	Event Counter Function
Timer Output Control	Compare Function
Pulse-Width Modulated Output Control	PWM Output Function
System Integrity	Watchdog Function

timer 1 module

The timer 1 module consists of three major blocks:

1. Prescaler/Clock Source, which determines the independent clock sources for the general purpose timer and the watchdog timer.
2. 16-bit General Purpose Timer, T1, which provides the event count, input capture, and compare functions.
3. 16-bit Watchdog Timer, which may be software programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not desired.

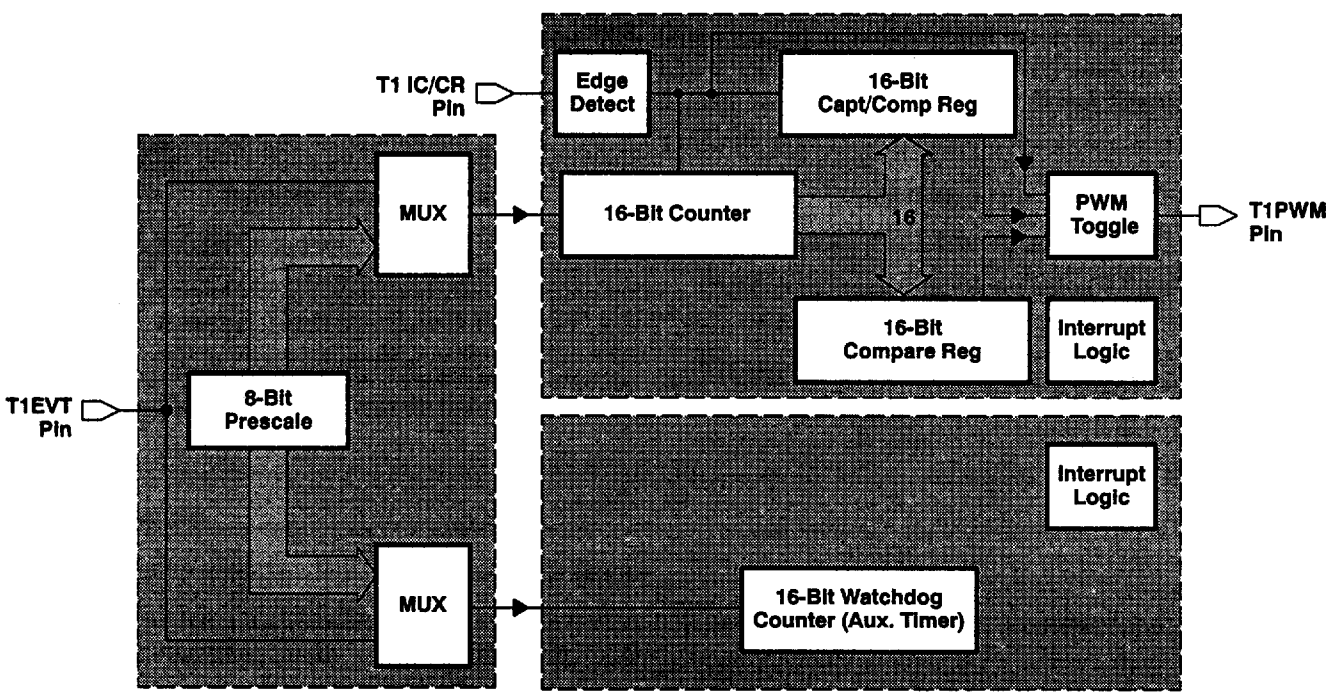


Figure 7. Timer 1 Module Block Diagram

timer 1 module prescaler/clock source

The clock source inputs for the general purpose timer and the watchdog timer are independently configured by the T1 and WD INPUT SELECT control bits of the T1CTL1 cotnrol register. The WD INPUT SELECT control bits cannot be changed after entering the watchdog mode (WD RST ENA = 1). Eight possible clock sources are programmable for each counter.

T1 INPUT				WD INPUT		
SELECT 2	SELECT 1	SELECT 0		SELECT 2	SELECT 1	SELECT 0
0	0	0	System Clock	0	0	0
0	0	1	Pulse Accumulate	0	0	1
0	1	0	Event Input	0	1	0
0	1	1	No Clock Input	0	1	1
1	0	0	System Clock/4	1	0	0
1	0	1	System Clock/16	1	0	1
1	1	0	System Clock/64	1	1	0
1	1	1	System Clock/256	1	1	1

For realtime control applications, both the general-purpose timer and the watchdog timer are independently programmable from 15 to 24 bits in length. The 24-bit prescaler/timer generates overflow rates ranging from 13.1 ms with 200 ns timer resolution to 3.35 seconds with 51.2 μs timer resolution (external clock = 20 MHz).

In the **Event Counter mode**, an external high-to-low transition on the T1EVT pin is used to provide the clock for the internal timers. As shown in Figure 8, the T1EVT input provides the timer clock and is not routed through the prescaler. The T1EVT external clock frequency may not exceed the system clock frequency divided by 2. The general-purpose timer and the watchdog timer are programmable as 16-bit event counters.

In the **Pulse Accumulate mode**, an external input on the T1EVT pin is used to gate the internal system clock to the internal timers. While T1EVT input is logic one (high), the timers will be clocked at the system clock rate and will accumulate system clock pulses until the T1EVT pin returns to logic zero. Both the general purpose timer and the watchdog timer are programmable as 16-bit pulse accumulators.

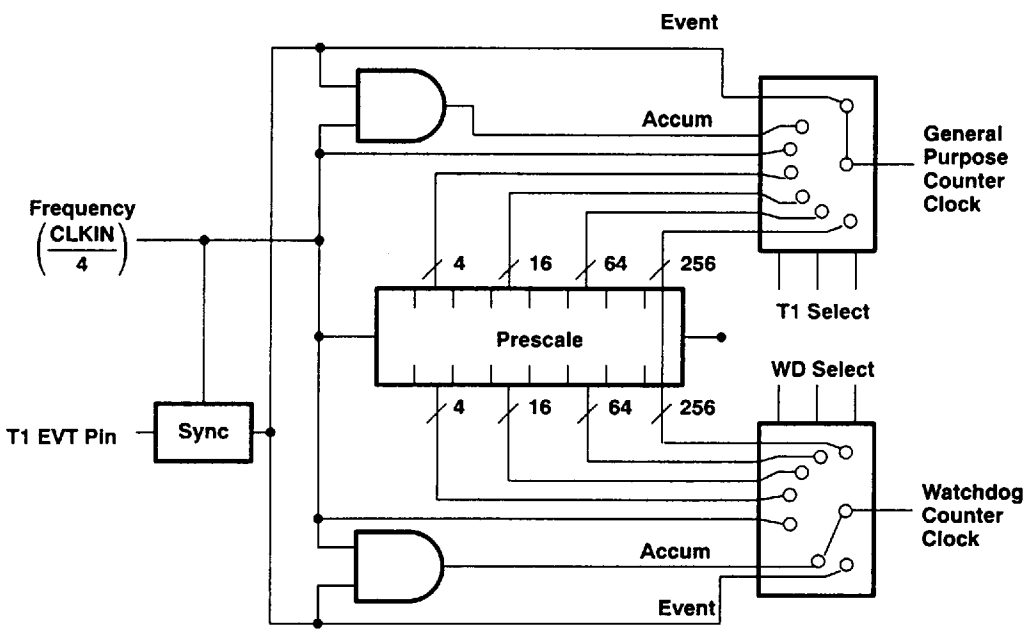


Figure 8. Timer 1 Counter Prescaler

T-49-19-01

timer 1 general purpose timer

The 16-bit general purpose timer, T1, is composed of a 16-bit resettable counter, a 16-bit compare register and associated compare logic, and a 16-bit register that functions as a capture register in one mode and a compare register in the other mode. The T1 MODE bit selects whether T1 operates in the Capture/Compare mode or the Dual Compare mode.

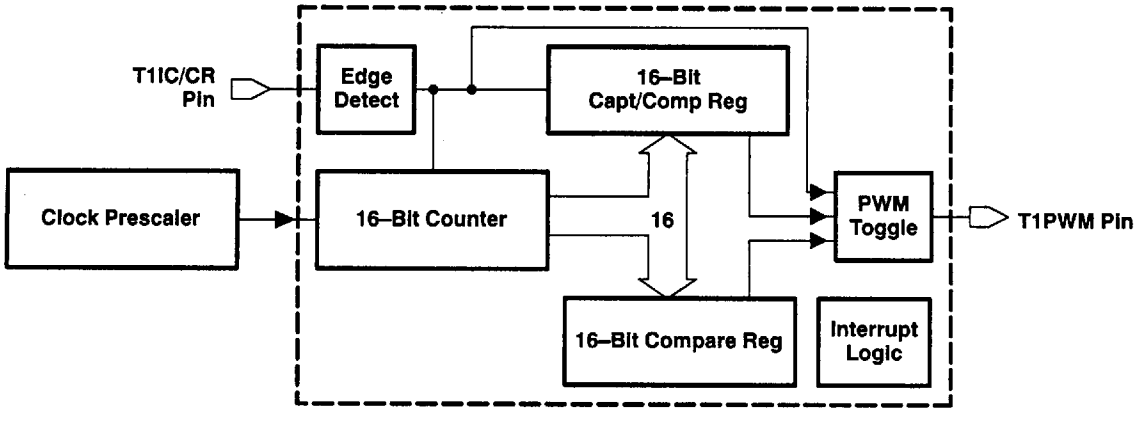


Figure 9. Timer 1 — General Purpose Timer

The counter is a free-running, 16-bit up-counter, clocked by the output of the Prescaler/Clock source. During initialization the counter is loaded with 0000h and begins its up-count. If the counter is not reset before reaching FFFFh, the counter will roll over to 0000h and continue counting. Upon counter roll-over, the T1 OVRFL INT FLAG is set to 1, and a timer interrupt is generated if the T1 OVRFL INT ENA bit is set to 1.

The counter may be reset to 0000h during counting by either; 1) writing a 1 to the T1 SW RESET bit; 2) a compare equal condition from the dedicated T1 compare function; or 3) an external pulse on the T1 IC/CR pin (Dual Compare mode). The designer may select via software (T1 EDGE POLARITY bit) which external transition, low-to-high or high-to-low, on the T1IC/CR pin will cause the counter to be reset.

Special circuitry prevents the 16-bit registers, including the Counter, Compare, or Capture registers, from changing in the middle of a 16-bit read or write operation. When reading a 16-bit register, read the LSB first and then read the MSB. When writing to a 16-bit register, write the MSB first and then write the LSB. The register value will not change between reading or writing the bytes when done in this order.

The timer 1 module has three I/O pins used for the functions shown in the following table. Any of these three pins not used in a timer application may be individually configured as general purpose digital I/O pins by the timer 1 module port control registers (T1PC1 and T1PC2).

Timer 1 Module I/O Pin Functions

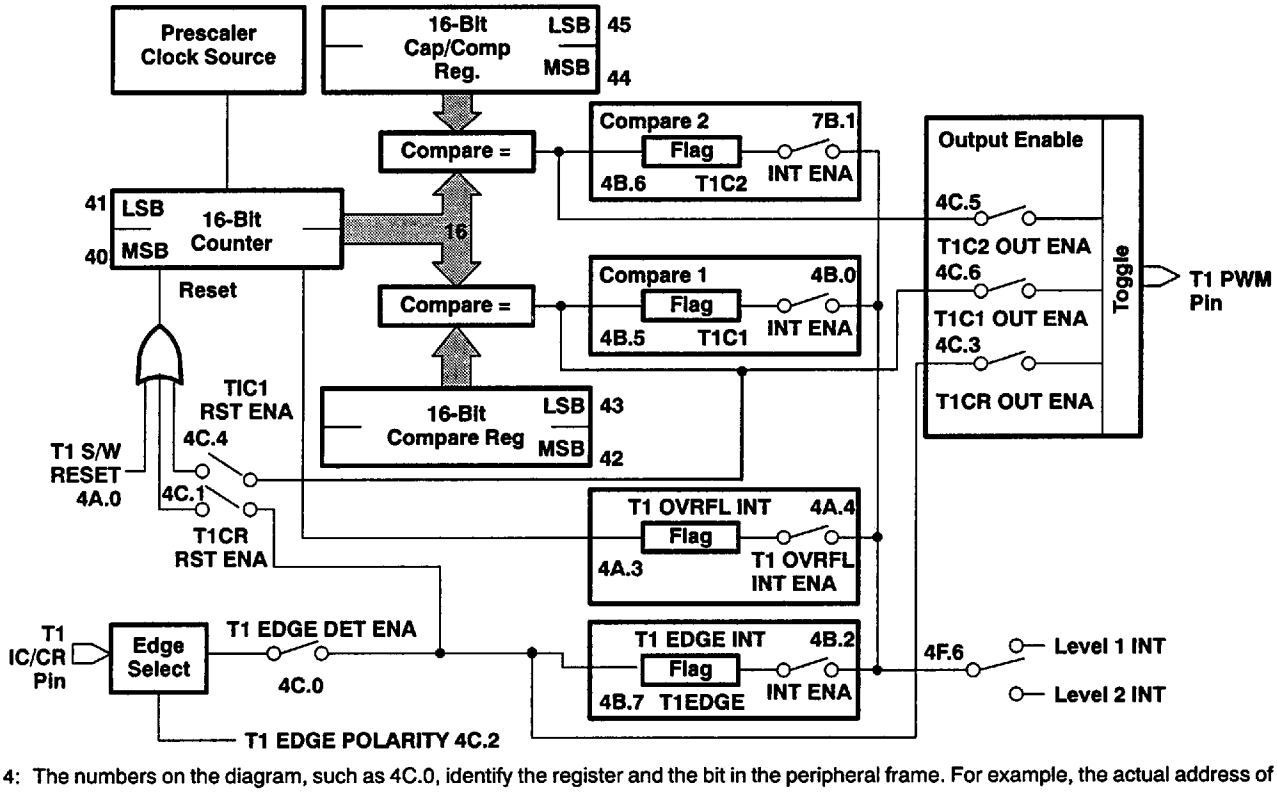
PIN	DUAL COMPARE MODE	CAPTURE/COMPARE MODE
T1IC/CR	Counter Reset input	Input Capture input
T1PWM	PWM output	Compare output
T1EVT	External Event input or Pulse Accumulate input	External Event input or Pulse Accumulate input

The **Dual Compare mode** (T1 MODE = 0) provides two compare registers, an external resettable counter, and a timer output pin. These allow the timer to act as an interval timer, a PWM output, simple output toggle, or many other timer functions. The Dual Compare mode as shown in Figure 10 continuously compares the contents of the two compare registers to the current value of the 16-bit counter. If a timer compare register equals the counter, the circuit sets the associated interrupt flag to 1 and toggles the T1PWM output pin if enabled, and/or

generates a Timer 1 interrupt. An output compare equal condition from the dedicated compare register can also initiate a counter reset. A programmable interval timer function, selected by using the compare equal condition to generate a system interrupt and the counter reset function, generates a periodic interrupt.

Either compare function may be used to toggle the T1PWM output pin when a timer compare equal occurs, while the other compare function may be used for another system timing function. Using both compare functions to control the T1PWM pin allows direct PWM generation with minimal CPU software overhead. In typical PWM applications, the compare register is written with the periodic interval and is configured to allow counter reset on compare equal, and the Capture/Compare register is written with the pulse width to be generated within that interval. The program pulse width may be changed by the application program during the timer operation to alter the PWM output. For high-speed control applications, a minimum pulse width of 200 ns and a period as low as 400 ns can be maintained when using a clock of 20 MHz.

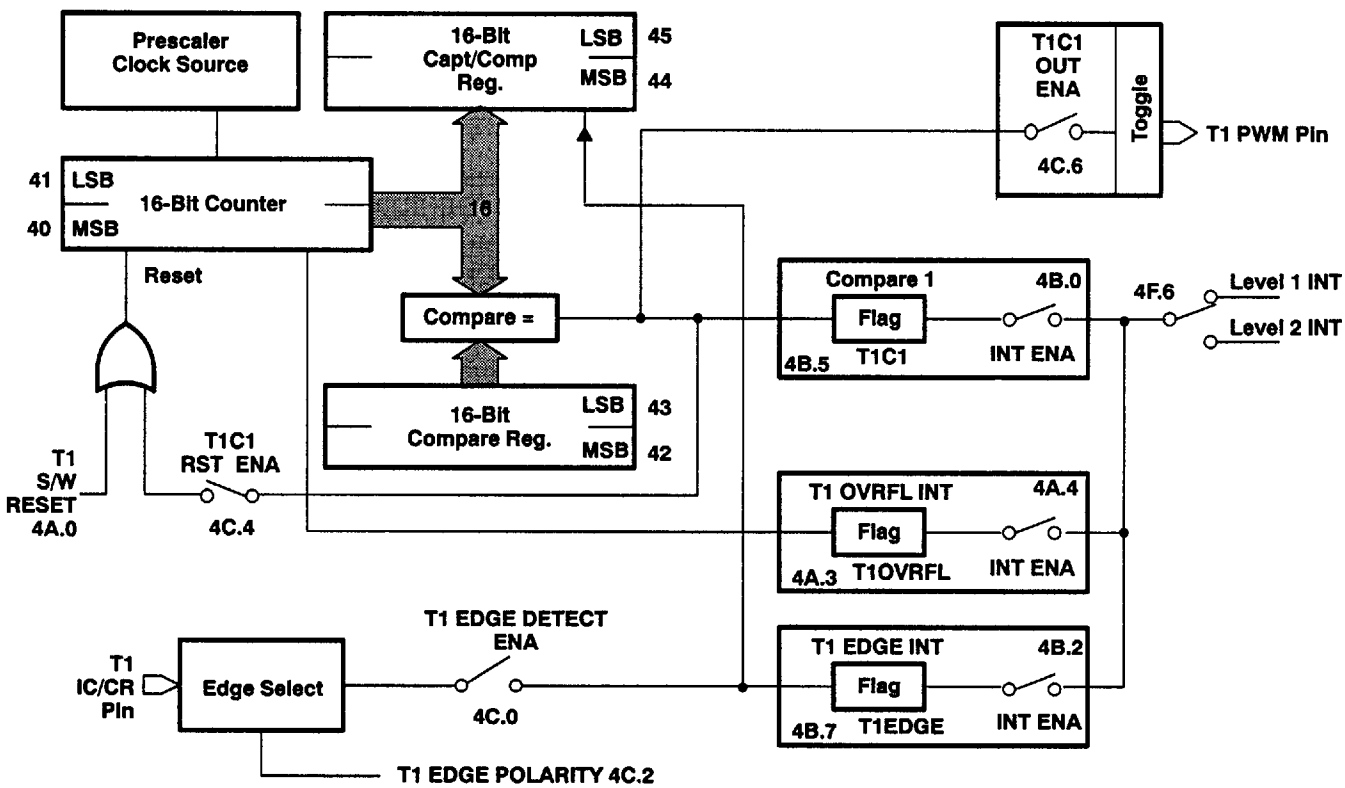
In addition, a PWM output that is initiated by a transition on an external pin is provided by the timer hardware to support time-critical control applications. Typically, in these applications an external input (T1IC/CR) is used to reset the counter, generate a timer interrupt, and toggle the T1PWM pin to start the PWM output. The compare function will then toggle the output after the programmed pulse width has elapsed. The input edge detect function is enabled under program control by the T1CR DET ENA bit, and upon the next occurrence of the selected edge transition, the T1EDGE INT FLAG bit is set to 1, a timer interrupt is generated (if T1EDGE INT ENA = 1), and the T1PWM output pin is toggled (if T1CR OUT ENA = 1). Selection of the active input transition is under control of T1EDGE POLARITY. In the Dual Compare mode, the edge detect function must be re-enabled after each valid edge detect.



NOTE 4: The numbers on the diagram, such as 4C.0, identify the register and the bit in the peripheral frame. For example, the actual address of 4C.0 is 104Ch, bit 0, in the T1CTL4 register.

Figure 10. Timer 1 — Dual Compare Mode

In the **Capture/Compare mode** (T1 MODE = 1), T1 is configured to provide one input capture register for external timing and pulse width measurement, and one compare register for use as a programmable interval timer. The compare register in this mode functions the same as in the Dual Compare mode described above, including the ability to toggle the PWM pin. The capture/compare register functions in this mode as a 16-bit input capture register, as shown in Figure 11. On the occurrence of a valid input on the T1IC/CR pin, the current counter value is loaded into the 16-bit input capture register, the T1 EDGE INT FLAG is set to 1, and a timer interrupt is generated (if TI EDGE INT ENA = 1). The input detect function is enabled by the T1 EDGE DET ENA bit, with T1 EDGE POLARITY selecting the active input transition. In the Capture/Compare mode, the edge detect function, once enabled, remains enabled following a valid edge detect.



NOTE 4: The numbers on the diagram, such as 4C.0, identify the register and the bit in the peripheral frame. For example, the actual address of 4C.0 is 104Ch, bit0, in the T1CTL4 register.

Figure 11. Timer 1 — Capture/Compare Mode

timer 1 module watchdog timer

The watchdog timer, contained in the timer 1 module, is a free-running 16-bit resettable up-counter clocked by the output of the Prescaler/Clock Source. The timer is software configured as either a watchdog timer to protect against system software failures and corruption, or as a general purpose timer if the watchdog function is not desired. The 16-bit up-counter is programmable (via the WD OVRFL TAP SEL bit) to set the initial count at either 0000h or 8000h. The current value of the watchdog timer may be read at any time during its operation.

In the **Watchdog mode** (WD OVRFL RST ENA = 1), the timer will generate a system reset if the timer is re-initialized by an incorrect value or if the counter overflows. The required re-initialization frequency is determined by the system clock frequency, the prescaler/clock source selected, and whether the WD OVRFL TAP SEL bit is set for 15 or 16 bit counter rollover. With a clock = 20 MHz, the watchdog timer overflow rates range form 6.55 ms to 3.35 seconds. These values are selected prior to entering the watchdog mode because once the software enables the watchdog reset function (WD OVRFL RST ENA set to 1), subsequent writes to these control bits are ignored. Writes to these watchdog control bits can occur only following a powerup reset, which enhances watchdog timer system integrity.

The watchdog timer is re-initialized by writing a predefined value to the watchdog reset key (WDRST) located in the peripheral file. The proper reset key alternates between 55h and AAh, beginning with 55h following the enable of the watchdog reset function. Writes of the correct value must occur prior to the timer overflow period. A write of any value other than the correct predefined value to the watchdog reset key will be interpreted as a lost program and a system reset will be initiated. A watchdog timer overflow or incorrect reset key will set the WD OVRFL INT FLAG bit to 1 and may be interrogated by the program following system reset to determine the source of the reset.

In the **Non-watchdog mode** (WD OVRFL RST ENA = 0), the watchdog timer may be used as an event counter, pulse accumulator, or as an interval timer. In this mode, the system reset function is disabled. The watchdog counter is re-initialized by writing any value to the watchdog reset key (WDRST). In real-time control applications, the timer overflow rates are determined by the system clock frequency, the prescaler/clock source value selected, and the value of the WD OVRFL TAP SEL bit. If the WD counter is not reset before overflowing, the counter will roll over to either 0000h or 8000h, as determined by the WD OVRFL TAP SEL bit, and continue counting. Upon counter overflow, the WD OVRFL INT FLAG is set to 1 and a timer interrupt is generated if the WD OVRFL INT ENA bit set to 1. Alternately, an external input on the T1EVT pin may be used with the watchdog timer to provide an additional 16-bit event counter or pulse accumulator.

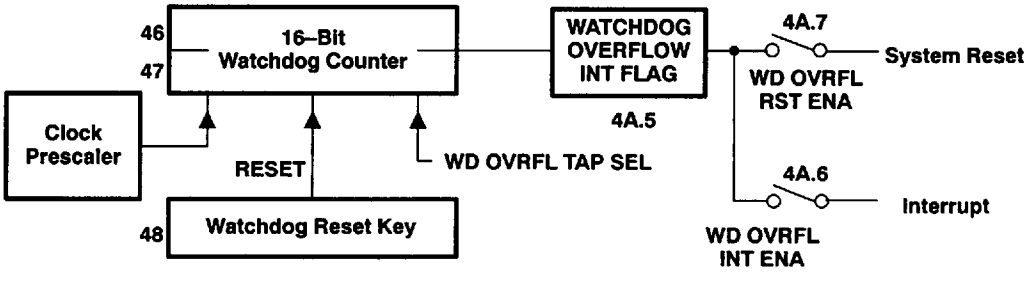


Figure 12. Watchdog/General Purpose Timer

T-49-19-01

Peripheral File Frame 4: Timer 1 Module Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
1040h	P040	Bit 15			Counter MSB				Bit 8	T1CNTR
1041h	P041	Bit 7			Counter LSB				Bit 0	
1042h	P042	Bit 15			Compare Register MSB				Bit 8	T1C
1043h	P043	Bit 7			Compare Register LSB				Bit 0	
1044h	P044	Bit 15			Capture/Compare Register MSB				Bit 8	T1CC
1045h	P045	Bit 7			Capture/Compare Register LSB				Bit 0	
1046h	P046	Bit 15			Watchdog Counter MSB				Bit 8	WDCNTR
1047h	P047	Bit 7			Watchdog Counter LSB				Bit 0	
1048h	P048	Watchdog Reset Key								WDRST
1049h	P049	WD OVRFL TAP SEL†	WD INPUT SELECT 2†	WD INPUT SELECT 1†	WD INPUT SELECT 0†	—	TI INPUT SELECT 2	TI INPUT SELECT 1	TI INPUT SELECT 0	T1CTL1
104Ah	P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	TI OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual Compare										
104Bh	P04B	T1 EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1 EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
104Ch	P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare										
104Bh	P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1 EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
104Ch	P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
104Dh	P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
104Eh	P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
104Fh	P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI

† Subsequent writes to these control bits are ignored after the WD OVRFL RST ENA bit is set to 1 (see **timer1 module watchdog timer**) and can be initialized only following a **powerup reset**.

The formulas in Figure 13 show the calculations for the resulting time, given values in the compare registers T1C and T1CC.

$$\text{time} = \left(\frac{4}{\text{CLKIN}}\right) (\text{prescale}) (\text{compare} + 1)$$

or

$$\text{time} = t_c (\text{prescale}) (\text{compare} + 1)$$

Figure 13. Timer 1 Compare Register Formulas

serial peripheral interface (SPI)

The Serial Peripheral Interface (SPI) is a high-speed synchronous serial I/O port that allows a serial bit stream of programmed length (one to eight data bits) to be shifted into and/or out of the device at a programmed bit transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion using devices such as shift registers, display drivers, A/D converters, etc. Multiprocessor communications are also supported by the master/slave operation of the SPI.

Three I/O pins are associated with the SPI. These include the SPI slave-in master-out (SPISIMO), SPI slave-out master-in (SPISOMI), and SPI serial serial clock (SPICLK). These I/O pins can be configured for three-wire full-duplex transmit/receive or two-wire receive or transmit only. Any of these three pins not used in an SPI application may be individually configured as general purpose digital I/O pins controlled by SPIPC1 and SPIPC2.

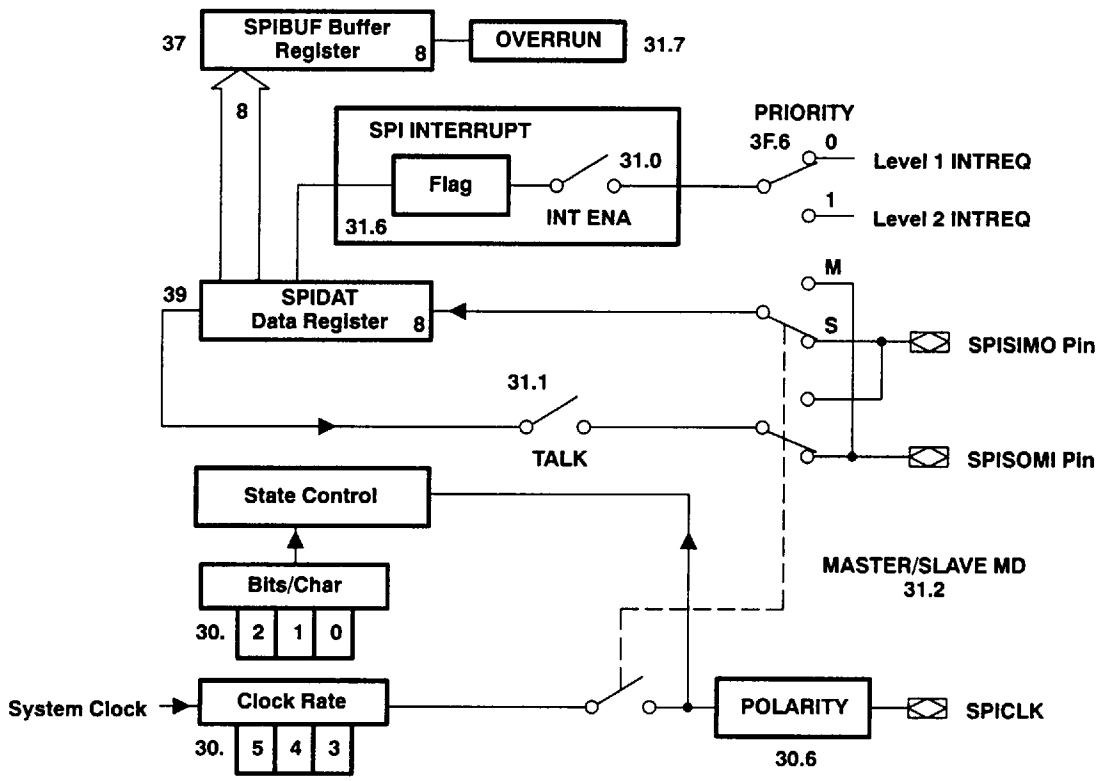


Figure 14. SPI Block Diagram

A variety of multiprocessor configurations can be supported, ranging from single master with multiple slaves to multi-master systems. General purpose I/O pins can be used to implement the slave enables and multi-master hardware handshakes between microcontrollers in the network.

The MASTER/SLAVE bit of the SPICTL control register determines if the SPI operates in the master or slave mode. Master or slave data transmission can be disabled by writing a zero to the TALK bit of the SPICTL control register, forming a two-wire receive-only network (SPICLK and data in).

In the **Master mode** (MASTER/SLAVE = 1), the SPI provides the serial clock on the SPICLK pin for the entire serial communications network. The SPICCR register (SPI BIT RATE2, RATE1, RATE0) determines the bit transfer rate for the network, both transmit and receive. For any specific system clock frequency, there are eight data transfer rates that can be selected by these control bits. The data transfer rate is defined by selecting a one-of-eight divide-by of the system clock frequency (divide-by-2, -4, -8, -16, -32, -64, -128, and -256).

$$\text{SPI Baud Rate} = \frac{\text{CLKIN}}{8 \times 2^{b}}$$

T-49-19-01

where b = bit rate in SPICCR bit 3, 4, 5 (range 0-7).

Data written to the SPIDAT register initiates data transmission on the SPISIMO pin, MSB of data transmitted first.Simultaneously, received data is shifted in the SPISOMI pin into the SPIDAT register, and upon completion of transmitting the selected number of bits, the data is transferred to the SPIBUF (double buffered receiver) for reading by the CPU to permit new transactions to take place. Data is shifted into the SPI the most significant bit first, there it is stored right-justified in the SPIBUF. To receive a character when operating as a master, data must be written to the SPIDAT to initiate the transaction. When the specified number of data bits have been shifted into or out of the SPIDAT register, the SPI INT FLAG bit is set and if the SPI INT ENA bit is set to one, an Interrupt is asserted.

In the **Slave mode** (MASTER/SLAVE = 0), data shifts out on the SPISOMI pin and in on the SPISIMO pin. The SPICLK pin is used as the input for the serial shift clock, which is supplied from the external network master. The transfer rate is defined by the input clock on the SPICLK pin, which is supplied from the network master. The SPICLK input frequency should be no greater than system clock frequency divided by eight.

Data written to the SPIDAT register will be transmitted to the network when the SPICLK is received from the network master. To receive data, the SPI waits for the network master to send SPICLK and then shifts the data on the SPISIMO pin into the SPIDAT register. If data is to be transferred by the slave simultaneously, then it must be written to the SPIDAT register prior to the beginning of SPICLK.

Compatibility with the broadest range of existing peripheral devices is provided by the SPI through its software programmable transmit/receive character length, bit transfer rate, and clock polarity. A character length from one to eight data bits is selected by writing to the SPICCR control register (SPI CHAR2, CHAR1, and CHAR0) to specifically match the peripheral's data length requirements, thereby not requiring the overhead of data bit padding during communications. Applications requiring more than eight bits of serial data use multiple back-to-back SPI operations.

External peripherals enable output data on either the rising or the falling edge of the serial clock, while latching incoming data on the opposite edge. The SPI supports data transfer using either of these approaches. The CLOCK POLARITY bit controls the steady-state or at-rest condition of the SPICLK signal. This bit affects both master and slave modes of operation. When CLOCK POLARITY is set to 1, the at-rest level of SPICLK is a logic one (high). Data is enabled at the output on the falling edge of SPICLK, and data is latched by the network master and slaves on the rising edge of SPICLK. When CLOCK POLARITY is set to zero, the at-rest level of SPICLK is a logic zero (low). Data is enabled for output on the rising edge of SPICLK, and data is latched by the network master on the falling edge of SPICLK.

Peripheral File Frame 3: Serial Peripheral Interface (SPI) Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
1030h	P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE 0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
1031h	P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/ SLAVE	TALK	SPI INT ENA	SPICTL
1032h to 1036h	P032 to P036	Reserved								
1037h	P037	SPI Receive Data Buffer Register								SPIBUF
1038h	P038	Reserved								
1039h	P039	SPI Serial Data Register								SPIDAT
103Ah to 103Dh	P03A to P03C	Reserved								
103Dh	P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
103Eh	P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
103Fh	P03F	**SPI STEST**	**SPI PRIORITY**	**SPI ESPEN**	—	—	—	—	—	SPIPRI

instruction set

T-49-19-01

The TMS370 family instruction set consists of 73 instructions that control input, output, data manipulations, data comparisons, and program flow. The instruction set is supported with 14 addresssing modes to provide the flexibility to optimize programs to the user's applications. For example, the MOV instruction has 27 operand combinations supported by its addressing modes.

ADDRESSING MODE	EXAMPLE		OPERATION
GENERAL:			
Implied	LDSP		(B) → (SP)
Register	MOV	R5,R4	(0005) → (0004)
Peripheral	MOV	P025,A	(1025) → A
Immediate	ADD	#123,R3	123 + (03) → (03)
PC Relative	JMP	offset	PCN + offset → (PC)
Stack Pointer Relative	MOV	2(SP),(A)	(2 + (SP)) → (A)
EXTENDED:			
Absolute Direct	MOV	A,1234	(A) → (1234)
Absolute Indexed	MOV	1234(B),A	(1234) + (B) → (A)
Absolute Indirect	MOV	@R4,A	((R3:R4)) → (A)
Absolute Offset Indirect	MOV	12(R4),A	(12 + (R3:R4)) → (A)
Relative Direct	JMPL	1234	PCN + 1234 → (PC)
Relative Indexed	JMPL	1234(B)	PCN + 1234 + (B) → (PC)
Relative Indirect	JMPL	@R4	PCN + (R3:R4) → (PC)
Relative Offset Indirect	JMPL	12(R4)	PCN + 12 + (R3:R4) → (PC)

PCN = 16-bit address of next instruction.
(x) = Contents of memory at address x.
((x)) = Contents of memory location designated by contents at address x.

The CPU controls instruction execution by executing microinstructions from a dedicated control memory at a rate of one microinstruction per internal system clock cycle, t_c. The number of system clock cycles required to execute one assembly language instruction varies depending on the instruction complexity, operand addressing mode, and number of wait states. Instruction execution times are stated in terms of the number of internal system clock cycles per instruction. Instruction execution times vary from 5 to 63 internal system clock cycles, with most instructions requiring less than 10 cycles to complete.

Similarly, the number of bytes of program memory required to store an instruction will vary with instruction complexity and addressing mode. TMS370 instructions require from one to five bytes of program memory space, with most instructions occupying one or two bytes.

The TMS370 INSTRUCTION SET SUMMARY, beginning on page 28, shows the instruction set, the addressing modes, the program memory byte length, and the execution cycle count for each instruction. The Addressing Mode entries are in the format of BYTE LENGTH/CYCLE COUNT. The following symbols and abbreviations are used:

SYMBOL	DEFINITION	SYMBOL	DEFINITION
s	Source Operand	d/D	Destination Operand (8-bit/16-bit)
A	Register A or R0 in Register File	B	Register B or R1 in Register File
Rs	Source Register in Register File	Rd	Destination Register in Register File
Ps	Source Register in Peripheral File	Pd	Destination Register in Peripheral File
Rps	Source Register Pair (Rn, Rn-1)	Rpd	Destination Register Pair (Rn, Rn-1)
Rp	General Purpose Register Pair	label	16-bit Label
iop8	8-bit Immediate Operand	iop16	16-bit Immediate Operand
off8	8-bit Signed Offset (label – PCN)	off16	16-bit Signed Offset
PC	Program Counter	PCN	16-bit Address of Next Instruction
SP	Stack Pointer	ST	Status Register
#	Immediate Operand	@	Indirect Addressing Operand
C	Status Register Carry Bit	XADDR	16-bit Address
( )	Contents of	→	Is Assigned to

TMS370 Instruction Set Summary

OPERATION		ADDRESSING MODES										DESCRIPTION
		DIRECT				EXTENDED						
		A	B	Rd	Pd	label	@Rp	label(B)	off8(Rp)	off8(SP)	OTHER	
ADC	B, __	1/8										Add with Carry
	Rs, __	2/7	2/7	3/9								(s) + (d) + (C) → (d)
	#iop8, __	2/6	2/6	3/8								
ADD	B, __	1/8										Add
	Rs, __	2/7	2/7	3/9								(s) + (d) → (d)
	#iop8, __	2/6	2/6	3/8								
AND	A, __				2/9							And
	B, __	1/8			2/9							(s) AND (d) → (d)
	Rs, __	2/7	2/7	3/9								
	#iop8, __	2/6	2/6	3/8	3/10							
BR						3/9	2/8	3/11	4/15			Branch; D → XADDR
BTJO†	A, __,off8				3/10							Bit Test and Jump If One
	B, __,off8	2/10			3/10							If (s) AND (d) ≠ 0 then
	Rs, __,off8	3/9	3/9	4/11								PCN + offset → (PC)
	#iop8, __,off8	3/8	3/8	4/10	4/11							
BTJZ†	A, __,off8				3/10							Bit Test and Jump If Zero
	B, __,off8	2/10			3/10							If (s).AND.(not d) ≠ 0 then
	Rs, __,off8	3/9	3/9	4/11								PCN + offset → (PC)
	#iop8, __,off8	3/8	3/8	4/10	4/11							
CALL	__					3/13	2/12	3/15	4/19			Call; Push PCN, D → XADDR
CALLR	__					3/15	2/14	3/17	4/21			Call Relative
												Push PCN, PCN + XADDR → (PC)
CLR	__	1/8	1/8	2/6								Clear; 0 → (d)
CLRC											1/19	Clear Carry; 0 → (C)
CMP	__,A					3/11	2/10	3/13	4/17	2/8		Compare
	B, __	1/8										(d) – (s) computed and
	Rs, __	2/7	2/7	3/9								Status Register flags set
	#iop8, __	2/6	2/6	3/8								
CMPBIT	__			3/8	3/10							Complement Bit (One's complement)
CMPL	__	1/8	1/8	2/6								Two's complement;
												0100h – (s) → (d)
DAC	B, __	1/10										Decimal Add with Carry
	Rs, __	2/9	2/9	3/11								(s) + (d) + (C) → (d) (BCD)
	#iop8, __	2/8	2/8	3/10								
DEC	__	1/8	1/8	2/6								Decrement; (d) – 1 → (d)
DINT											2/6	Disable Interrupt; 00 → (ST)
DIV	Rs, __	3/47-63‡										Integer Divide; 16 by 8-bit
												A:B/Rs → A(=quo), B(=rem)
												# cycles depends on operands
DJNZ†	__,off8	2/10	2/10	3/8								Decrement and Jump If Not 0
												(d) – 1 → (d); if (d) ≠ 0
												then PCN + offset → (PC)

† Add 2 to cycle count if jump is taken.
‡ Actual number of cycles is 14 if the quotient is greater than 8 bits (overflow condition).

T-49-19-01

TMS370 Instruction Set Summary (continued)

OPERATION		ADDRESSING MODES										DESCRIPTION
		DIRECT				EXTENDED						
		A	B	Rd	Pd	label	@Rp	label(B)	off8(Rp)	off8(SP)	OTHER	
DSB	B, __	1/10										Decimal Subtract with Borrow
	RS, __	2/8	2/9	3/11								(d) – (s) – 1 + (C) → (d) (BCD)
	#iop8, __	2/8	2/8	3/10								
EINT											2/6	Enable Interrupts; 0Ch → (ST)
EINTH											2/6	EINT High Priority; 04h → (ST)
EINTL											2/6	EINT Low Priority; 08h → (ST)
IDLE											1/6	Idle Until Interrupt, Low Power entry
INC	__	1/8	1/8	2/6								Increment; (d) + 1 → (d)
INCW	#off8, __			3/11								(Rp) + offset → (Rp)
INV	__	1/8	1/8	2/6								Invert; NOT (d) → (d)
JMP	__										2/7	Jump; PCN + offset8 → (PC)
JMPL	__					3/9	2/8	3/11	4/15			Jump; PCN + XADDR → (PC)
Jcnd†											2/5	Jump Conditional
JN											2/5	Negative
JZ											2/5	Zero
JC											2/5	Carry
JP											2/5	Positive
JPZ											2/5	Positive or Zero
JNZ											2/5	Negative or Zero
JNC											2/5	No Carry
JV											2/5	Overflow, signed
JNV											2/5	No Overlfow, signed
JGE											2/5	Greater Than or Equal, signed
JL											2/5	Less Than, signed
JG											2/5	Greater Than, Signed
JLE											2/5	Less Than or Equal, signed
JL0											2/5	Lower Value
JHS											2/5	Higher or Same
JBIT0†	__			4/10	4/11							Jump If Bit = 0
JBIT1†	__			4/10	4/11							Jump If Bit = 1
LDSP											1/7	Load Stack Pointer; (B) → (SP)
LDST	#iop8										2/6	Load ST Register; (s) → (SP)
MOV	A, __		1/9	2/7	2/8	3/10	2/9	3/12	4/16	2/7		Move; (s) → (d)
	__, A		1/8	2/7	2/8	3/10	2/9	3/12	4/16	2/7		
	B, __	1/8		2/7	2/8							
	Rs, __	2/7	2/7	3/9	3/10							
	Ps, __	2/8	2/8	3/10								
	#iop8, __	2/6	2/6	3/8	3/9							
MOVW	Rps, __			3/12								Move Word; 16-bit operands
	#iop16, __			4/13								(s) → (d)
	#iop16(B), __			4/15								
	#off8(Rp), __			5/19								

† Add 2 to cycle count if jump is taken.

TMS370 Instruction Set Summary (concluded)

OPERATION		ADDRESSING MODES										DESCRIPTION
		DIRECT				EXTENDED						
		A	B	Rd	Pd	label	@Rp	label(B)	off8(Rp)	off8(SP)	OTHER	
MPY	B, __	1/47										Multiply
	RS, __	2/46	2/46	3/48								(s) × (d) → (A:B)
	#iop8, __	2/45	2/45	3/47								A = MSB, B = LSB
NOP											1/7	NOP; (PC) +1 → (PC)
OR	A, __				2/9							OR
	B, __	1/8			2/9							(s) OR (d) → (d)
	Rs, __	2/7	2/7	3/9								
	#iop8, __	2/6	2/6	3/8	3/10							
POP	__	1/9	1/9	2/7							1/8	Pop Top of Stack
												((SP)) → (d); (SP) – 1 → (SP)
PUSH	__	1/9	1/9	2/7							1/8	Push onto Stack
												(SP) + 1 → (SP); (s) → ((SP))
RL	__	1/8	1/8	2/6								Rotate Left
RLC	__	1/8	1/8	2/6								Rotate Left Through Carry
RR	__	1/8	1/8	2/6								Rotate Right
RRC	__	1/8	1/8	2/6								Rotate Right Through Carry
RTI											1/12	Return from Interrupt
												Pop PC, Pop ST
RTS											1/9	Return from Subroutine, Pop PC
SBIT0	__			3/8	3/10							Set Bit to 0
SBIT1	__			3/8	3/8							Set BIT to 1
SETC											17	Set Carry; A0h → (ST)
SSB	B, __	1/8										Subtract with Borrow
	Rs, __	2/7	2/7	3/9								(d) – (s) – 1 + (C) → (d)
	#iop8, __	2/6	2/6	3/8								
STSP											1/8	Store Stack Pointer; (SP) → (B)
SUB	B, __	1/8										Subtract
	Rs, __	2/7	2/7	3/9								(d) – (s) → (d)
	#iop8, __	2/6	2/6	3/8								
SWAP	__	1/11	1/11	2/9								Swap Nibbles
												s(7-4,3-0) → d(3-0,7-4)
TRAPn											1/14	Trap to Subroutine; Push PCN;
												Vector n → (PC)
TST	__	1/9	1/10									Test; Set flags from register
XCHB	__	1/10	1/10	2/8								Exchange B; (B) ↔ (d)
XOR	A, __				2/9							Exclusive OR
	B, __	1/8			2/9							(s) XOR (d) → (d)
	Rs, __	2/7	2/7									
	#iop8, __	2/6	2/6	3/8	3/10							

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T-49-19-01

TMS370 Family OPCODE/Instruction Map

SECOND NIBBLE	FIRST NIBBLE 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP ra 2/7							INCW #n,Rd 3/11	MOV Pa,A 2/8			CLRC TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2.5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,Rd 3/10				MOV B,Rd 2/7	TRAP 14 1/14	MOV n(SP),A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOF #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rn 2/8	TRAP 13 1/14	MOV A,n(SP) 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/7	AND Rs,B 3/9	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 2/9	INC A 1/8	INC B 1/8	INC Rn 2/6	TRAP 12 1/14	CMP n(SP),A 2/8
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rn 2/6	TRAP 11 1/14	extend inst,2 opcodes
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
6	JNZ ra 2/5	BTJO Rs,A 3/9	BTJO #n,A 3/8	BTJO B,Pd 3/9	BTJO Rs,Rd 4/11	BTJO #n,B 3/8	BTJO B,A 2/10	BTJO #n,Rd 4/10	BTJO A,Pd 3/11	BTJO B,Pd 3/10	BTJO #n,Pd 4/11	XCHB A 1/10	XCHB TESTB 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
7	JNC ra 2/5	BTJZ Rs,A 3/9	BTJZ #n,A 3/8	BTJZ Rs,B 3/9	BTJZ Rs,Rd 4/11	BTJZ #n,B 3/8	BTJZ B,A 2/10	BTJZ #n,Rd 4/10	BTJZ A,Pd 3/10	BTJZ B,Pd 3/10	BTJZ #n,Pd 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16(B),Rd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rs 2/7	TRAP 7 1/14	SETC 1/7
9	JL ra 2/5	ADC Rs,A 2/7	SX #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL @Rd 2/8	JMPL lab(B) 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A	JLE ra 2/5	SUB Rs,A 2/6	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB B,A 1/8	MOV lab,A 3/10	MOV @Rs,A 2/9	MOV lab(B),A 3/12	DJNZ A,ra 2/10	DJNZ B,ra 2/10	DJNZ Rn,ra 3/8	TRAP 5 1/14	RTI 1/12
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SUB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A,lab 3/10	MOV A,@Rd 2/9	MOV A,lab(B) 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rn 2/6	TRAP 4 1/14	PUSH ST 1/8
C	JNV ra 2/5	MPy Rs, A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 2/46	MPY #n,B 2/48	MPY B,A 1/47	MPY #n,Rd 3/47	BR lab 3/9	BR @Rd 2/8	BR lab(B) 1/8	RR A 1/8	RR B 1/8	RR Rn 2/6	TRAP 3 1/14	POP ST 1/8
D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP lab,A 3/11	CMP @Rs,A 2/10	CMP lab(B),A 3/13	RRC A 1/8	RRC B 1/8	RRC Rn 2/6	TRAP 2 1/14	LDSP ST 1/7
E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL @Rd 2/12	CALL lab(B) 3/13	RL A 1/8	RL B 1/8	RL Rn 2/6	TRAP 1 1/14	STSP ST 1/8
F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR @Rd 2/14	CALLR lab(B) 3/17	RLC A 1/8	RLC B 1/8	RLC Rn 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

	E	F
8	MOVW n(Rn) 4/15	DIV Rn,A 3/14-63
9	JMPL n(Rn) 4/16	
A	MOV n(Rn),A 4/17	
B	MOV A,n(Rn) 4/16	
C	BR n(Rn) 4/16	
D	CMP n(Rn) 4/18	
E	CALL n(Rn) 4/20	
F	CALLR n(R) 4/22	

ra — relative address
Rn — Register
Rs — Register containing source byte
Rd — Register containing destination byte
Ps — Peripheral register containing source byte
Pd — Peripheral register containing destination byte
Pn — Peripheral register
#n — Immediate 8-bit number
#16 — Immediate 16-bit number
lab — 16-bit label
@Rn — 16-bit address of contents of register pair

development system support

The TMS370 family development support tools include an Assembler, a C-Compiler, a Linker, an In-Circuit emulator (XDS – eXtended Development Support), and an EEPROM/UVEPROM programmer. All of the tools work closely together using any MS ™-DOS-Based Personal Computer (PC) or a VMS ™-based DEC VAX™ computer as the host and central control element. This allows selection of the host computer and the text management and editing tools based on user preference.

- Assembler/Linker (Part Number TMDS3740810-02 for PC, Part No. TMDS3740210-08 for VAX/VMS)
  - — Extensive macro capability.
  - — High-speed operation.
  - — Format conversion utilities available for popular formats.
- ANSI C-Compiler (Part No. TMDS3740815-02 for PC, Part No. TMD3704215-08 for VAX/VMS)
  - — Generates assembly code fo the TMS370 that can be easily inspected.
  - — The compilation, assembly and linking steps can all be performed with a single command.
  - — Enables the user to directly reference the TMS370's port registers by using a naming convention.
  - — Provides flexibility in specifying the storage for data objects.
  - — C-functions and Assembly functions can be easily interfaced.
- XDS/11 (eXtended Development Support) In-Circuit Emulator (Part Number TMDS3761111)
  - — PC-based, window/function-key oriented user interface for ease of use and a rapid learning environment.
  - — Symbolic debugging.
  - — Execute single/multiple instructions, single/multiple statements, until/while condition, or at full speed until breakpoint.
  - — The user needs to provide a regulated 5 V power supply with a 3A current capability.
- XDS/22 (eXtended Development Support) In-Circuit Emulator (Part Number TMDS3762210)
  - — Contains all of the features of the XDS/11 described above but does not require an external power supply.
  - — Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly.
  - — Allows break points to be qualified by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint.
  - — Provides timers fo analyzing total and average time in routines.
  - — Contains an eight line logic probe for adding visibility of external signals to the breakpoint qualifier and to the trace display.
- EEPROM/EPROM Programmer (Part Number TMDS3760510)
  - — PC-based, window/function-key oriented user interface for ease of use and a rapid learning environment.
  - — Supports all TMS370 series devices to provide rapid target prototyping capability.
  - — Also programs TMS2732, TMS2764, TMS27128, and TMS27256 NMOS and CMOS EPROMs.
  - — Plug-in personality boards and loadable parameters to support future packages and devices.
- Design Kit (Part No. TMDS3770110)
  - — Includes TMS370 Application Board and TMS370 Assembler diskette and documentation.
  - — Supports quick evaluation of TMS370 functionality.
  - — Capability to upload and download code.
  - — Capability to execute programs and software routines, and to single-step executable instructions.
  - — Software breakpoints to halt program execution at selected addresses.
  - — Wire-wrap prototype area.
  - — Reverse assembler.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 6) ..... – 0.6 to 7 V
Input voltage range, All pins except MC ..... – 0.6 to 7 V
MC ..... – 0.6 to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current per buffer, I_O (V_O = 0 to V_{CC}) (see Note 5) ..... ±10 mA
Maximum I_{CC} current ..... 170 mA
Maximum I_{SS} current ..... –170 mA
Continuous power dissipation ..... 500 mW
Storage temperature range ..... – 65°C to 150 °C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 5. Electrical characteristics are specified with all output buffers loaded with the specified I_O current. Exceeding the specified I_O current in any buffer may affect the levels on other buffers.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 6)		4.5	5	5.5	V
V_{CC}	RAM data-retention supply voltage (see Note 7)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{RESET}$	2		V_{CC}	V
		MC/Write Protect Override (WPO)	11.7		13	
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		$\overline{RESET}$	0.7 V_{CC}		V_{CC}	
T_A	Operating free-air temperature	A version	– 40		85	°C
		L version	0		70	°C

NOTES: 6. Unless otherwise noted, all voltages are with respect to V_{SS}.
7. To guarantee RAM data retention form 3 V to 4.5 V, $\overline{RESET}$ must be externally asserted and released only while V_{CC} is within the recommended operating range of 4.5 V to 5.5 V.

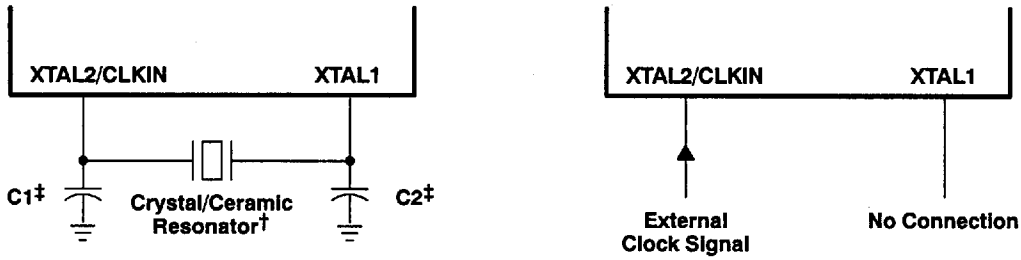
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level digital output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = – 50 µA	0.9 V_{CC}			V
			I_{OH} = – 2 mA	2.4			
I_I	Input current	MC	0 V ≤ V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	
		I/O pins	0 V ≤ V_I ≤ V_{CC}			± 10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = 0.9 V_{CC}	– 50			µA
			V_{OH} = 2.4 V	– 2			mA
I_{CC}	Supply current (Operating mode) Osc Power bit = 0 (see Note 10)		(see Notes 8 and 9) CLKIN = 20 MHz		20	36	mA
			(see Notes 8 and 9) CLKIN = 12 MHz		13	25	
			(see Notes 8 and 9) CLKIN = 2 MHz		5	11	
I_{CC}	Supply current (Standby mode) Osc Power bit = 0 (see Note 11)		(see Notes 8 and 9) CLKIN = 20 MHz		10	17	mA
			(see Notes 8 and 9) CLKIN = 12 MHz		6.5	11	
			(see Notes 8 and 9) CLKIN = 2 MHz		2	3.5	
I_{CC}	Supply current (Standby mode) Osc Power bit = 1 (see Note 12)		(see Notes 8 and 9) CLKIN = 12 MHz		4.5	8.6	mA
			(see Notes 8 and 9) CLKIN = 2 MHz		1.5	3.0	
I_{CC}	Supply current (Halt Mode)		(see Note 8) XTAL2/CLKIN < 0.2 V		1	30	µA

NOTES: 8. Single chip mode, ports configured as inputs, or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.
9. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Currents may be higher with a crystal oscillator. At 20 MHz this extra current = .01 mA × (total load capacitance + crystal capacitance in pF).
10. Maximum operating current for TMS370Cx10 = 1.4 (CLKIN) + 8 mA.
11. Maximum standby current for TMS370Cx10 = 0.75 (CLKIN) + 2 mA.
12. Maximum standby current for TMS370Cx10 = 0.56 (CLKIN) + 1.9 mA. (Osc power bit valid only from 2 MHz to 12 MHz.)

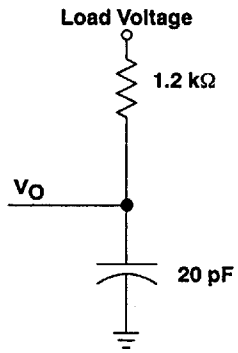
T-49-19-01

Recommended Crystal/Clock Connections



† The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
‡ The values of C1 and C2 should be the values recommended by the crystal/ceramic resonator manufacturer.

Typical Output Load Circuit§



Case 1: $V_O = V_{OH}$ = 2.4 V; Load Voltage = 0 V
Case 2: $V_O = V_{OL}$ = 0.4 V; Load Voltage = 2.1 V

§ All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	S	Slave mode
B	Byte	SIMO	SPISIMO
CI	XTAL2/CLKIN	SOMI	SPISOMI
CO	CLKOUT	SPC	SPICLK
PGM	Program		

Lowercase subscripts and their meanings are:

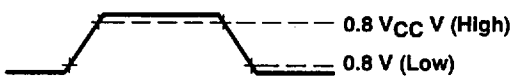
c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time	x	oscillator

The following additional letters are used with these meanings:

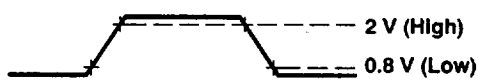
H	High
L	Low
V	Vallid

PARAMETER MEASUREMENT INFORMATION

All timings are measured between high and low measurement points as indicated in the figures below.



XTAL2/CLKIN Measurment Points



General Measurement Points

TEXAS INSTRUMENTS
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T-49-19-01

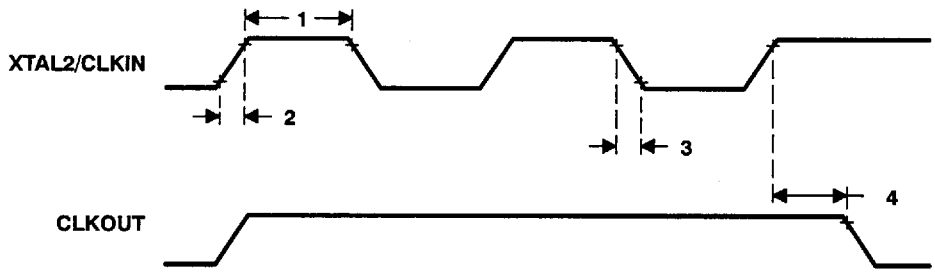
external clocking requirements†

NO.	PARAMETER		MIN	NOM	MAX	UNIT
1	$t_{w(CI)}$	XTAL2/CLKIN pulse duration (see Note 13)	20			ns
2	$t_{r(CI)}$	XTAL2/CLKIN rise time			30	ns
3	$t_{f(CI)}$	XTAL2/CLKIN fall time			30	ns
4	$t_{d(CIH-COL)}$	Delay time, XTAL2/CLKIN rise to CLKOUT fall			100	ns
	CLKIN	Crystal operating frequency	2		20	MHz

† For V_{IL} and V_{IH}, refer to "Recommended Operating Conditions".

NOTE 13: This pulse may be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

external clock timing

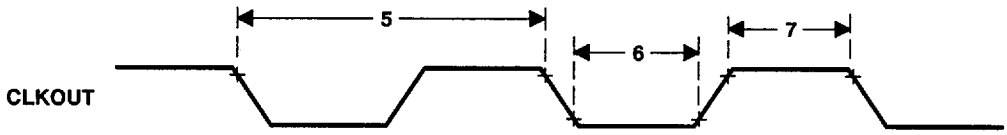


switching characteristics and timing requirements ‡

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	CLKOUT (system clock) cycle time	200	2000	ns
6	$t_{w(COL)}$	CLKOUT low pulse duration	$0.5t_c$-20	$0.5t_c$	ns
7	$t_{w(COH)}$	CLKOUT high pulse duration	$0.5t_c$	$0.5t_c$+20	ns

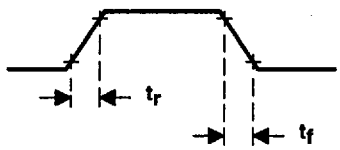
‡ t_c = system clock cycle time = 4/CLKIN.

CLKOUT timing



general purpose output signal switching time requirements

		MIN	NOM	MAX	UNIT
t_r	Rise time			45	ns
t_f	Fall time			45	ns



recommended EEPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w((PGM)B}$	Programming signal pulse duration to insure valid data is stored (byte mode)	10			ms
tw(PGM)AR	Programming signal pulse duration to insure valid data is stored (array mode)	20			ms

recommended EPROM operating conditions for programming

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.5	6.0	V
V_{PP}	Supply voltage at MC pin	12	12.5	13	V
I_{PP}	Supply current at MC pin during programming (V_{PP} = 13 V)		35	50	mA
CLKIN	Operating crystal frequency	2		20	MHz

recommended EPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w(IEPGM)}$	Initial programming pulse (see Note 14)	0.95	1	1.05	ms
$t_{w(FEPGM)}$	Final programming pulse	2.85		78.75	ms

NOTE 14: Programming pulse is active when both EXE (EPCTL.0) and VPPS (EPCTL.6) are set.

Serial Peripheral Interface (SPI) Timing

SPI master external timing characteristics†

NO.	PARAMETER		MIN	MAX	UNIT
38	$t_{C(SPC)}$	SPICLK cycle time	$2t_C$	$256t_C$	ns
39	$t_{w(SPCL)}$	SPICLK-low pulse duration	$t_C - 45$	$0.5t_{C(SPC)}+45$	ns
40	$t_{w(SPCH)}$	SPICLK-high pulse duration	$t_C - 45$	$0.5t_{C(SPC)}+45$	ns
41	$t_{d(SPCL-SIMOV)}$	Delay time, SPISIMO valid after SPICLK low (Polarity =1)	– 50	50	ns
42	$t_{v(SPCH-SIMO)}$	SPISIMO data valid after SPICLK high (Polarity =1)	$t_{w(SPCH)} - 50$		ns

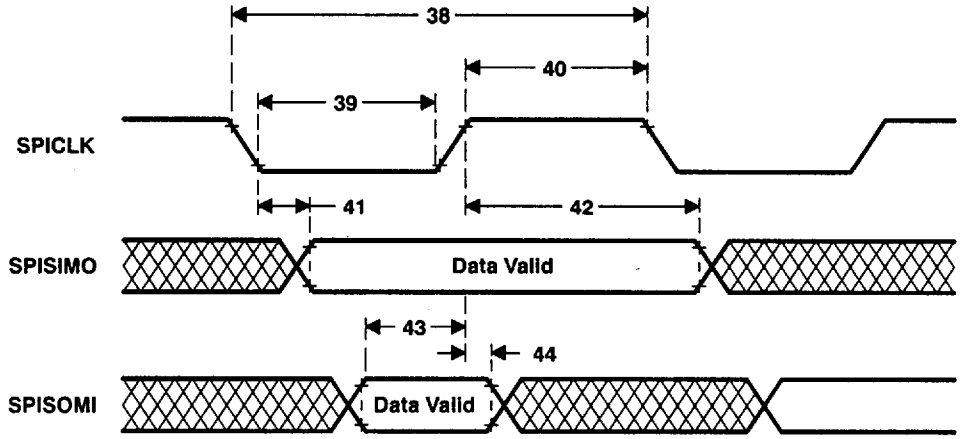
SPI master external timing requirements†

NO.			MIN	MAX	UNIT
43	$t_{su(SOMI-SPCH)}$	SPISOMI setup time to SPICLK high (Polarity = 1)	$0.25t_C + 150$		ns
44	$t_{v(SPCH-SOMI)}$	SPISOMI data valid afterSPICLK high (Polarity = 1)	0		ns

† t_C = system clock cycle time = 4/CLKIN.

T-49-19-01

SPI master external timing



NOTE 15: The diagram above is for Polarity = 1. SPICLK is inverted from above diagram when Polarity = 0.

SPI slave external timing characteristics†

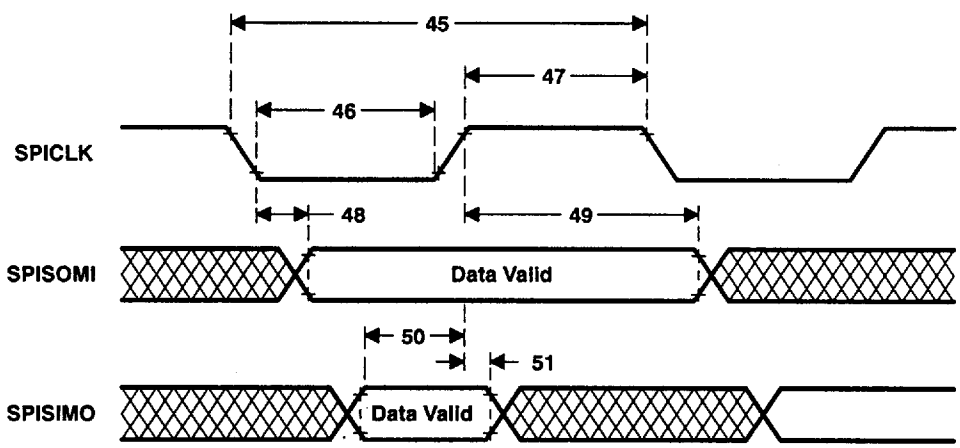
NO.	PARAMETER		MIN	MAX	UNIT
48	$t_{d(SPCL-SOMIV)S}$	Delay time, SPISOMI valid after SPICLK low (Polairty = 1)		$3.25t_c + 125$	ns
49	$t_{v(SPCH-SOMI)S}$	SPISOMI data valid after SPICLK high (Polarity =1)	$t_{w(SPCH)S}$		ns

SPI slave external timing requirements†

NO.	PARAMETER		MIN	MAX	UNIT
45	$t_{c(SPC)S}$	SPICLK cycle time	$8t_c$		ns
46	$t_{w(SPCL)S}$	SPICLK-low pulse duration	$4t_c - 45$	$0.5t_{c(SPC)S+45}$	ns
47	$t_{w(SPCH)S}$	SPICLK high pulse duration	$4t_c - 45$	$0.5t_{c(SPC)S+45}$	ns
50	$t_{su(SIMO-SPCH)S}$	SPISIMO setup time to SPICLK high (Polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)S}$	SPISIMO data valid after SPICLK high (Polarity = 1)	$3t_c + 100$		ns

† t_c = system clock cycle time = 4/CLKIN.

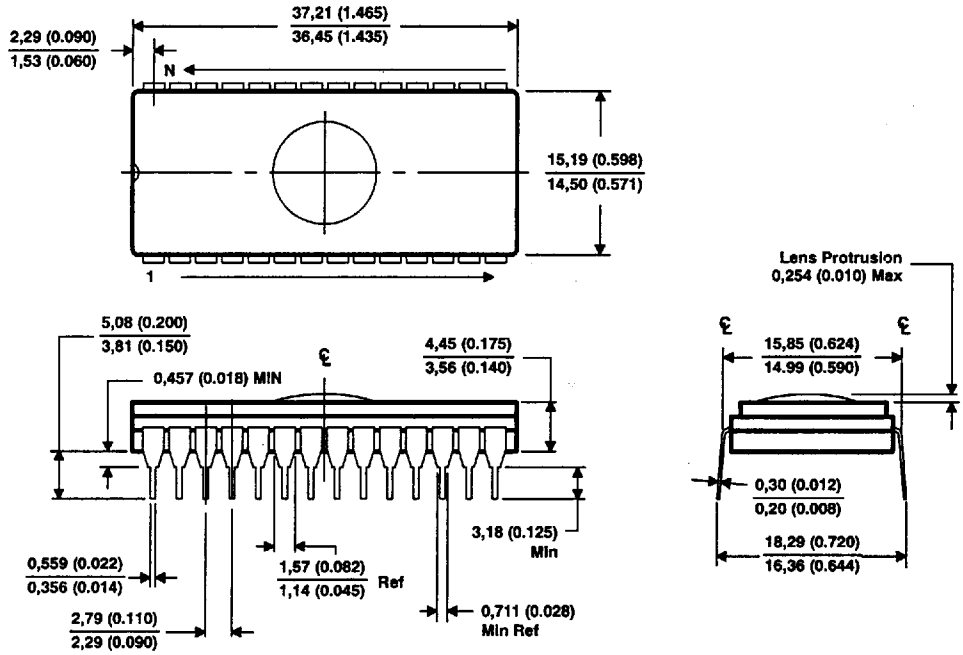
SPI slave external timing



NOTES: 16. The diagram above is for Polarity =1. SPICLK is inverted from above diagram when Polarity = 0.
17. As a slave, the SPICLK pin is used as the input for the serial clock, which is supplied from the network master.

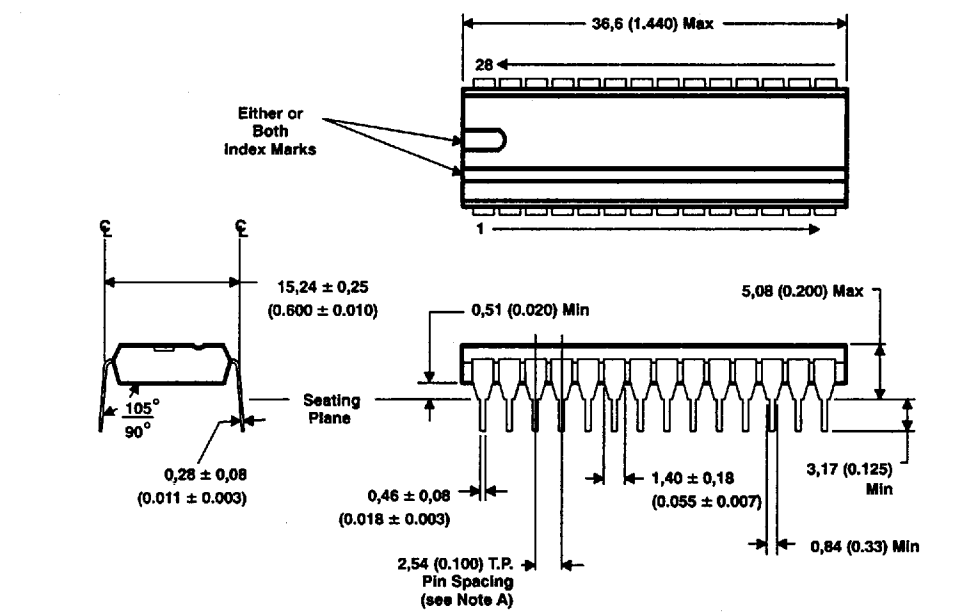
MECHANICAL DATA

28-pin ceramic leaded chip carrier package (J suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHICALLY IN INCHES

28-pin plastic leaded chip carrier package (N suffix)



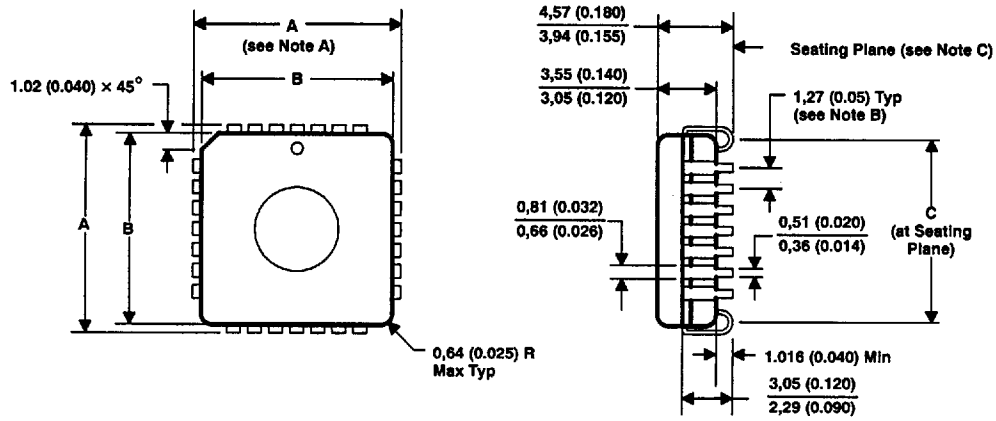
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHICALLY IN INCHES

NOTE A: Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.

T-49-19-01

MECHANICAL DATA

FZ cerquad chip carrier package

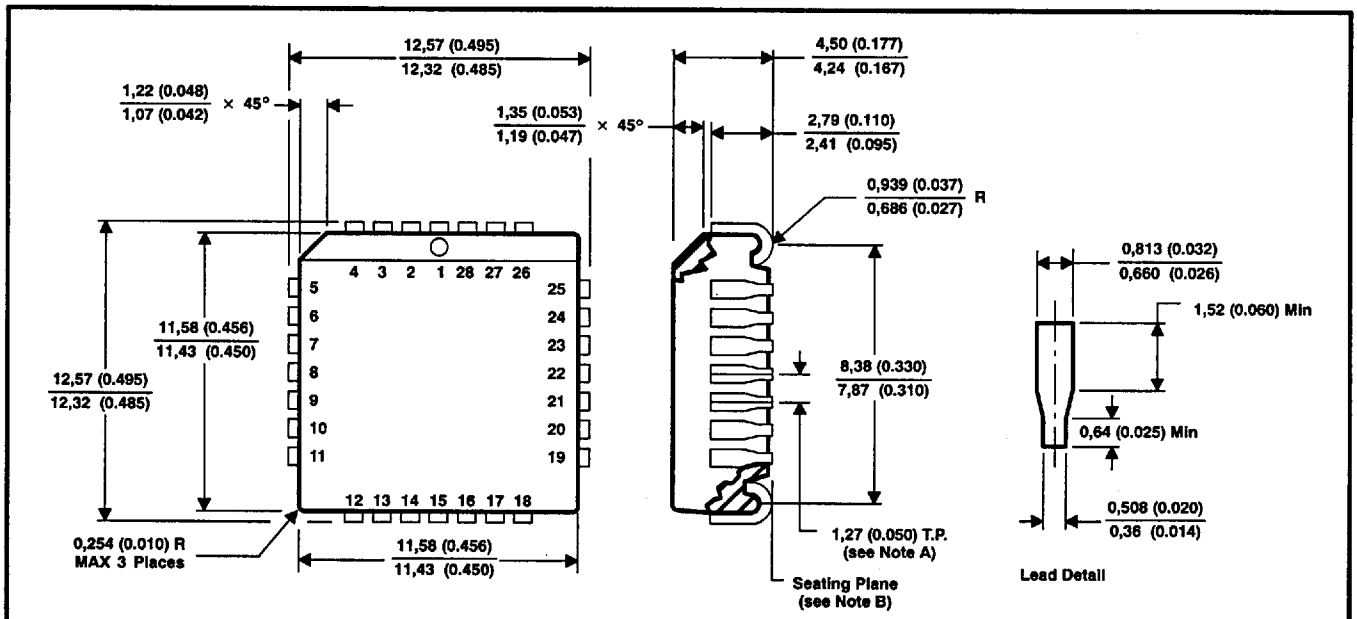


		A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
M0-087AA	28	12,32 (0.485)	12,57 (0.495)	10,92 (0.430)	11,56 (0.455)	10,41 (0.410)	10.92 (0.430)
M0-087AB	44	17,40 (0.685)	17,65 (0.695)	16,00 (0.630)	16,64 (0.655)	15,49 (0.610)	16,00 (0.630)
—	68	25,02 (0.985)	25,27 (0.995)	23,62 (0.930)	24,26 (0.955)	23.11 (0.910)	23,62 (0.930)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHICALLY IN INCHES

NOTES: A. Center line of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar with 0,15 (0.006).

28-pin plastic leaded chip carrier package (FN suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHICALLY IN INCHES

NOTES: A. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
B. The lead contact points are planar within 0,101(0.004).