**MOS**
**LSI**

- 4096 x 1 Organization
- 3 Performance Ranges:

| | ACCESS TIME (MAX) | READ OR WRITE CYCLE (MIN) | READ, MODIFY WRITE CYCLE (MIN) |
|---|---|---|---|
| TMS 4060 | 300 ns | 470 ns | 710 ns |
| TMS 4060-1 | 250 ns | 430 ns | 640 ns |
| TMS 4060-2 | 200 ns | 400 ns | 580 ns |

- **Full TTL Compatibility on All Inputs Except CE (No Pull-Up Resistors Needed)**
- **Low Power Dissipation**
  - — 400 mW Operating (Typical)
  - — 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-in-Line Package

**22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)**

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | $V_{BB}$ | | 22 | $V_{SS}$ |
| 2 | A9 | | 21 | A8 |
| 3 | A10 | | 20 | A7 |
| 4 | A11 | | 19 | A6 |
| 5 | $\overline{CS}$ | | 18 | $V_{DD}$ |
| 6 | DI | | 17 | CE |
| 7 | $\overline{DO}$ | | 16 | N/C |
| 8 | A0 | | 15 | A5 |
| 9 | A1 | | 14 | A4 |
| 10 | A2 | | 13 | A3 |
| 11 | $V_{CC}$ | | 12 | R/$\overline{W}$ |

**description**

The TMS 4060 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4060, 250 ns access for the TMS 4060-1, and 200 ns for the TMS 4060-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. When driven by a Series 74 device, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible buffer is guaranteed to drive two Series 74 TTL gates. The TMS 4060 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of these RAM's is 400 mW active and 0.2 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4060 series is offered in both 22-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting hole rows on 0.400-mil centers.
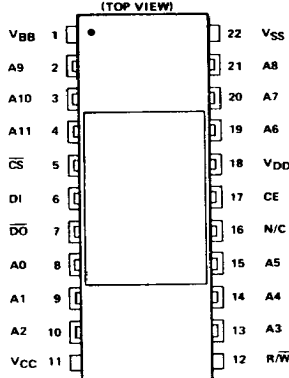
**operation**

**chip select ($\overline{CS}$)**

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the data-in, data-out and read/write inputs. The data input and data output terminals are enabled when chip select is low. Therefore, the read, write, and read-modify-write operations are performed only when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip select must be held high as long as chip enable is high. A register for the chip-select input is provided on the chip to reduce overhead and simplify system design.

**chip enable (CE)**

A single external clock input is required. All read, write, and read-modify-write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode. No read or write operations can take place because the chip is automatically precharging.

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## peration (continued)

### mode select (R/W̄)

The read or write mode is selected through the read/write (R/W̄) input. A logic high on the R/W̄ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected.

### address (A0—A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

### data-in (DI)

Data is written during a write or read-modify-write cycle while the chip enable is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. There is no register on the data-in terminal.

### data-out (D̄Ō)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates. The output is in the high-impedance (floating) state when the chip enable is low. It remains in the high-impedance state if the chip-select input is high when chip enable goes high and provided that chip select remains high as long as chip enable is high. If the chip select is set up low prior to the rise of chip enable and held low an interval after that rise, the output will be enabled as long as chip enable stays high regardless of subsequent changes in the level of chip select. A data-valid mode is always preceded by a low output state. Data-out is inverted from data-in.

### refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs, A0 through A5 (pins 8, 9, 10, 13, 14, 15), or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row. The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, then chip select must be high. The column addresses (A6 through A11) can be indeterminate during refresh.

### functional block diagram
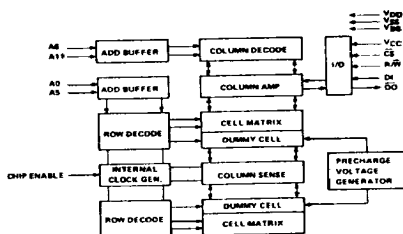


### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note) | −0.3 to 20 V |
| Supply voltage, $V_{CC}$, $V_{DD}$ relative to $V_{SS}$ | −1 to 15 V |
| Supply voltage, $V_{DD}$ (see Note) | −0.3 to 20 V |
| Supply voltage, $V_{SS}$ (see Note) | −0.3 to 20 V |
| All input voltages (see Note) | −0.3 to 20 V |
| Chip-enable voltage (see Note) | −2 to 7 V |
| Output voltage (operating, with respect to $V_{SS}$) | 0°C to 70°C |
| Operating free-air temperature range | −55°C to 150°C |
| Storage temperature range | |

NOTE: Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, $V_{BB}$ (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to $V_{SS}$.

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# TMS 4060 JL, NL
## 4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

### recommended operating conditions (see Note)

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Supply voltage, $V_{DD}$ | 11.4 | 12 | 12.6 | V |
| Supply voltage, $V_{SS}$ | | 0 | | V |
| Supply voltage, $V_{BB}$ | −4.5 | −5 | −5.5 | V |
| High-level input voltage, $V_{IH}$ (all inputs except chip enable) | 2.2 | | 5.25 | V |
| High-level chip enable input voltage, $V_{IH(CE)}$ | $V_{DD}$ −0.6 | | $V_{DD}$ +1.0 | V |
| Low-level input voltage, $V_{IL}$ (all inputs except chip enable) (see Note) | −0.6 | | 0.6 | V |
| Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note) | −1 | | 0.6 | V |
| Refresh time, $t_{refresh}$ | | | 2 | ms |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

NOTE: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

### electrical characteristics over full range of recommended operating conditions, $T_A$ = 0°C to 70°C (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP[†] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_O$ = −2 mA | | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | $I_O$ = 3.2 mA | | $V_{SS}$ | | 0.4 | V |
| $I_I$ | Input current (all inputs except chip enable) | $V_I$ = 0 to 5.25 V | | | | 10 | µA |
| $I_{I(CE)}$ | Chip enable input current | $V_I$ = 0 to 13.2 V | | | | 2 | µA |
| $I_{OZ}$ | High-impedance-state (off-state) output current | $V_O$ = 0 to 5.25 V | | | | 10 | µA |
| $I_{CC}$ | Supply current from $V_{CC}$ | 2 Series 74 TTL loads | | | | 1 | mA |
| $I_{DD}$ | Supply current from $V_{DD}$ | $V_{IH(CE)}$ = 12.6 V | | | 30 | 60 | mA |
| $I_{DD}$ | Supply current from $V_{DD}$, standby | $V_{IL(CE)}$ = 0.6 V (after 1 memory cycle)(See Note 2) | | | 20 | | µA |
| $I_{DD(av)}$ | Average supply current from $V_{DD}$ during read or write cycle | Minimum cycle time | TMS 4060 | | 32 | | mA |
| | | | TMS 4060-1 | | 35 | | |
| | | | TMS 4060-2 | | 38 | | |
| | | | TMS 4060-3 | | 42 | | |
| $I_{DD(av)}$ | Average supply current from $V_{DD}$ during read, modify write cycle | | TMS 4060 | | 32 | | mA |
| | | | TMS 4060-1 | | 35 | | |
| | | | TMS 4060-2 | | 38 | | |
| | | | TMS 4060-3 | | 42 | | |
| $I_{BB}$ | Supply current from $V_{BB}$ | $V_{BB}$ = −5.5 V, $V_{CC}$ = 5.25 V, $V_{DD}$ = 12.6 V, $V_{SS}$ = 0 V | | | −5 | −100 | µA |

[†] All typical values are at $T_A$ = 25°C.
NOTE 2: Chip enable must be cycled before $I_{DD}$ standby measurement is made.

### capacitance at $V_{DD}$ = 12 V, $V_{SS}$ = 0 V, $V_{BB}$ = −5 V, $V_{CC}$ = 5 V, $V_{I(CE)}$ = 0 V, $V_I$ = 0 V, f = 1 MHz[‡], $T_A$ = 0°C to 70°C (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP[†] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{i(ad)}$ | Input capacitance address inputs | | | 5 | 7 | pF |
| $C_{i(CE)}$ | Input capacitance clock input | $V_{I(CE)}$ = 10.8 V | | 18 | 22 | pF |
| | | $V_{I(CE)}$ = 0 V | | 23 | 27 | |
| $C_{i(\overline{CS})}$ | Input capacitance chip select input | | | 4 | 6 | pF |
| $C_{i(data)}$ | Input capacitance data input | | | 4 | 6 | pF |
| $C_{i(R/\overline{W})}$ | Input capacitance read/write input | | | 5 | 7 | pF |
| $C_O$ | Output capacitance | | | 5 | 7 | pF |

[†] All typical values are at $T_A$ = 25°C.
[‡] AC characteristics guaranteed only for cumulative chip enable duty cycle less than 65% over each 2 millisecond period.

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read cycle timing requirements over recommended supply voltage range, $T_A = 0°C$ to $70°C$

| PARAMETER | | TMS 4060 | | TMS 4060-1 | | TMS 4060-2 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{c(rd)}$ | Read cycle time | 470 | | 430 | | 400 | | ns. |
| $t_{w(CEH)}$ | Pulse width, chip enable high | 300 | 4000 | 260 | 4000 | 230 | 4000 | ns |
| $t_{w(CEL)}$ | Pulse width, chip enable low | 130 | | 130 | | 130 | | ns |
| $t_{r(CE)}$ | Chip-enable rise time | | 40 | | 40 | | 40 | ns |
| $t_{f(CE)}$ | Chip-enable fall time | | 40 | | 40 | | 40 | ns |
| $t_{su(ad)}$ | Address setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{su(CS)}$ | Chip-select setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{su(rd)}$ | Read setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{h(ad)}$ | Address hold time | 150↑ | | 150↑ | | 150↑ | | ns |
| $t_{h(CS)}$ | Chip-select hold time | 150↑ | | 150↑ | | 150↑ | | ns |
| $t_{h(rd)}$ | Read hold time | 40↓ | | 40↓ | | 40↓ | | ns |

*.The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

read cycle switching characteristics over recommended supply voltage range, $T_A = 0°C$ to $70°C$

| PARAMETER | | TMS 4060 | | TMS 4060-1 | | TMS 4060-2 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{a(CE)}$ | Access time from chip enable† | | 280 | | 230 | | 180 | ns |
| $t_{a(ad)}$ | Access time from address† | | 300 | | 250 | | 200 | ns |
| $t_{PHZ}$ or $t_{PLZ}$ | Output disable time from high or low level‡ | | 30 | | 30 | | 30 | ns |
| $t_{PZL}$ | Output enable time to low level‡ | | 250 | | 200 | | 150 | ns |

†Test conditions: $C_L = 50$ pF, $t_{r(CE)} = 20$ ns, Load = 1 Series 74 TTL gate.
‡Test conditions: $C_L = 50$ pF, Load = 1 Series 74 TTL gate.

write cycle timing requirements over recommended supply voltage range, $T_A = 0°C$ to $70°C$

| PARAMETER | | TMS 4060 | | TMS 4060-1 | | TMS 4060-2 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{c(wr)}$ | Write cycle time | 470 | | 430 | | 400 | | ns |
| $t_{w(CEH)}$ | Pulse width, chip enable high | 300 | 4000 | 260 | 4000 | 230 | 4000 | ns |
| $t_{w(CEL)}$ | Pulse width, chip enable low | 130 | | 130 | | 130 | | ns |
| $t_{w(wr)}$ | Write pulse width | 200 | | 190 | | 180 | | ns |
| $t_{r(CE)}$ | Chip-enable rise time | | 40 | | 40 | | 40 | ns |
| $t_{f(CE)}$ | Chip-enable fall time | | 40 | | 40 | | 40 | ns |
| $t_{su(ad)}$ | Address setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{su(CS)}$ | Chip-select setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{su(da-wr)}$ | Data-to-write setup time§ | 0 | | 0 | | 0 | | ns |
| $t_{su(wr)}$ | Write-pulse setup time | 240↑ | | 220↑ | | 210↑ | | ns |
| $t_{h(ad)}$ | Address hold time | 150↑ | | 150↑ | | 150↑ | | ns |
| $t_{h(CS)}$ | Chip-select hold time | 150↑ | | 150↑ | | 150↑ | | ns |
| $t_{h(da)}$ | Data hold time | 40↓ | | 40↓ | | 40↓ | | ns |

*.The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
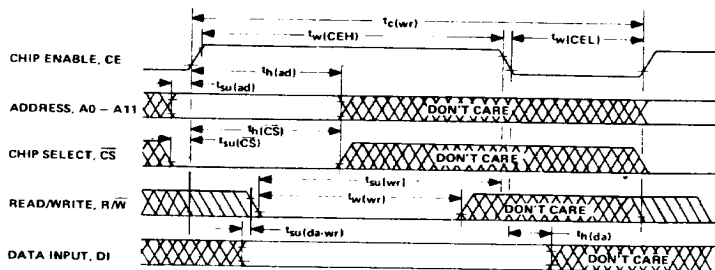§If R/W is low before CE goes high, then DI must be valid when CE goes high.

## TMS 4060 JL, NL
## 4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

read cycle timing
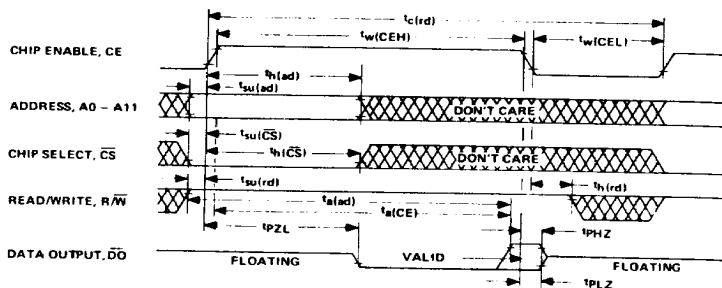


NOTE: For the chip enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). During the time from the rise of CE to the fall of R/W, R/W is pe mitted to change from high to low only. AC characteristics guaranteed only for cumulative CE duty cycle less than 65% over each 2 n period.

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**read-modify-write cycle timing requirements over recommended supply voltage range, $T_A = 0°C$ to $70°C$**

| PARAMETER | | TMS 4060 | | TMS 4060-1 | | TMS 4060-2 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{c(RMW)}$ | Read-modify-write cycle time* | 710 | | 640 | | 580 | | ns |
| $t_{w(CEH)}$ | Pulse width, chip enable high* | 540 | 4000 | 470 | 4000 | 410 | 4000 | ns |
| $t_{w(CEL)}$ | Pulse width, chip enable low | 130 | | 130 | | 130 | | ns |
| $t_{w(wr)}$ | Write pulse width | 200 | | 190 | | 180 | | ns |
| $t_{r(CE)}$ | Chip-enable rise time | | 40 | | 40 | | 40 | ns |
| $t_{f(CE)}$ | Chip-enable fall time | | 40 | | 40 | | 40 | ns |
| $t_{su(ad)}$ | Address setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{su(CS)}$ | Chip-select setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{su(da-wr)}$ | Data-to-write setup time | 0 | | 0 | | 0 | | ns |
| $t_{su(rd)}$ | Read pulse setup time | 0↑ | | 0↑ | | 0↑ | | ns |
| $t_{su(wr)}$ | Write pulse setup time | 240↓ | | 220↓ | | 210↓ | | ns |
| $t_{h(ad)}$ | Address hold time | 150↑ | | 150↑ | | 150↑ | | ns |
| $t_{h(CS)}$ | Chip-select hold time | 150↑ | | 150↑ | | 150↑ | | ns |
| $t_{h(rd)}$ | Read hold time | 280↑ | | 230↑ | | 180↑ | | ns |
| $t_{h(da)}$ | Data hold time | 40↓ | | 40↓ | | 40↓ | | ns |

*↑The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*Test conditions: $t_{f(rd)} = 20$ ns.

**read-modify-write cycle switching characteristics over recommended supply voltage range, $T_A = 0°C$ to 70 $T_A = 0°C$ to $70°C$**

| PARAMETER | | TMS 4060 | | TMS 4060-1 | | TMS 4060-2 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{a(CE)}$ | Access time from chip enable† | | 280 | | 230 | | 180 | ns |
| $t_{a(ad)}$ | Access time from address† | | 300 | | 250 | | 200 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high level output from write pulse‡ | 30 | | 30 | | 30 | | ns |
| $t_{PHZ}$ | Output disable time from high level‡ | 30 | | 30 | | 30 | | ns |
| $t_{PZL}$ | Output enable time to low level‡ | | 250 | | 200 | | 150 | ns |

†Test conditions: $C_L = 50$ pF, $t_{r(CE)} = 20$ ns, Load = 1 Series 74 TTL gate.
‡Test conditions: $C_L = 50$ pF, Load = 1 Series 74 TTL gate.

**read-modify-write cycle timing**
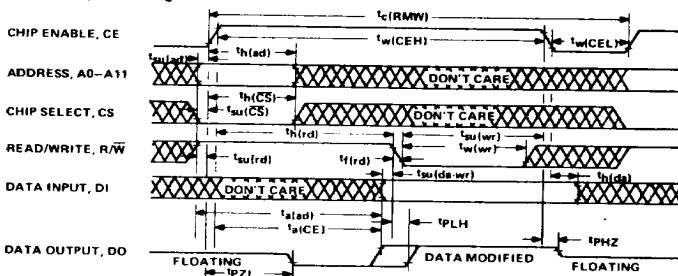


NOTE: For the chip enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). AC characteristics guaranteed only for cumulative CE duty cycle less than 65% over each 2 ms period.
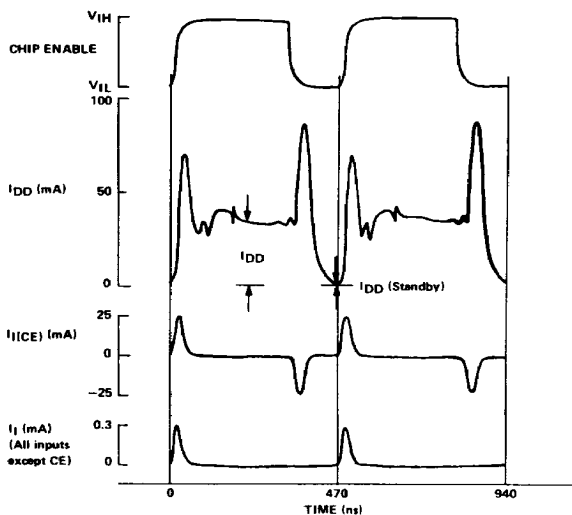
## TMS 4060 JL, NL
## 4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

**timing diagram conventions**

| TIMING DIAGRAM SYMBOL | MEANING | |
|---|---|---|
| | INPUT FORCING FUNCTIONS | OUTPUT RESPONSE FUNCTIONS |
| ‾‾‾‾‾ | Must be steady high or low | Will be steady high or low |
| ╲╲╲╲ | High-to-low changes permitted | Will be changing from high to low sometime during designated interval |
| ╱╱╱╱ | Low-to-high changes permitted | Will be changing from low to high sometime during designated interval |
| ✕✕✕✕✕ | Don't care | State unknown or changing |
| ⟩⟩⟩⟨⟨⟨ | (Does not apply) | Center line is high-impedance off-state |

### TYPICAL WAVEFORMS

**ACCESS TIMES vs TEMPERATURE**

TMS 4060 MAX
TMS 4060-1 MAX
TMS 4060-2 MAX
TYPICAL TMS 4060
TYPICAL TMS 4060-1
TYPICAL TMS 4060-2
TYPICAL SLOPE = 0.75 ns/°C
$C_L$ = 50 pF
$t_{a(ad)}$ – Access Time – ns
$T_A$ – Free-Air Temperature – °C
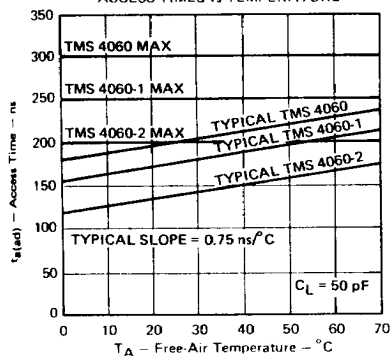
**ACCESS TIMES vs LOAD CAPACITANCE**

TMS 4060 MAX
TMS 4060-1 MAX
TMS 4060-2 MAX
TYPICAL TMS 4060
TYPICAL TMS 4060-1
TYPICAL TMS 4060-2
TYPICAL SLOPE = 0.25 ns/pF
$T_A$ = 25°C
$t_{a(ad)}$ – Access Time – ns
$C_L$ – Load Capacitance – pF
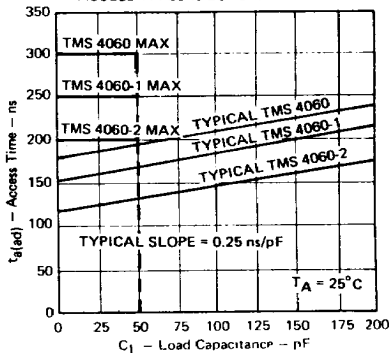
**REFRESH TIME vs TEMPERATURE**

TYPICAL REQUIRED
MAXIMUM RECOMMENDED
$t_{c(rfsh)}$ – Refresh Time – ms
$T_A$ – Free-Air Temperature – °C
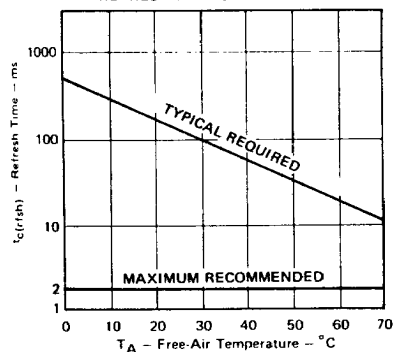
**AVERAGE CURRENT vs TEMPERATURE**

TYPICAL TMS 4060-2
TYPICAL TMS 4060-1
TYPICAL TMS 4060
CURRENT MEASURED AT MINIMUM CYCLE TIMES
$I_{DD(av)}$ – Supply Current – mA
$T_A$ – Free-Air Temperature – °C