TMS 4050 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

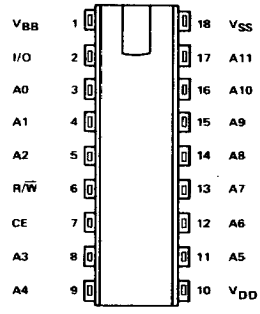
BULLETIN NO. DL-S 7512242, FEBRUARY 1975—REVISED OCTOBER 1977

- 4096 x 1 Organization
- 18-Pin 300-Mil Package Configuration
- Multiplexed Data Input/Output
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4050	300 ns	470 ns	730 ns
TMS 4050-1	250 ns	430 ns	660 ns
TMS 4050-2	200 ns	400 ns	600 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Single Low-Capacitance Clock
- Low-Power Dissipation
  - 420 mW Operating (Typical)
  - 0.1 mW Standby (Typical)
- N-Channel Silicon-Gate Technology

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



description

The TMS 4050 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4050, 250 ns access for the TMS 4050-1, and 200 ns for TMS 4050-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The input buffers allow a minimum 200 mV noise margin when driven by a series 74 TTL device. The TTL-compatible open-drain buffer is guaranteed to drive 1 series 74 TTL gate. The low capacitance of the address and control inputs precludes the need for specialized drivers. The TMS 4050 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12 line address is available, which minimizes external control logic and optimizes system performance.

The typical power dissipation of these RAM's is 420 mW active and 0.1 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4050 series is offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting hole rows on 300-mil centers.

operation

chip enable (CE)

A single external clock input is required. All read, write, and read-modify-write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode and is not selected. No read/write operations can take place during the standby mode because the chip is disabled and is automatically precharging.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

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operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected and the data output is disabled when the write mode is selected.

address (A0—A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data input/output (I/O)

Data input and output are multiplexed on a common input/output terminal, which is controlled by the R/$\overline{W}$ input. Data is written during a write or read-modify-write cycle while the chip enable is high. The I/O terminal requires connection to an external pull-up resistor since the output buffer has an open-drain configuration. The open-drain output buffer provides direct TTL sink compatibility with a fan-out of one Series 74 TTL gate. A low logic level results from conduction in the open-drain output buffer while a high level occurs with the buffer in its high-impedance state. Data written into the memory is read out in its true form.

refresh

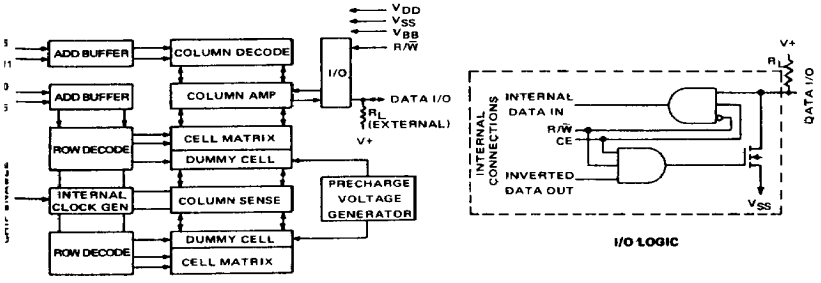
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses (A0 through A5) every 2 milliseconds or less. Addressing any row refreshes all 64 bits in that row. The column addresses (A6 through A11) can be indeterminate during refresh.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{DD} relative to V_{SS}	−0.1 to 15 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Chip-enable voltage (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

functional block diagram



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note 2)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note 2)	−1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate		2.4			V
V_{OL}	Low-level output voltage			V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V		5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = 0 to 5.5 V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = 0 to 13.2 V				10	μA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 13.2 V	TMS4050		35	60	mA
			TMS4050-1				
			TMS4050-2		35	70	
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V (See Note 3)			20		μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing	TMS 4050		32		mA
			TMS 4050-1		35		
			TMS 4050-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4050		32		mA
			TMS 4050-1		35		
			TMS 4050-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V, V_{SS} = 0 V			5	100	μA

†All typical values are at T_A = 25°C.
NOTE 3: Chip enable must be cycled before I_{DD} standby measurement is made.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz‡, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 12 V		24	28	pF
		$V_{I(CE)}$ = 0 V		29	33	
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
$C_{i(I/O)}$	I/O terminal capacitance			7	9	pF

†All typical values are at T_A = 25°C.
‡AC characteristics guaranteed only for cumulative chip enable duty cycle less than 65% over each 2 millisecond period.

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read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access time from addresses†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from chip enable*	40		40		40		ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate, $t_{r(CE)}$ = 20 ns.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

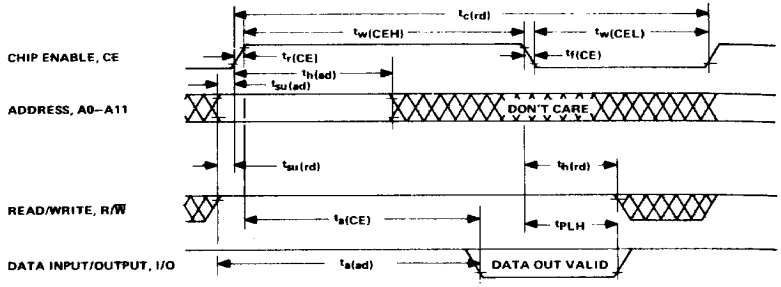
PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(da-wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{d(CEH-wr)}$	Chip-enable-high-to-write delay time†		40↑		40↑		40↑	ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

*If R/$\overline{W}$ is low before CE goes high, then I/O (data in) must be valid when CE goes high.

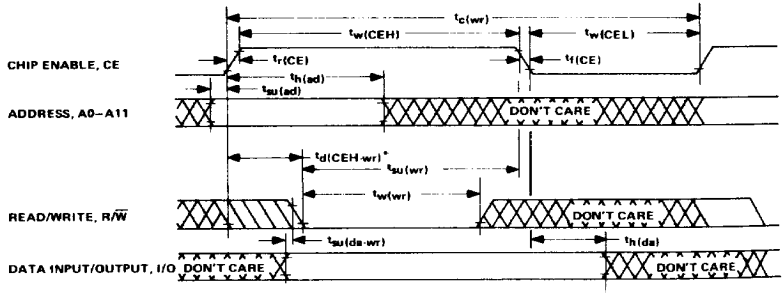
†The write pulse must go low at least $t_{su(wr)}$ minimum before CE goes low. If R/$\overline{W}$ remains high more than $t_{d(CEH-wr)}$ maximum (40 ns) after CE goes high, the data in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices (see comments on Region 1 under read, modify write timing diagram).

read or refresh cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
*The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(CEH-wr)}$ maximum (40 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices. During $t_{d(CEH-wr)}$, R/$\overline{W}$ is permitted to change from high to low only.

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read-modify-write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

	PARAMETER	TMS 4050 MIN	TMS 4050 MAX	TMS 4050-1 MIN	TMS 4050-1 MAX	TMS 4050-2 MIN	TMS 4050-2 MAX	UNIT
$t_{c(RMW)}$	Read-modify-write cycle time†	730		660		600		ns
$t_{w(CEH)}$	Pulse width, chip enable high†	560	4000	490	4000	430	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{d(wr-deL)}$	Write to data-in-low delay time		20		20		20	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(deH)}$	Data-in-high setup time	240↓		220↓		210↓		ns
$t_{su(rd)}$	Read-pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	300↑		250↑		200↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

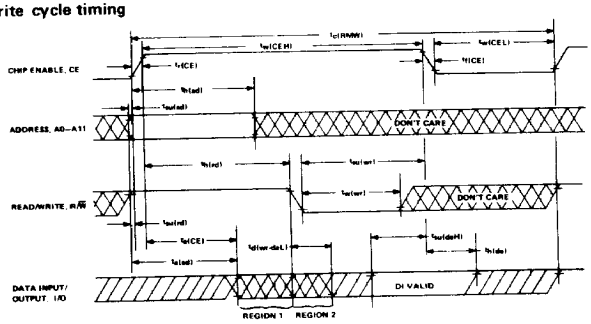
†↓ The arrow indicates the edge of the chip-enable pulse for reference: ↑ for the rising edge; ↓ for the falling edge.
‡Test conditions: $t_{f(rd)}$ = 20 ns.

read-modify-write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

	PARAMETER	TMS 4050 MIN	TMS 4050 MAX	TMS 4050-1 MIN	TMS 4050-1 MAX	TMS 4050-2 MIN	TMS 4050-2 MAX	UNIT
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access Time from addresses†		300		250		200	ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate. $t_{r(CE)}$ = 20 ns.

read-modify-write cycle timing



REGION 1 – In region 1 data-out is valid until the I/O terminal is forced high or low by the data-in driver. A transition from low to high is permissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty.

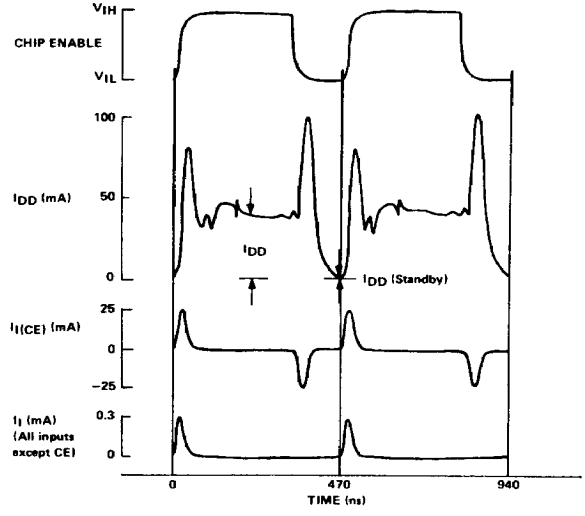
REGION 2 – In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be valid by the end of region 2.

NOTE: For the chip enable input high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(CE)}$ and $t_{f(CE)}$ are equal to 20 ns.

timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING	
	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

TYPICAL WAVEFORMS



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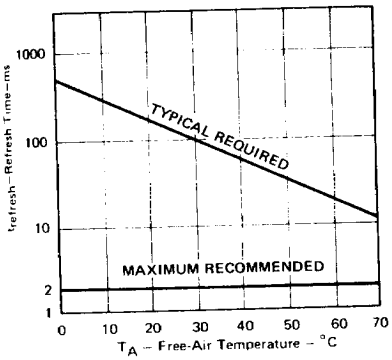
REFRESH TIME vs TEMPERATURE



ACCESS TIMES vs TEMPERATURE