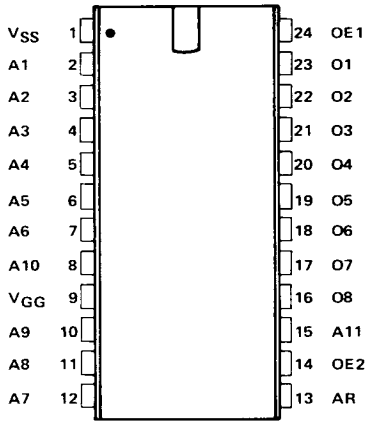
TMS 4800 JL, NL
16384-BIT READ-ONLY MEMORY

BULLETIN NO. DL-S 7512260, MAY 1975

- 2048 x 8 or 4096 x 4 Organization
- Total TTL-Compatibility
- Maximum Access Time . . . 700 ns
- Minimum Cycle Time . . . 1000 ns
- Typical Power Dissipation . . . 450 mW
- Open-Drain Output for Wire-OR Configurations
- 24-Pin 600-Mil Dual-in-Line Packages
- Two Chip-Enable Controls

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4800 JL, NL is a 16384-bit read-only memory, organized as either 2048 words of 8-bits or 4096 words of 4-bits. All inputs are TTL-compatible. The eight open-drain outputs must be connected by pull-down resistors to an external negative supply to drive standard TTL circuits. Two output-enable terminals allow each 2048 x 4-bit array to be read independently as 4-bit words or simultaneously as 8-bit words.

Two devices can be OR-tied, with proper choice of programming on the output-enable terminals to be specified by the customer. Addresses may change up to 50 ns after the clock cycle begins. This allows TTL address-decoding circuits to synchronize on the rise of the clock and stabilize during this interval effectively shortening the device read-access time. The TMS 4800 is designed with P-channel enhancement-type technology for high-density, fixed-memory applications such as logic function generation and microprogramming. This ROM is supplied in a ceramic (JL suffix) or plastic (NL suffix) 24-pin package designed for insertion in mounting-hole rows on 600-mil centers.

operation

address read (AR)

Address read constitutes the master timing signal of the device. After AR goes high, address and output enable inputs latch. The address-read clock is high during the address-valid and output-enable-valid intervals. Data out is valid both before and after AR goes low, since enabled outputs latch during the cycle.

address (A1-A11)

Any of the 2048-word addresses are selected by an 11-bit positive-logic binary word, A1 being the least-significant bit progressing through to A11, which is the most-significant bit. Address inputs can change up to 50 ns after the AR clock goes high and must remain valid 250 ns after AR goes high. This input latching feature allows the user to change address while data is being read. These system advantages result from latching of the internal address register during a short address-valid interval.

output enable (OE1 and OE2)

The ROM consists of two side-by-side 2048-word-by-4-bit arrays. OE1 enables output terminals O1 through O4 and OE2 outputs O5 through O8 with the two arrays being enabled independently. The user may choose any of four combinations by enabling with either a low or high level on OE1 or OE2. To read 8-bit words with a single address, both OE1 and OE2 must be enabled. For 8-bit readout, two devices may be OR-tied to increase the effective size of the ROM system by programming complementary enable levels on corresponding device terminals.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

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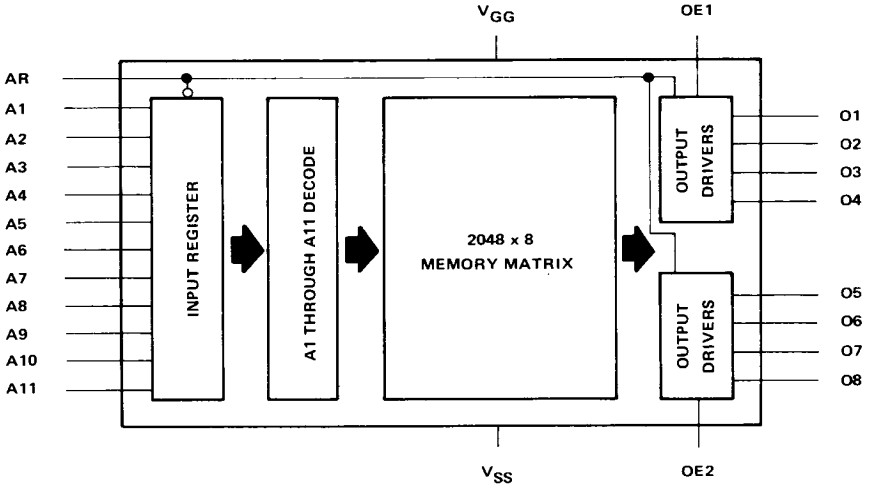
operation (continued)

Output terminals on a single device are OR-tied for a 4096-word x 4-bit organization as follows: O1 to O5; O2 to O6; O3 to O7; and O4 to O8. Since the OE1 and OE2 inputs latch internally, the enable signals may change before or during the output data-valid interval. For additional information on OR-ties, see the section on Expanded Memory Configurations.

data out (O1-O8)

Outputs O1 through O4 are enabled by OE1 with outputs O5 through O8 enabled by OE2. Output transistors are open-drain and compatible with TTL circuits when connected to an external negative supply through a pull-down resistor. All outputs go low immediately after the rise of AR. A disabled output rises to a high level after a propagation delay following the fall of the AR clock if a high logic level was stored. If devices are OR-tied, an enabled output should be read before AR goes low in order to distinguish a stored high from a high coming from the OR-tied disabled output. Because the outputs latch, data on an enabled output remains valid until the next rise of the AR clock.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1)	−20 to 0.3 V
All input voltages (see Note 1)	−20 to 0.3 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	4.75	5	5.25	V
Supply voltage, V_{GG}	−11	−12	−13	V
High-level input voltage, V_{IH} (all inputs)	V_{SS} −1.5		V_{SS}	V
Low-level input voltage, V_{IL} (all inputs) (see Note 2)	−4		0.6	V
Read cycle time, $t_{c(rd)}$	1000			ns
Pulse width, address read high, $t_{w(ARH)}$	500		100000	ns
Pulse width, address read low, $t_{w(ARL)}$	450			ns
Address-read rise time, $t_{r(AR)}$			40	ns
Address-read fall time, $t_{f(AR)}$			40	ns
Address-read-high-to-address delay time, $t_{d(ARH\text{-}ad)}$			50	ns
Address-read-high-to-output-enable delay time, $t_{d(ARH\text{-}OE)}$			50	ns
Address hold time, $t_{h(ad)}$	250			ns
Output-enable hold time, $t_{h(OE)}$	250			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 2. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2.4 mA	2.5			V
I_{OL}	Low-level output current	V_{OL} = 0.4 V			50	μA
I_I	Input current (all inputs)	$V_I = V_{SS}$			1	μA
I_{SS}	Supply current from V_{SS}			29	40	mA
I_{GG}	Supply current from V_{GG}			−29	−40	mA

‡All typical values are at T_A = 25°C.

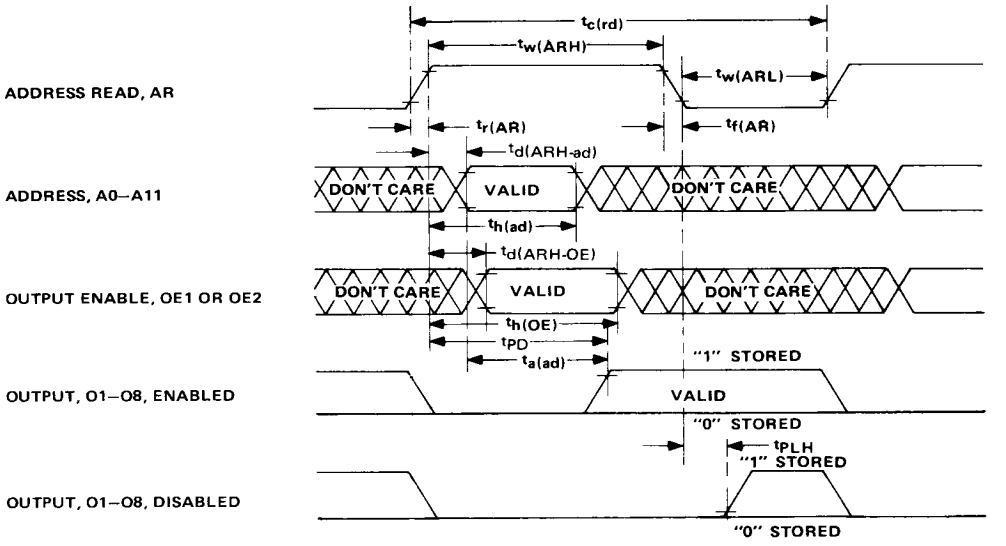
switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		550	700	ns
t_{PLH}	Propagation delay time, low-to-high level output from address read (output disabled)	200			ns
t_{PD}	Propagation delay time from address read to data valid		600	750	ns

‡Typical values are measured at V_{SS} = 5 V, V_{GG} = −12 V, and T_A = 25°C.

NOTES: 3. Enabled outputs remain valid until next AR pulse. Disabled outputs may be considered valid until 200 ns after the high-to-low transition of AR.
4. All rise and fall times are ≤20 ns.

voltage waveforms



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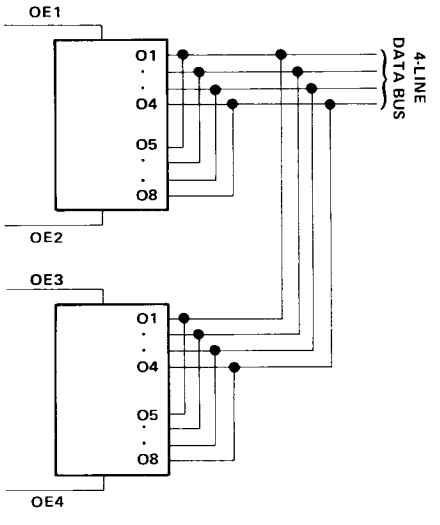
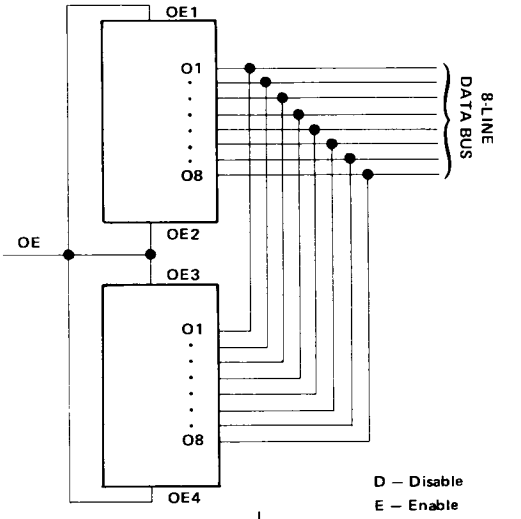
EXPANDED READ-ONLY MEMORY CONFIGURATIONS

8K x 4



WORDS	OE1	OE2	OE3	OE4
0–2048	E	D	D	D
2049–4096	D	E	D	D
4097–6144	D	D	E	D
6145–8192	D	D	D	E

4K x 8



WORDS	OE
0–2048	E
2049–4096	D

NOTE: One device programmed to enable with OE1 = OE2 = 1
Other device programmed to enable with OE1 = OE2 = 0

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SOFTWARE PACKAGE

The TMS 4800 JL, NL is a fixed program memory in which the programming is performed by TI, at the factory during the manufacturing cycle, to the specific customer inputs supplied in the format shown. The device is organized so that it can be used for storing either 2048 words of 8 bits or 4096 words of 4 bits. Words of 8- or 4-bit lengths are read by proper enable levels on OE1 and OE2. Output O1 is the least-significant bit in an 8-bit word, O5 and O1 in 4-bit words. All addresses and stored words in either organization are coded in octal. Any address up to 2048 can be written as a 4-digit octal number. Any 8-bit binary word can be converted to a 3-bit octal number. In coding, all binary words must be in positive logic and right justified before conversion to octal.

Every card must include the following coded information.

Column 73—OE1 enable code
Column 74—OE2 enable code
Columns 75—80 — TI CUSTOM DEVICE NUMBER ZAXXXX (4-DIGIT NUMBER ASSIGNED BY TI)

The output enable (OE) option is programmed on the chip with the customer pattern. A high voltage level enable is specified by a "1" in columns 73 or 74, a low voltage level enable by a "0".

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2048-word by 8-bits

Code deck format –

Card	Column	Octal Information
1	1–4	Octal address (N) of 1st output word on 1st card
	5–7	1st stored 8-bit word (in octal)
	8–10	2nd stored 8-bit word (in octal)
	•	
	•	
	•	
	50–52	16th stored 8-bit word (in octal)
2	1–4	Octal address (N + 16) of 1st output word on 2nd card
	5–7	17th stored 8-bit word
	•	
	•	
	•	
	50–52	32nd stored 8-bit word
128	1–4	Octal address (N + 2032) of 1st output word on 128th card
	5–7	2033rd stored 8-bit word
	•	
	•	
	•	
	50–52	2048th stored 8-bit word

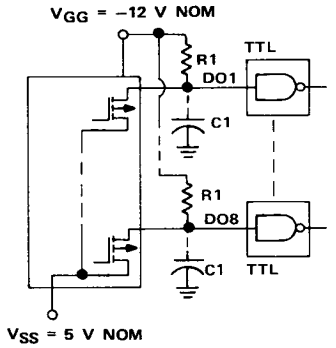
4096-word by 4-bits

Terminals OE1 and OE2 independently enable outputs O1-O4 and O5-O8. Each enable terminal can be programmed to enable with a high or low level input.

To read only 4 bits simultaneously from either set of output terminals, the stored information *must* be coded as an 8-bit positive logic binary word converted to octal. Each 4-bit binary word is right justified before forming the 8-bit word. In coding, words 1 and 2049, 2 and 2050, . . . and 2048 and 4096 are combined (O8-O5 on the left of O4-O1) as 8-bit words and converted to octal as in the case of the 2048 by 8 coding instructions. This coding format also requires 128 cards with 16 octal words (32 4-bit binary words) per card.

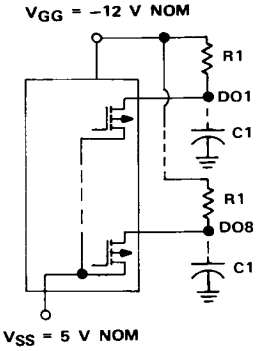
OUTPUT INTERFACE

single resistor TTL interface



R1 = 6.8 kΩ
C1 = 15 pF
MAX TTL FAN-OUT = 1

MOS interface



R1 = 12 kΩ
C1 = 10 pF

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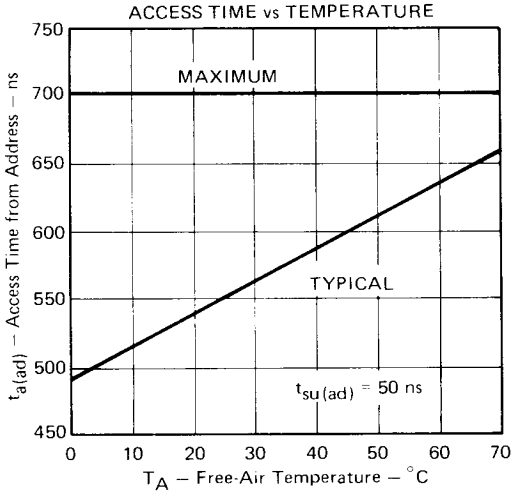
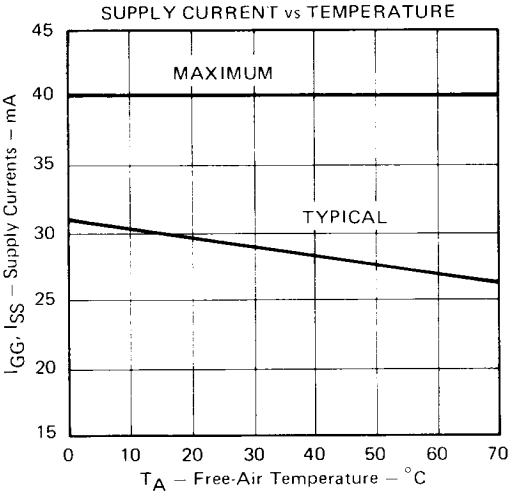
TYPICAL CHARACTERISTICS





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