## 4.2 TMS7002 and TMS7042 Specifications



### Table 4-6. Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)

| | |
|---|---|
| Supply voltage range, $V_{CC}$† | -0.3 V to 7 V |
| Input voltages range | -0.3 V to 7 V |
| Output voltages range | -0.3 V to 7 V |
| Maximum buffer current | ±10 mA |
| Continuous power dissipation | 1.4 W |
| Storage temperature range | -55°C to 150°C |

† Unless otherwise noted, all voltages are with respect to $V_{SS}$.

**Caution:**

**Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.**

### Table 4-7. Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | CLKIN | 2.6 | | | V |
| | | All other inputs | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | CLKIN | | | 0.6 | V |
| | | All other inputs | | | 0.8 | V |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## Table 4-8. Electrical Characteristics over Full Range of Operating Conditions

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input current | A5,MC,$\overline{RESET}$, $\overline{INT1}$, $\overline{INT3}$, XTAL2 | $V_I = V_{SS}$ to $V_{CC}$ | | ±2 | ±10 | µA |
| | | Ports C and D A0–A4, A6, A7 | $V_I$ = 0.4 V to $V_{CC}$ | | ±10 | ±100 | |
| $C_I$ | Input capacitance | | | | 2 | | pF |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = -400 µA | 2.4 | 2.8 | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OH}$ = 3.2 mA | | 0.2 | 0.4 | V |
| $t_{r(O)}$ | Output rise time‡ | | See Figure 4-7 | | 9 | 30 | ns |
| $t_{f(O)}$ | Output fall time‡ | | See Figure 4-7 | | 10 | 35 | ns |
| $I_{CC}$ | Supply current | | All outputs open | | 160 | 210 | mA |
| $P_{D(av)}$ | Average power dissipation | | | | 800 | 1155 | mW |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points (see Figure 4-8).

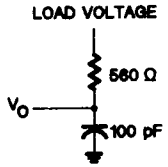



**Figure 4-6. Output Loading Circuit for Test**

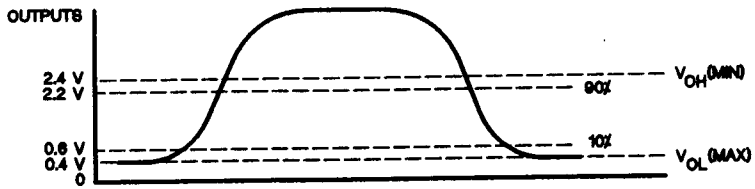



**Figure 4-7. Measurement Points for Switching Characteristics**

### Table 4-9. Recommended Crystal Operating Conditions over Full Operating Range

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{osc}$ | Crystal frequency | 1.0 | | 8.0 | MHz |
| | CLKIN duty cycle | | 50 | | % |
| $t_{c(P)}$ | Crystal cycle time‡ | 125 | | 1000 | ns |
| $t_{c(C)}$ | Internal state cycle time | 250 | | 2000 | ns |
| $t_{w(PH)}$ | CLKIN pulse duration high | 50 | | | ns |
| $t_{w(PL)}$ | CLKIN pulse duration low | 50 | | | ns |
| $t_r$ | CLKIN rise time† | | | 30 | ns |
| $t_f$ | CLKIN fall time† | | | 30 | ns |
| $t_{d(PH-CH)}$ | CLKIN rise to CLKOUT rise delay | | 70 | 200 | ns |

† Rise and fall times are measured between the maximum low level and the minimum high level.
‡ See Section 3.4 for Recommended Clock Connections.

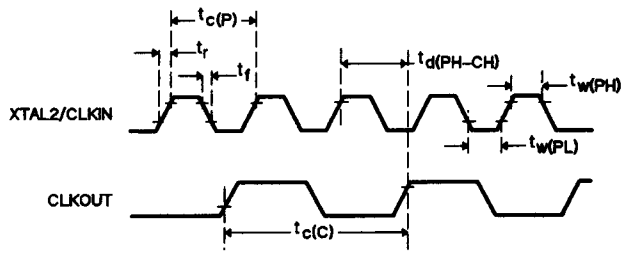



Figure 4-8. Clock Timing

## Table 4-10. Memory Interface Timing

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{c(C)}$ | CLKOUT cycle time† | 250 | 2000 | ns |
| $t_{w(CH)}$ | CLKOUT high pulse duration | $0.5t_{c(C)}$-40 | $0.5t_{c(C)}$+10 | ns |
| $t_{w(CL)}$ | CLKOUT low pulse duration | $0.5t_{c(C)}$-40 | $0.5t_{c(C)}$+15 | ns |
| $t_{d(CH-JL)}$ | Delay time, CLKOUT rise to ALATCH fall | $0.5t_{c(C)}$-10 | $0.5t_{c(C)}$+30 | ns |
| $t_{w(JH)}$ | ALATCH high pulse duration | $0.25t_{c(C)}$-15 | $0.25t_{c(C)}$+30 | ns |
| $t_{su(HA-JL)}$ | Setup time, high address valid before ALATCH fall | $0.25t_{c(C)}$-40 | $0.25t_{c(C)}$+45 | ns |
| $t_{su(LA-JL)}$ | Setup time, low address valid before ALATCH fall | $0.25t_{c(C)}$-40 | $0.25t_{c(C)}$+15 | ns |
| $t_{h(JL-LA)}$ | Hold time, low address valid after ALATCH fall | $0.25t_{c(C)}$ | $0.25t_{c(C)}$+45 | ns |
| $t_{su(RW-JL)}$ | Setup time, R/$\overline{W}$ valid before ALATCH fall | $0.25t_{c(C)}$-35 | $0.25t_{c(C)}$+30 | ns |
| $t_{h(EH-RW)}$ | Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise | $0.5t_{c(C)}$-40 | | ns |
| $t_{h(EH-HA)}$ | Hold time, high address valid after $\overline{ENABLE}$ rise | $0.5t_{c(C)}$-50 | | ns |
| $t_{su(Q-EH)}$ | Setup time, data output valid before $\overline{ENABLE}$ rise | $0.5t_{c(C)}$-45 | | ns |
| $t_{h(EH-Q)}$ | Hold time, data output valid after $\overline{ENABLE}$ rise | $0.5t_{c(C)}$-45 | | ns |
| $t_{d(LA-EL)}$ | Delay time, low address high impedance to $\overline{ENABLE}$ fall | $0.25t_{c(C)}$-45 | $0.25t_{c(C)}$ | ns |
| $t_{d(EH-A)}$ | Delay time, $\overline{ENABLE}$ rise to next address drive | $0.5t_{c(C)}$-25 | | ns |
| $t_{a(EL-D)}$ | Access time, data input valid after $\overline{ENABLE}$ fall | $0.75t_{c(C)}$-105 | | ns |
| $t_{a(A-D)}$ | Access time, address valid to data input valid | $1.5t_{c(C)}$-115 | | ns |
| $t_{d(A-EH)}$ | Delay time, address valid to $\overline{ENABLE}$ rise | $1.5t_{c(C)}$-80 | $1.5t_{c(C)}$+30 | ns |
| $t_{h(EH-D)}$ | Hold time, data input valid after $\overline{ENABLE}$ rise | 0 | | ns |
| $t_{d(EH-JH)}$ | Delay time, $\overline{ENABLE}$ rise to ALATCH rise | $0.5t_{c(C)}$-25 | $0.5t_{c(C)}$+10 | ns |
| $t_{d(CH-EL)}$ | Delay time, CLKOUT rise to $\overline{ENABLE}$ fall | -10 | 35 | ns |

† $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

## Table 4-11. Memory Interface Timing at 8 MHz

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{c(C)}$ | CLKOUT cycle time† | f = 8 MHz, 50% duty cycle | | 250 | | ns |
| $t_{w(CH)}$ | CLKOUT high pulse duration | | 85 | 110 | 135 | ns |
| $t_{w(CL)}$ | CLKOUT low pulse duration | | 85 | 115 | 140 | ns |
| $t_{d(CH-JL)}$ | Delay time, CLKOUT rise to ALATCH fall | | 115 | 135 | 155 | ns |
| $t_{w(JH)}$ | ALATCH high pulse duration | | 47 | 70 | 92 | ns |
| $t_{su(HA-JL)}$ | Setup time, high address valid before ALATCH fall | | 22 | 65 | 108 | ns |
| $t_{su(LA-JL)}$ | Setup time, low address valid before ALATCH fall | | 22 | 50 | 78 | ns |
| $t_{h(JL-LA)}$ | Hold time, low address valid after ALATCH fall | | 62 | 90 | 108 | ns |
| $t_{su(RW-JL)}$ | Setup time, R/$\overline{W}$ valid before ALATCH fall | | 27 | 60 | 93 | ns |
| $t_{h(EH-RW)}$ | Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise | | 85 | 120 | | ns |
| $t_{h(EH-HA)}$ | Hold time, high address valid after $\overline{ENABLE}$ rise | | 75 | 120 | | ns |
| $t_{su(Q-EH)}$ | Setup time, data output valid before $\overline{ENABLE}$ rise | | 80 | 120 | | ns |
| $t_{h(EH-Q)}$ | Hold time, data output valid after $\overline{ENABLE}$ rise | | 80 | 115 | | ns |
| $t_{d(LA-EL)}$ | Delay time, low address high impedance to $\overline{ENABLE}$ fall | | 17 | 40 | 62 | ns |
| $t_{d(EH-A)}$ | Delay time, $\overline{ENABLE}$ rise to next address drive | | 100 | 150 | | ns |
| $t_{a(EL-D)}$ | Access time, data input valid after $\overline{ENABLE}$ fall | | 82 | 120 | | ns |
| $t_{a(A-D)}$ | Access time, address valid to data input valid | | 260 | 300 | | ns |
| $t_{d(A-EH)}$ | Delay time, address valid to $\overline{ENABLE}$ rise | | 295 | 350 | 405 | ns |
| $t_{h(EH-D)}$ | Hold time, data input valid after $\overline{ENABLE}$ rise | | 0 | | | ns |
| $t_{d(EH-JH)}$ | Delay time, $\overline{ENABLE}$ rise to ALATCH rise | | 100 | 105 | 135 | ns |
| $t_{d(CH-EL)}$ | Delay time, CLKOUT rise to $\overline{ENABLE}$ fall | | -10 | 25 | 35 | ns |

† $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

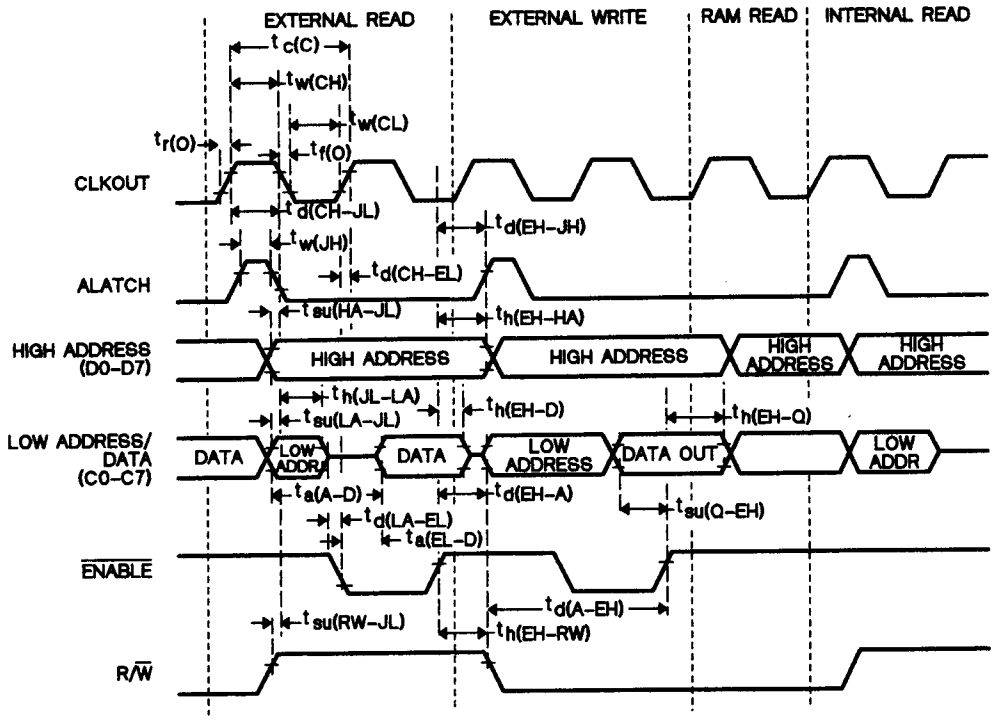



**Figure 4-9. Read and Write Cycle Timing**

### 4.2.1 Application of Ceramic Resonator

The circuit shown in Figure 4-10 provides an economical alternative to quartz crystals where frequency tolerance is not a major concern. Frequency tolerance over temperature is about 1%.



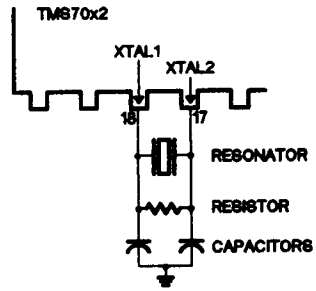



**Figure 4-10. Ceramic Resonator Circuit**

The following manufacturers supply ceramic resonators.

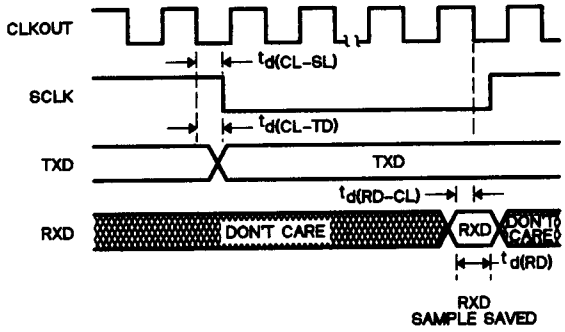
Murata Corporation of America
2200 Lake Park Dr.
Smyrna, GA 30080
(404) 436-1300
Telex - 4363030

For 5 MHz operation
Resonator ceralock CSA5.00MT
Resistor 1 MΩ 10%
Capacitors (both) 30 pF

Kyocera International
8611 Balboa Ave.
San Diego, CA 92123
(714) 279-8319
Telex - 697929

## 4.2.2 Serial Port Timing

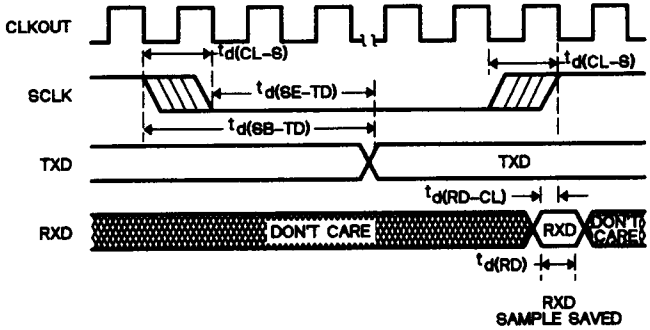
### *4.2.2.1 Internal Serial Clock*




**Notes:** 1) The CLKOUT signal is not available in Single-Chip mode.
2) CLKOUT = $t_{c(C)}$.

| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $t_{d(CL-SL)}$ | CLKOUT low to SCLK low | 1/4 $t_{c(C)}$ | ns |
| $t_{d(CL-TD)}$ | CLKOUT low to new TXD data | 1/4 $t_{c(C)}$ | ns |
| $t_{d(RD-CL)}$ | RXD data valid before CLKOUT low | 1/4 $t_{c(C)}$ | ns |
| $t_{d(RD)}$ | RXD data valid time | 1/2 $t_{c(C)}$ | ns |

### *4.2.2.2 External Serial Clock*

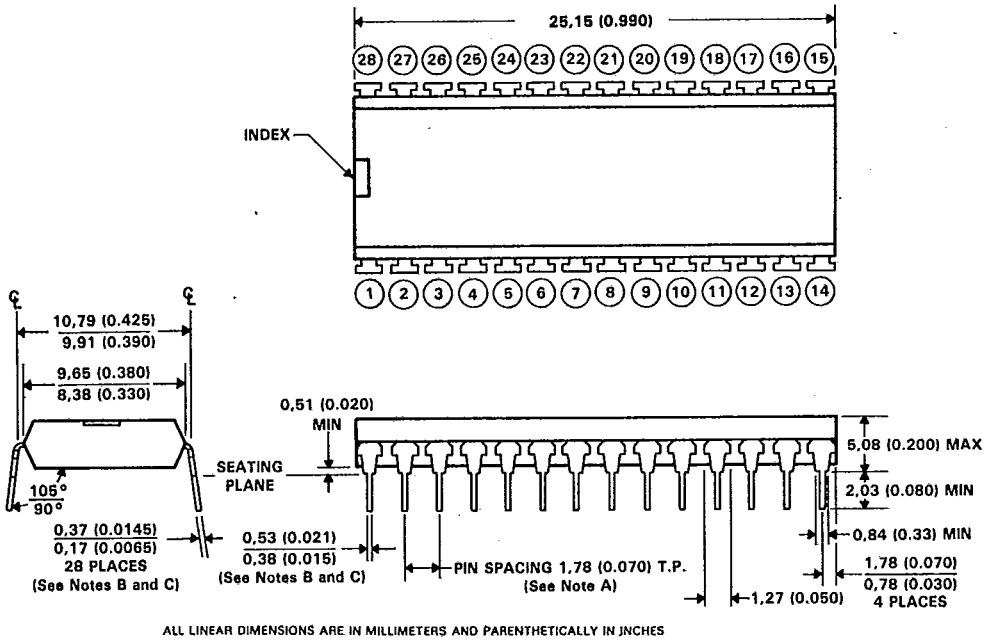



**Notes:** 1) The CLKOUT signal is not available in Single-Chip mode.
2) CLKOUT = $t_{c(C)}$.
3) SCLK sampled; if SCLK = 1 then 0, fall transition found.
4) SCLK sampled; if SCLK = 0 then 1, rise transition found.

| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $t_{d(RD-CL)}$ | RXD data valid before CLKOUT low | 1/4 $t_{c(C)}$ | ns |
| $t_{d(RD)}$ | RXD data valid time | 1/2 $t_{c(C)}$ | ns |
| $t_{d(SB-TD)}$ | Start of SCLK sample to new TXD data | 3 1/4 $t_{c(C)}$ | ns |
| $t_{d(SE-TD)}$ | End of SCLK sample to new TXD data | 2 1/4 $t_{c(C)}$ | ns |
| $t_{d(CL-S)}$ | Clockout low to SCLK transition | $t_{c(C)}$ | ns |

T-90-20

## 28-pin N2 plastic package




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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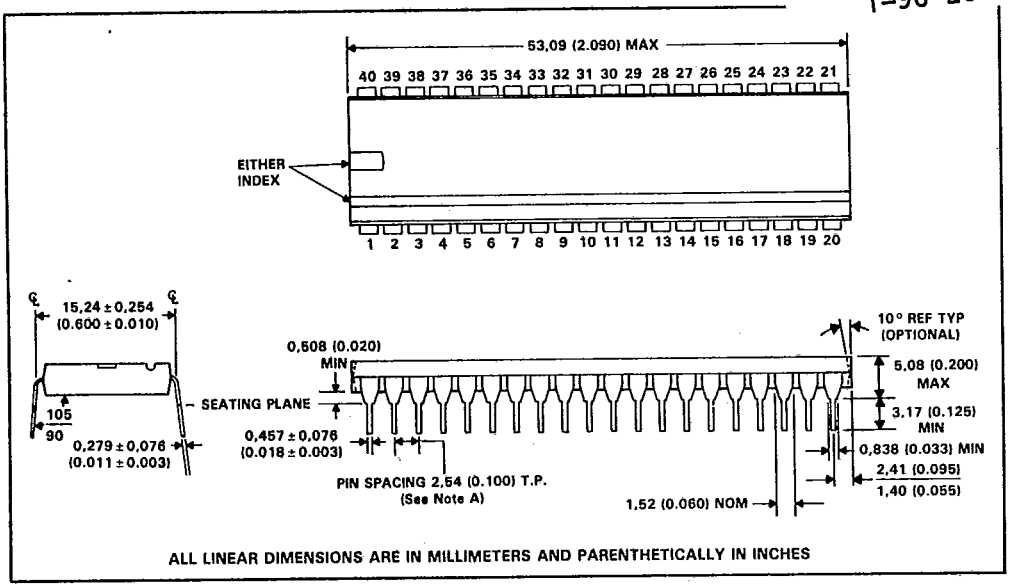
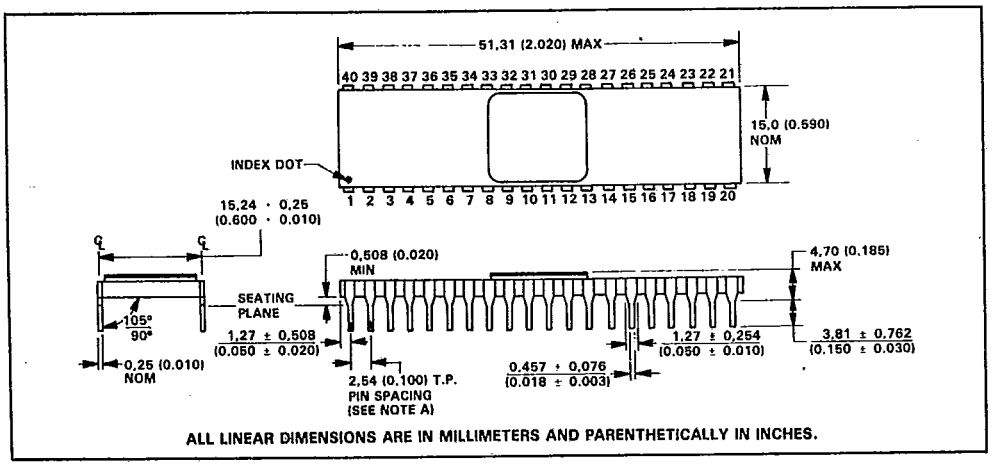
**Figure 12-2. 28-Pin Plastic Package, 70-MIL Pin Spacing (Type N2 Package Suffix)**

T-90-20




NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.

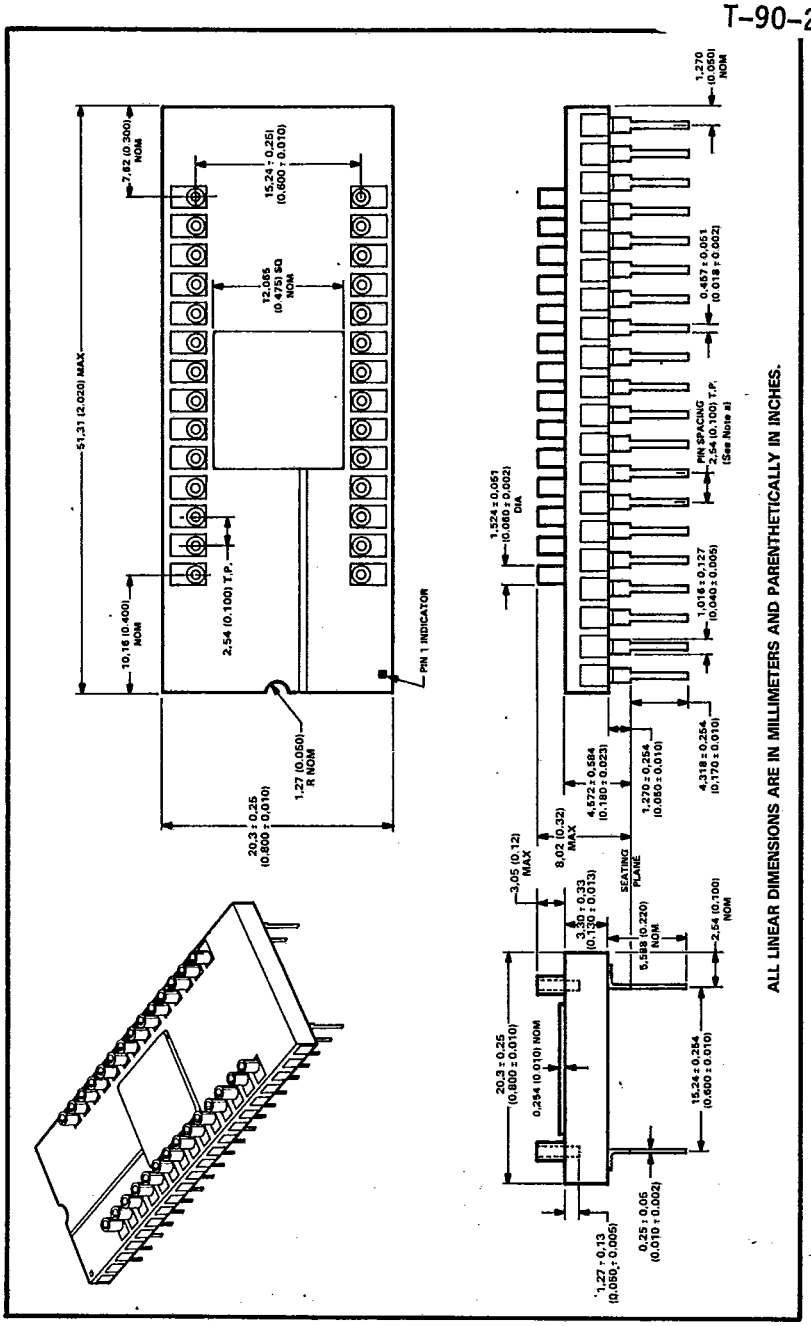
**Figure 12-3. 40-Pin Plastic Package, 100-MIL Pin Spacing (Type N Package Suffix)**




NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.

**Figure 12-4. 40-Pin Ceramic Package, 100-MIL Pin Spacing (Type JD Package Suffix)**

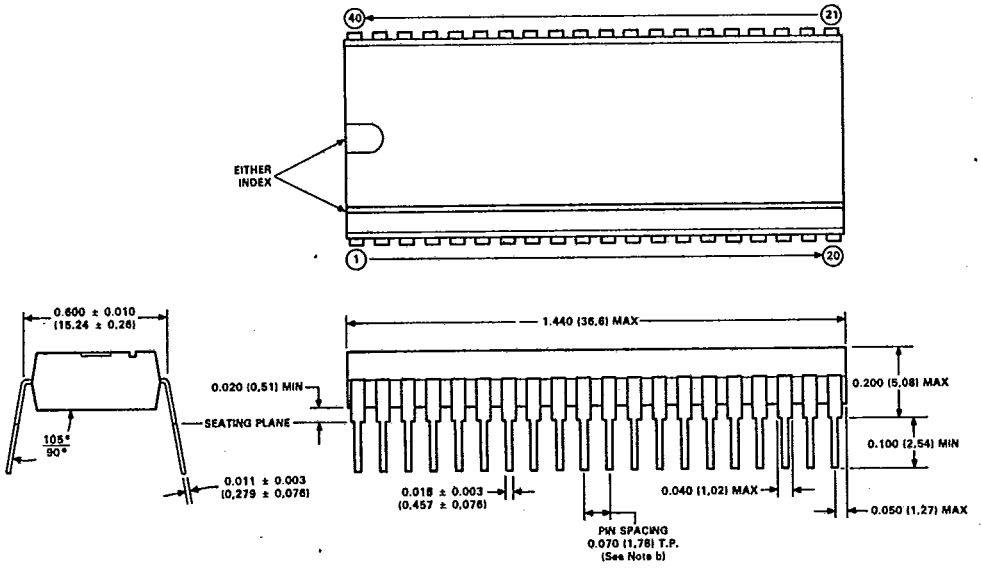
12




NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.

**Figure 12-5. 40-Pin Ceramic Piggyback Package, 100-MIL Pin Spacing (Type JD Package Suffix)**

12




NOTES: a. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

**Figure 12-6. 40-Pin N2 Plastic Package, 0.070 "Pin Center Spacing, 0.600" Pin Row Spacing**

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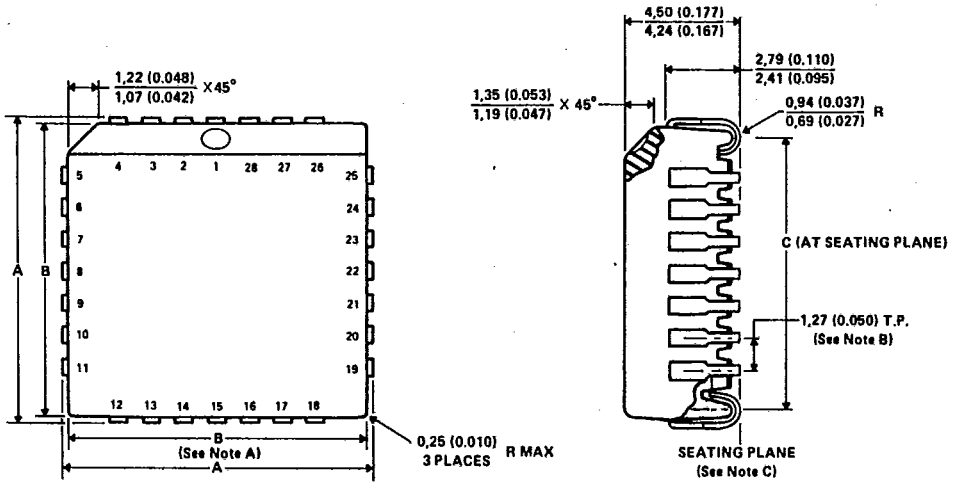
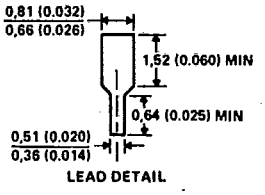
## Customer Information – Mechanical Package Information

T-90-20




| NO. OF TERMINALS | A MIN | A MAX | B MIN | B MAX | C MIN | C MAX |
|---|---|---|---|---|---|---|
| 20 | 9,78 (0.385) | 10,03 (0.395) | 8,89 (0.350) | 9,04 (0.356) | 7,87 (0.310) | 8,38 (0.330) |
| 28 | 12,32 (0.485) | 12,57 (0.495) | 11,43 (0.450) | 11,58 (0.456) | 10,41 (0.410) | 10,92 (0.430) |
| 44 | 17,40 (0.685) | 17,65 (0.695) | 16,51 (0.650) | 16,66 (0.656) | 15,49 (0.610) | 16,00 (0.630) |
| 68 | 25,02 (0.985) | 25,27 (0.995) | 24,13 (0.950) | 24,33 (0.956) | 23,11 (0.910) | 23,62 (0.930) |




12

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

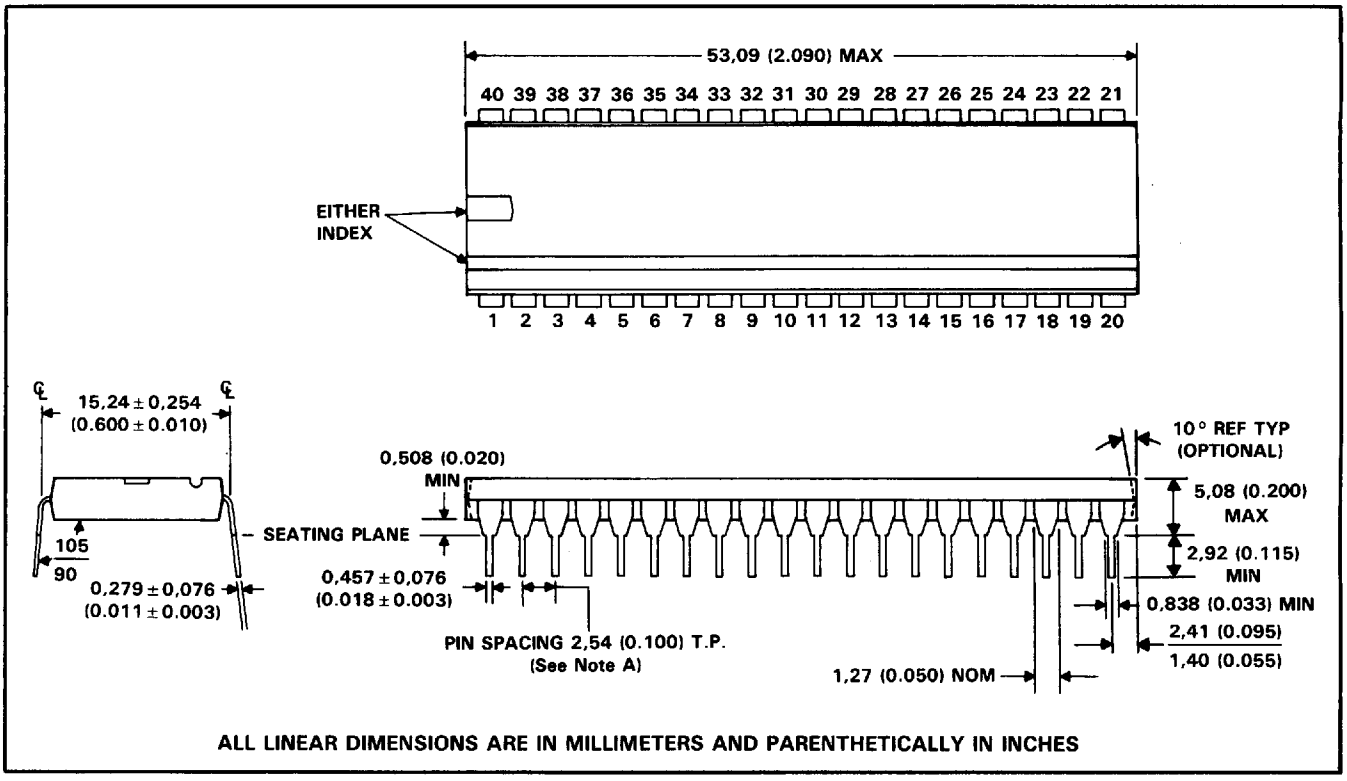
NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

**Figure 12-7. 44-Pin Plastic-Leaded Chip Carrier FN Package**

## MECHANICAL DATA

T-90-20

### 40-pin N dual-in-line package




NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.