PRELIMINARY DATA SHEET

BU-64703

SIMPLE SYSTEM RT Mark3 (SSRT Mark3)

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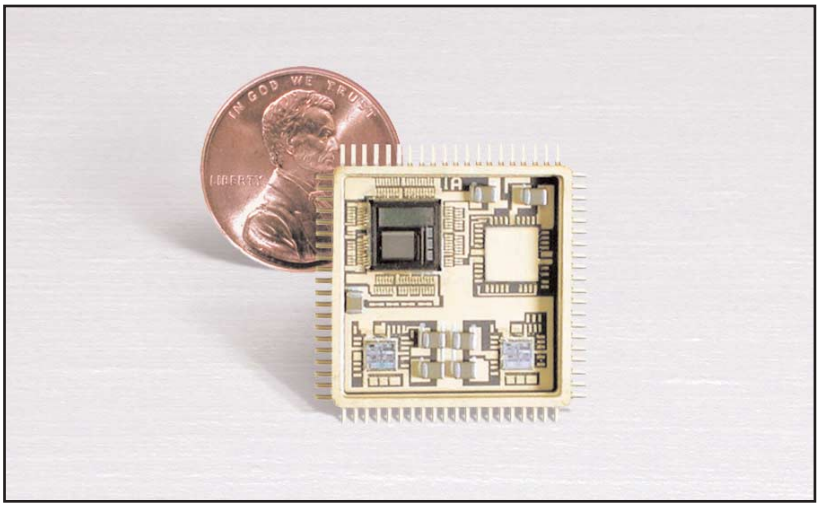

DESCRIPTION

The BU-64703 Simple System RT Mark3 (SSRT Mark3) MIL-STD-1553 terminals provide a complete interface between a simple system and a MIL-STD-1553 bus. The SSRT Mark3 is powered entirely by 3.3 volts, thus eliminating the need for a 5V power supply. This terminal integrates dual transceiver, protocol logic, and a FIFO memory for received messages in a 0.88 inch square ceramic package. The gull wing package with a “toe-to-toe” maximum dimension of 1.13 inches enables its use in applications where PC board space is at a premium. The SSRT Mark3 provides multi-protocol support of MIL-STD-1553A/B, MIL-STD-1760, McAir, and STANAG-3838.

The SSRT Mark3's transceivers are completely monolithic, require only a +3.3V supply, and consume low power. The internal architecture is identical to that of the original BU-61703/61705 Simple System RT (SSRT). There are versions of the Simple System RT Mark3 available with transceivers trimmed for MIL-STD-1760 compliance, or compatible to McAir standards. The SSRT Mark3 can operate with a choice of clock frequencies of 10, 12, 16, or 20 MHz.

The SSRT Mark3 incorporates a built-in self-test (BIT). This BIT, which is processed following power turn-on or after receipt of an Initiate Self-Test Mode command, provides a comprehensive test of the SSRT Mark3's encoders, decoders, protocol, transmitter watchdog timer, and protocol section. The SSRT Mark3 also includes an auto-configuration feature.

The SSRT Mark3 is ideal for stores and other simple systems that do not require a microprocessor. To streamline the interface to simple systems, the SSRT Mark3 includes an internal 32-word FIFO for received data words. This serves to ensure that only complete, consistent blocks of validated data words are transferred to a system.

FEATURES

- Complete Integrated Remote Terminal Including:
  - All 3.3Volt Terminal (No Other Power Supplies Are Required)
  - Dual Low-Power 3.3V Only Transceivers
  - Complete RT Protocol Logic
- Supports MIL-STD-1553A/B Notice 2, STANAG-3838 RT, and MIL-STD-1760 Stores Management
- 0.88” X 0.88”, 0.130”, Max Height CQFP
- 80-Pin Ceramic Flatpack or Gullwing Package
- 3.3V Logic Power
- Meets 1553A/McAir Response Time Requirements
- Internal FIFO for Burst Mode Capability on Receive Data
- 16-bit DMA Interface
- Auto Configuration Capability
- Comprehensive Built-In Self-Test
- Direct Interface to Simple (Processorless) Systems
- Available with Full Military Temperature Range and Screening
- Selectable Input Clock: 10, 12, 16, or 20 MHz

This Preliminary data sheet provides detailed functional capabilities for product currently in prototype production. These specifications are being provided to allow for electrical design, layout and operation.

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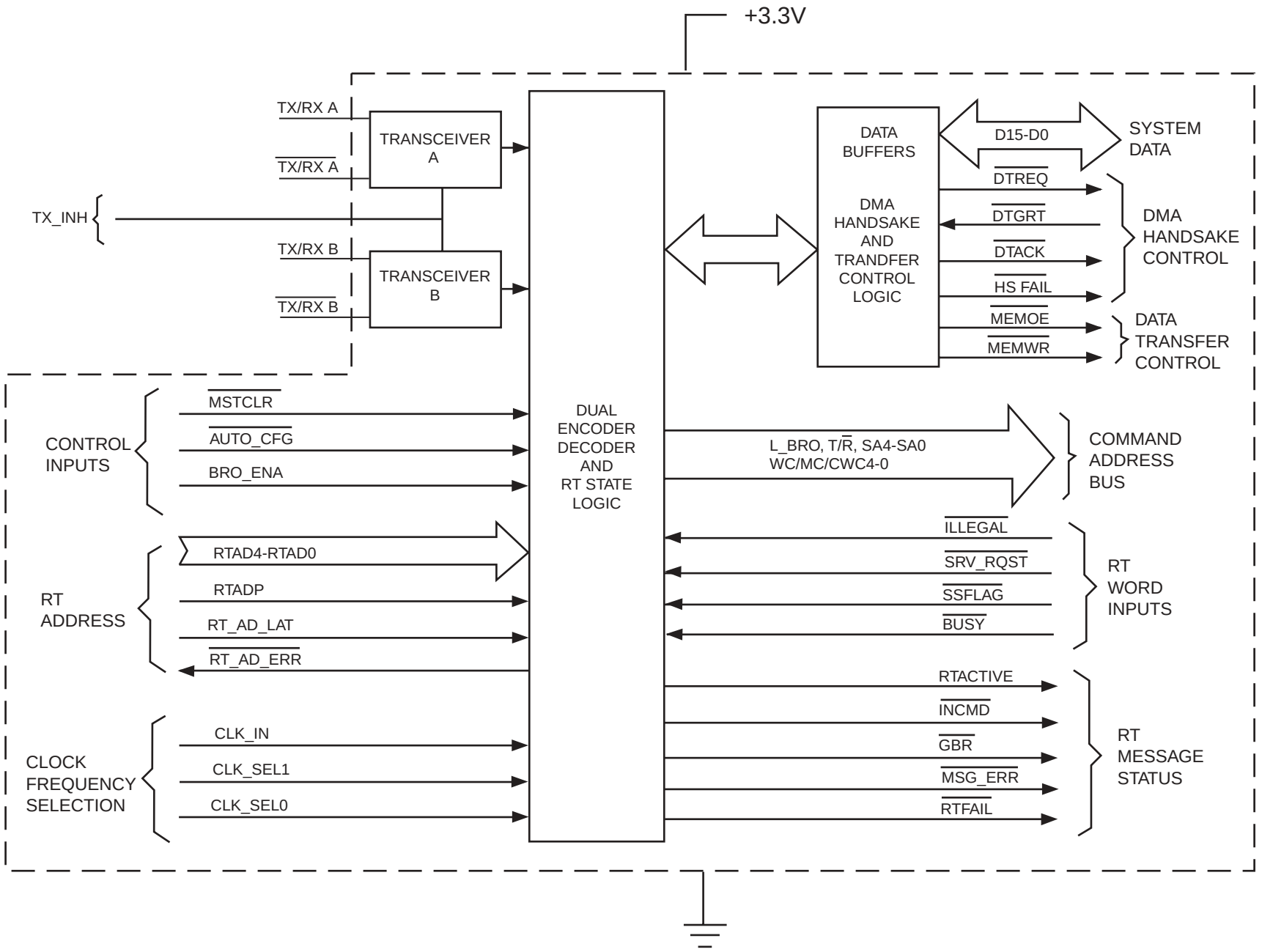


FIGURE 1. SSRT Mark3 BLOCK DIAGRAM

TABLE 1. SSRT Mark3 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATING				
Supply Voltage (Note 10)				
• Logic (Voltage Input Range)	-0.3		6.0	V
• Transceivers	-0.3		6.0	V
(not during transmit)				
• Transceiver (during transmit)	-0.3		4.5	V
RECEIVER				
Differential Input Resistance (Notes 1-6)	2.5			kΩ
Differential Input Capacitance (Notes 1-6)			5	pF
Threshold Voltage, Transformer Coupled, Measured on Stub	0.200		0.860	Vp-p
Common Mode Voltage (Note 7)			10	Vpeak
TRANSMITTER				
Differential Output Voltage (Note 8)				
• Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	Vp-p
• Transformer Coupled Across 70 Ω, Measured on Bus				
BU-64703XX-XX0	18	20	27	Vp-p
BU-64703X8-XX2 (Note 9)	20	22	27	Vp-p
Output Noise, Differential (Direct Coupled)			10	mVp-p
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250		250	mV_{peak}
Rise/Fall Time				
BU-64703X8	100	150	300	nsec
BU-64703X9	200	250	300	nsec
LOGIC				
V_{IH}				
All signals except CLOCK_IN	2.1			V
CLOCK_IN	0.8•Vcc			V
V_{IL}				
All signals except CLOCK_IN			0.7	V
CLOCK_IN			0.2•Vcc	V
Schmidt Hysteresis				
All signals except CLOCK_IN	0.4			V
CLOCK_IN	1.0			V
I_{IH}, I_{IL}				
All signals except CLOCK_IN				
I_{IH} (Vcc=3.6V, V_{IN}=Vcc)	-10		10	µA
I_{IH} (Vcc=3.6V, V_{IH}=2.7V)	-350		-33	µA
I_{IL} (Vcc=3.6V, V_{IH}=0.4V)	-350		-33	µA
CLOCK_IN				
I_{IH}	-10		10	µA
I_{IL}	-10		10	µA
V_{OH} (Vcc=3.0V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OH}=max)	2.4			V
V_{OL} (Vcc=3.0V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OL}=max)			0.4	V
I_{OL}	3.4			mA
I_{OH}			-3.4	mA
C_I (Input Capacitance)		50		pF
C_{IO} (Bi-directional signal input capacitance)		50		pF

TABLE 1. SSRT Mark3 SPECIFICATIONS (Cont'd)

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (Note 10)				
• +3.3V Logic	3.14	3.3	3.46	V
• +3.3V Transceivers	3.14	3.3	3.46	V
Current Drain(Total Hybrid)(Notes 8,14)				
• BU-64703X8/9-XX0,(1553 & McAir)				
• Idle			95	mA
• 25% Transmitter Duty Cycle			310	mA
• 50% Transmitter Duty Cycle			525	mA
• 100% Transmitter Duty Cycle			955	mA
• BU-64703X8-XX2, (1760)				
• Idle			95	mA
• 25% Transmitter Duty Cycle			332	mA
• 50% Transmitter Duty Cycle			583	mA
• 100% Transmitter Duty Cycle			1.041	A
POWER DISSIPATION				
Total Hybrid (Notes 8, 11 and 14)				
• BU-64703X8/9-XX0, (1553 & McAir)				
• Idle			0.31	W
• 25% Transmitter Duty Cycle			0.67	W
• 50% Transmitter Duty Cycle			1.02	W
• 100% Transmitter Duty Cycle			1.72	W
• BU-64703X8-XX2, (1760)				
• Idle			0.31	W
• 25% Transmitter Duty Cycle			0.74	W
• 50% Transmitter Duty Cycle			1.16	W
• 100% Transmitter Duty Cycle			2.01	W
Hottest Die				
• BU-64703X8/9-XX0 (1553 &McAir)				
• Idle			0.09	W
• 25% Transmitter Duty Cycle			0.45	W
• 50% Transmitter Duty Cycle			0.80	W
• 100% Transmitter Duty Cycle			1.51	W
• BU-64703X8-XX2 (1760)				
• Idle			0.09	W
• 25% Transmitter Duty Cycle			0.54	W
• 50% Transmitter Duty Cycle			0.95	W
• 100% Transmitter Duty Cycle			1.80	W
CLOCK INPUT				
Frequency				
• Nominal Value				
• Default		16.0		MHz
• Option		12.0		MHz
• Option		10.0		MHz
• Option		20.0		MHz
• Long Term Tolerance				
• 1553A Compliance	0.01		-0.01	%
• 1553B Compliance	0.10		-0.10	%
• Short Term Tolerance, 1 second				
• 1553A Compliance	-0.001		0.001	%
• 1553B Compliance	-0.01		0.01	%
• Duty Cycle	40		60	%

TABLE 1. SSRT Mark3 SPECIFICATIONS (Cont'd)

PARAMETER	MIN	TYP	MAX	UNITS
1553 MESSAGE TIMING				
RT-to-RT Response Timeout (Note 12)	17.5	18.5	19.5	µs
RT Response Time (mid-parity to mid-sync) (Note 12)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
Thermal Resistance (Notes 8, 13) Ceramic Flatpack / Gull Lead Junction-to-Case, Hottest Die (θ_{JC})		9	11	°C/W
Operating Case Temperature				
-1XX, -4XX	-55		+125	°C
-2XX, -5XX	-40		+85	°C
-3XX, -8XX	0		+70	°C
Operating Junction Temperature	-55		155	°C
Storage Temperature	-65		155	°C
Lead Temperature (soldering, 10 sec.)			+300	°C
PHYSICAL CHARACTERISTICS				
Size 80-pin Ceramic Flatpack / Gull Lead	0.88 X 0.88 X 0.13 (22.3 x 22.3 x 3.3)			in. (mm)
Lead Toe-Toe Distance 80-pin Gull Wing	1.13 (28.7)			in. (mm)
Weight 80-pin Ceramic Flatpack/Gull Wing Package	0.353 (10)			oz (g)

NOTES:

Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance Specifications:

(1) Specifications include both transmitter and receiver (tied together internally).

(2) Impedance parameters are specified directly between pins TX/RX A(B) and $\overline{\text{TX/RX A(B)}}$ of the SSRT Mark3 hybrid.

(3) It is assumed that all power and ground inputs to the hybrid are connected.

(4) The specifications are applicable for both unpowered and powered conditions.

(5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.

(6) Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.

(7) Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to the pins of the isolation transformer on the stub side (either direct or transformer coupled), and referenced to hybrid ground. Transformer must be a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.

(8) An "X" in one or more of the product type fields indicates that the reference is applicable to all available product options.

(9) MIL-STD-1760 requires a 20 Vp-p minimum output on the stub connection.

(10) External 10 µF tantalum and 0.1 µF capacitors to ground should be located as close as possible to +3.3 Vdc input pins.

(11) Power dissipation specifications assume a transformer coupled configuration, with external dissipation (while transmitting) of 0.14 watts for the active isolation transformer, 0.08 watts for the active bus coupling transformer, 0.45 watts for each of the two bus isolation resistors, and 0.15 watts for each of the two bus termination resistors.

(12) Measured from mid-parity crossing of command word to mid-sync crossing of RT's status word.

(13) θ_{JC} is measured to bottom of ceramic case.

(14) Current drain and power dissipation specs are preliminary and subject to change.

INTRODUCTION

GENERAL

The BU-64703 Simple System RT Mark3 (SSRT Mark3) is a complete MIL-STD-1553 Remote Terminal (RT) bus interface unit. Contained in this hybrid are a dual transceiver and Manchester II encoder/decoder, and MIL-STD-1553 Remote Terminal (RT) protocol logic. Also included are built-in self-test capability and a parallel subsystem interface. The subsystem interface includes a 12-bit address bus and a 16-bit data bus that operates in a 16-bit DMA handshake transfer configuration. The local bus and associated control signals are optimized for +3.3 volt logic but are +5 volt tolerant.

The transceiver front end of the SSRT Mark3 is implemented by means of low-power monolithic technology. The transceiver requires only a single +3.3 V voltage source. The voltage source transmitters provide superior line driving capability for long cables and heavy amounts of bus loading. In addition, the monolithic transceivers can provide a minimum stub voltage level of 20 volts peak-to-peak transformer coupled, making the SSRT Mark3 suitable for MIL-STD-1760 applications. To provide compatability to McAir specs, the SSRT Mark3 is available with an option for transmitters with increased rise and fall times.

Besides eliminating the demand for an additional power supply, the use of a +3.3V only transceiver requires the use of a step-up, rather than a step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15V, 12V or 5V transmitter. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test. This allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

The receiver sections of the SSRT Mark3 are fully compliant with MIL-STD-1553B in terms of front-end overvoltage protection, threshold, and bit-error rate.

The SSRT Mark3 implements all MIL-STD-1553 message formats, including all 13 MIL-STD 1553 dual redundant mode codes. Any subset of the possible 1553 commands (broadcast, T/R bit, subaddress, word count/mode code) may be optionally illegalized by means of an external PROM, PLD, or RAM. An extensive amount of message validation is performed for each message received. Each word received is validated for correct sync type and sync encoding, Manchester II encoding, parity, and bit count. All messages are verified to contain a legal, defined command word and correct word count. If the SSRT Mark3 is the receiving RT in an RT-to-RT transfer, it verifies that the T/R bit of the transmit command word is logic "1" and that the transmitting RT responds in time and contains the correct RT address in its Status Word.

The SSRT Mark3 may be operated from a 10, 12, 16, or 20 MHz clock input. For any clock frequency, the decoder samples incoming data on **both** edges of the clock input. This oversampling, in effect, provides for a sampling rate of twice the input clocks' frequency. Benefits of the higher sampling rate include a wider tolerance for zero-crossing distortion and improved bit error rate performance.

The SSRT Mark3 includes a hardwired RT address input. This includes 5 address lines, an address parity input, and an address parity error output. The RT address can also be latched by means of a latching input signal.

The SSRT Mark3 supports command illegalization. Commands may be illegalized by asserting the input signal $\overline{\text{ILLEGAL}}$ active low within approximately 2 µs after the mid-parity bit zero-crossing of the received command word. Command words may be illegalized as a function of broadcast, T/R bit, subaddress, word count, and/or mode code.

An internal Built-in-Test (BIT) Word register is updated at the end of each message. The contents of the BIT Word Register are transmitted in response to a Transmit BIT Word Mode Command. The SSRT Mark3 provides a number of real-time output signals. These various signals provide indications of message in progress, valid received message, message error, handshake fail, loop-test fail or transmitter timeout.

The SSRT Mark3 includes standard DMA handshake signals (Request, Grant, and Acknowledge) as well as transfer control outputs ($\overline{\text{MEMOE}}$ and $\overline{\text{MEMWR}}$). The DMA interface operates in a 16-bit mode, supporting word-wide transfers.

The SSRT Mark3's system interface allows the SSRT Mark3 to be interfaced directly to a simple system that doesn't include a microprocessor. This provides a low-cost 1553 interface for A/D and D/A converters, switch closures, actuators, and other discrete I/O signals.

The SSRT Mark3 has an internal FIFO for received data words. This 32-word deep FIFO may be used to allow the SSRT Mark3 to transfer its data words to the local system in burst mode. Burst mode utilizes the FIFO by transferring data to the local bus at a rate of one data word every three clock cycles. Burst mode negotiates only once for use of the subsystem bus. Negotiation is performed only after all 1553 data words have been received and validated. In non-burst mode, the SSRT Mark3 will negotiate for the local bus after every received data word. The data word transfer period is three clock cycles for each received 1553 data word.

The SSRT Mark3 may also be used in a shared RAM interface configuration. By means of tri-state buffers and a small amount of "glue" logic, the SSRT Mark3 will store Command Words and access Data Words to/from dedicated "mailbox" areas in a shared RAM for each broadcast / T/R bit / subaddress / mode code.

ADDRESS MAPPING

A typical addressing scheme for the SSRT Mark3 12-bit address bus could be as follows:

A11: BROADCAST/$\overline{\text{OWNADDRESS}}$

A10: TRANSMIT/$\overline{\text{RECEIVE}}$

A9-A5: SUBADDRESS 4-0

A4-A0: WORD COUNT/MODE CODE 4-0

This method of address mapping provides for a "mailbox" allocation scheme for the storage of data words. The 12 address outputs may be used to map into 4K words of processor address space. The SSRT Mark3's addressing scheme maps messages in terms of broadcast/ownaddress, transmit/receive, subaddress, and word/count mode code. A 32-word message block is allocated for each T/R-subaddress.

For non-mode code messages, the Data Words to be transmitted or received are accessed from (to) relative locations 0 through 31 within the respective message block. For the MIL-STD-1553B Synchronize with data, Selected transmitter shutdown, Override selected transmitter shutdown, and Transmit vector word mode commands which involve a single data word transfer, the address for the data word is offset from location 0 of the message block for subaddresses 0 and 31 by the value of the mode code field of the received command word.

The data words transmitted in response to the Transmit last command or Transmit BIT word mode commands are accessed from a pair of internal registers.

DMA INTERFACE

A 16-bit data bus, a 12-bit address bus, and six control signals are provided to facilitate communication with the parallel subsystem. The data bus D15-D0 consists of bi-directional tri-state signals. The address bus L_BRO, T/$\overline{R}$, SA4-SA0, and WC/MC/CWC4-0; along with the data transfer control signals $\overline{MEMOE}$ and $\overline{MEMWR}$ are two-state output signals.

The control signals include the standard DMA handshake signals $\overline{DTREQ}$, $\overline{DTGRT}$, $\overline{DTACK}$, as well as the transfer control outputs $\overline{MEMOE}$ and $\overline{MEMWR}$. $\overline{HS\_FAIL}$ provides an indication to the subsystem of a handshake failure condition.

Data transfers between the subsystem and the SSRT Mark3 are performed by means of a DMA handshake, initiated by the SSRT Mark3. A data read operation is defined to be the transfer of data from the subsystem to the SSRT Mark3. Conversely, a data write operation transfers data from the SSRT Mark3 to the subsystem. Data is transferred as a single 16-bit word.

DMA READ OPERATION

In response to a transmit command, the SSRT Mark3 needs to read data words from the external subsystem. To initiate a data word read transfer, the SSRT Mark3 asserts the signal $\overline{DTREQ}$ low. Assuming that the subsystem asserts $\overline{DTGRT}$ in time, the SSRT Mark3 will then assert the appropriate values of L_BRO (logic "0"), T/$\overline{R}$ (high), SA4-0, and MC/CWC4-0; $\overline{MEMWR}$ high, along with $\overline{DTACK}$ low and $\overline{MEMOE}$ low to enable data to be read from the subsystem.

After the transfer of each Data Word has been completed, the value of the address bus outputs CWC4 through CWC0 is incremented.

DMA WRITE OPERATION

In response to a receive command, the SSRT Mark3 will need to transfer data to the subsystem. There are two options for doing this, the burst mode and the non-burst mode. In burst mode, all received data words are transferred from the SSRT Mark3 to the subsystem in a contiguous burst, only following the reception of the correct number of valid data words. In the non-burst mode, single data words are written to the external subsystem immediately following the reception of each individual data word.

To initiate a DMA write cycle, the SSRT Mark3 asserts $\overline{DTREQ}$ low. The subsystem must then respond with $\overline{DTGRT}$ low. Assuming that $\overline{DTGRT}$ was asserted in time, the SSRT Mark3 will then assert $\overline{DTACK}$ low. The SSRT Mark3 will then assert the appropriate value of L_BRO, T/$\overline{R}$, SA4-0, and MC/CWC4-0, $\overline{MEMOE}$ high, and $\overline{MEMWR}$ low. $\overline{MEMWR}$ will be asserted low for one clock cycle. The subsystem may then use either the falling or rising edge of $\overline{MEMWR}$ to latch the data. Similar to the DMA read operation, the address outputs CWC4 through CWC0 are incremented after the completion of a DMA write operation.

HANDSHAKE FAIL

Following the assertion of $\overline{DTREQ}$ low by the SSRT Mark3, the external subsystem has 10 µs to respond by asserting $\overline{DTACK}$ to logic "0".

If the SSRT Mark3 (SSRT Mark3) asserts $\overline{DTREQ}$ and the subsystem does not respond with $\overline{DTGRT}$ in time for the SSRT Mark3 to complete a data word transfer, the $\overline{HSFAIL}$ output will be asserted low to inform the subsystem of the handshake failure, and bit 12 in the internal Built-In-Test (BIT) word will be set to logic "1". If the handshake failure occurs on a data word read transfer (for a transmit command), the SSRT Mark3 will abort the current message transmission. In the case of a handshake failure on a write transfer (received command) the SSRT Mark3 will set the handshake failure output and BIT word bit, and abort processing the current message.

MESSAGE PROCESSING OPERATION

Following the receipt and transfer of a valid Command Word, the SSRT Mark3 will attempt to perform one of the following operations: (1) transfer received 1553 data to the subsystem, (2) read data from the subsystem for transmission on the 1553 bus, (3) transmit status (and possibly the last command word or RT BIT word) on the 1553 bus, and/or (4) set status word conditions.

The SSRT Mark3 responds to all non-broadcast messages to its RT address with a 1553 Status Word.

RT ADDRESS

RT Address 4-0 (RT_AD_4 = MSB) and RT Address Parity (RT_AD_P) should be programmed for a unique RT address and reflect an odd parity sum. The SSRT Mark3 will not respond to any MIL-STD-1553 commands or transfer received data from any non-broadcast messages if an odd parity sum is not presented by RT_AD_4-0 and RT_AD_P. An address parity error will be indicated by a low output on the $\overline{RT\_AD\_ERR}$ pin. The input signal RT_AD_LAT operates a transparent latch for RTAD4-RTAD0 and RTADP. If RT_AD_LAT is low, the output of the latch tracks the value presented on the input pins. If RT_AD_LAT is high, the output of the internal latch becomes latched to the val-

ues presented at the time of a low-to-high transition of RT_AD_LAT.

RT address and RT Address Parity must be presented valid before the mid-parity crossing of the 1553 command and held, at least, until following the first received data word.

COMMAND ILLEGALIZATION

The SSRT Mark3 includes a provision for command illegalization. If a command is illegalized, the SSRT Mark3 will set the Message error bit and transmit its status word to the Bus Controller. No data words will be transmitted in response to an illegalized transmit command. However, data words associated with an illegalized receive command **will** be written to the external subsystem (although these transfers may be blocked using external logic).

$\overline{\text{ILLEGAL}}$ is sampled approximately 2 µs following the mid-parity bit zero crossing of the received command word. A low on $\overline{\text{ILLEGAL}}$ will illegalize a particular command word and cause the SSRT Mark3 to respond with its Message error bit set in its status word. Command illegalization based on broadcast, T/$\overline{\text{R}}$ bit, subaddress, and/or word count/mode code may be implemented by means of an external PROM, PLD, or RAM device, as shown in Figure 2.

The external device may be used to define the legality of specific commands. Any subset of the possible 1553 commands may be illegalized as a function of broadcast, T/$\overline{\text{R}}$ bit, subaddress, word count, and/or mode code. The output of the illegalization device should be tied directly to the SSRT Mark3's $\overline{\text{ILLEGAL}}$ signal input. The maximum access time of the external illegalizing device is 400 ns.

If illegalization is not used, $\overline{\text{ILLEGAL}}$ should be hardwired to logic "1".

BUSY

The external subsystem may control the SSRT Mark3's Busy RT status word bit by means of the $\overline{\text{BUSY}}$ input signal. The SSRT Mark3 samples $\overline{\text{BUSY}}$ approximately 2 µs following the mid-parity bit zero crossing of the received Command Word. If $\overline{\text{BUSY}}$ is sampled low for a particular message, the value of the busy bit transmitted in the SSRT Mark3's status word will be logic "1". If $\overline{\text{BUSY}}$ is sampled high for a particular message, the value of the busy bit transmitted in the SSRT Mark3's status word will be logic "0".

If the RT responds to a transmit command with a busy bit of logic "1", the status word will be transmitted, but no data words will be transmitted by the SSRT Mark3. If the SSRT Mark3 responds to a receive command with a busy bit of logic "1", data words **will be** transferred to the external subsystem (although these may be blocked by means of external logic).

Similar to $\overline{\text{ILLEGAL}}$, it is possible to cause the SSRT Mark3 to respond with Busy for specific command words (only), by means of an external PROM, RAM, or PLD device.

TRANSMIT COMMAND (RT-TO-BC TRANSFER)

If the SSRT Mark3 receives a valid Transmit command word that the subsystem determines is legal (input signal $\overline{\text{ILLEGAL}}$ is high) and the subsystem is not BUSY (input signal $\overline{\text{BUSY}}$ is high), the SSRT Mark3 will initiate a transmit data response following transmission of its status word. This entails a handshake/read cycle for each data word transmitted, with the number of data words to be transmitted specified by the word count field of the transmit command word.

If $\overline{\text{ILLEGAL}}$ is sampled low, the Message Error bit will be set in the SSRT Mark3's status word. No data words will be transmitted following transmission of the status word to an illegalized transmit command. A low on the $\overline{\text{BUSY}}$ input will set the busy bit in the Status Word; in this instance, only the status word will be transmitted, with no data words.

RECEIVE COMMAND (BC-TO-RT TRANSFER)

In non-burst mode, a DMA handshake will be initiated for each data word received from the 1553 data bus. If successful, the

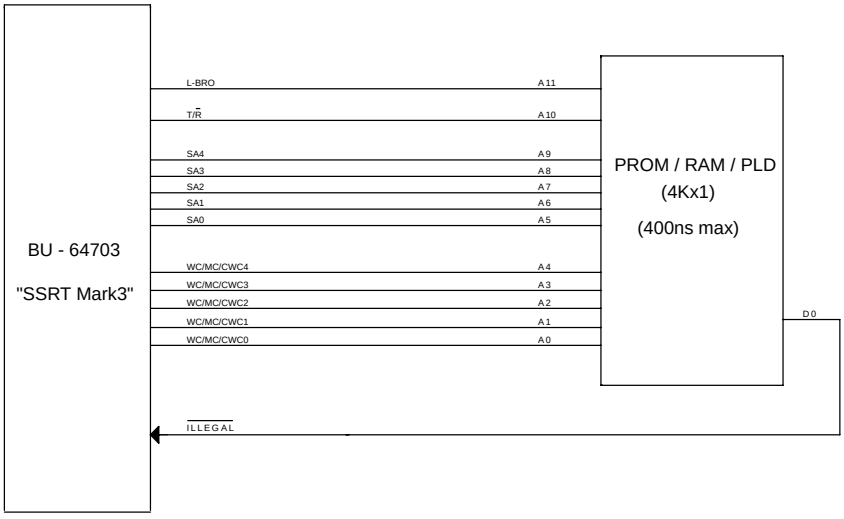


FIGURE 2. SSRT Mark3 ILLEGALIZATION

respective handshake will be followed by a corresponding write cycle. A handshake timeout will not terminate transfer attempts for the remaining data words, error flagging or Status Word transmission. After the reception of a valid non-mode code receive Command Word followed by the correct number of valid Data Words and assuming that all words are successfully transferred to the subsystem, a negative pulse will be asserted on the Good Block Received ($\overline{GBR}$) output. The width of this pulse is two clock cycles.

In burst mode, a DMA handshake will not be initiated until after **all** data words have been received over the 1553 data bus and stored into the SSRT Mark3's internal FIFO. After the handshake has been negotiated, the SSRT Mark3 will burst the contents of the FIFO to the local bus (D0-D15). After the reception of a valid non-mode code receive command word followed by the correct number of valid data words and assuming that all words are successfully transferred to the subsystem, a negative pulse will be asserted on the output Good Block Received ($\overline{GBR}$). The width of this pulse is two clock cycles.

RT-TO-RT TRANSFER ERRORS

For the case where the SSRT Mark3 is the receiving RT of an RT-to-RT transfer, if the transmitting RT does not respond within the specified time period, the SSRT Mark3 will determine that a timeout condition has occurred. The value of the SSRT Mark3's RT-to-RT timeout timer is in the range from 17.5 to 18.5 µs, and is specified from the mid-parity bit crossing of the transmit command word to the mid-sync crossing of the transmitting RT's status word. In the case of an RT-to-RT timeout, the SSRT Mark3 will not respond and the RT-to-RT NO TRANSFER TIMEOUT bit (bit 2) of the SSRT Mark3's BIT Word will be set to logic "1".

Also, if the SSRT Mark3 is the receiving RT for an RT-to-RT transfer, and the T/$\overline{R}$ bit of the second command word is logic "0", **or** the RT address field for the transmit command is the same as for the receive command, or the subaddress for the transmit command is 00000 or 11111, the SSRT Mark3 will not respond, and will set the RT-to-RT SECOND COMMAND ERROR bit (bit 1) of the RT BIT word to logic "1".

RT STATUS, ERROR HANDLING, AND MESSAGE TIMING SIGNALS

Message transfers and transfer errors are indicated by means of the $\overline{INCMD}$, $\overline{HS\_FAIL}$, $\overline{MSG\_ERR}$, and $\overline{RTFAIL}$ error indication outputs. Additional error detection and indication mechanisms include updating of the internal command, RT status and BIT word registers.

The SSRT Mark3 provides a number of timing signals during the processing of 1553 messages. $\overline{INCMD}$ is asserted low when a new command is received. At the end of a message (either valid or invalid), $\overline{INCMD}$ transitions from low to high.

As discussed above, $\overline{HS\_FAIL}$ will be asserted low if the subsystem fails to respond to $\overline{DTREQ}$ within the maximum amount of time (10 µs).

Following the last data word transfer for a valid non-mode code receive message (for either non-burst mode or burst mode), $\overline{GBR}$ will be asserted low for two clock cycles.

$\overline{MSG\_ERR}$ is asserted as a low output level following any detected error in a received message, except for an error in the command word. If an error is detected in a received command word, the rest of the message will be ignored.

If $\overline{MSG\_ERR}$ and/or $\overline{HS\_FAIL}$ have been asserted (low), they will be cleared to logic "1" following receipt of a subsequent valid command word.

LOOPBACK TEST

The SSRT Mark3 performs a loopback self-test at the end of each non-broadcast message processed. The loopback test consists of the following verifications: (1) The received version of every transmitted word is verified for validity (encoding, bit count, parity) and correct sync type; and (2) The received version of the last transmitted word is verified by means of a bit-by-bit comparison to the transmitted version of this word. If there is a transmitter timeout (660.5 µs) and/or if the loopback test fails for one or more transmitted words, the Terminal flag status word bit will be set in response to the next non-broadcast message.

Note that the setting of the Terminal flag status bit following a loop test failure may be disabled by means of the Auto-Config feature; i.e., by setting Auto-Config bit 4 to logic "0".

STATUS WORD

The Broadcast Command Received bit is formulated internally by the SSRT Mark3. The Message Error Status bit will be set if the current command is a Transmit Status Word or Transmit Last Command mode command if there was an error in the data portion of the previous receive message. Message Error will also be set if $\overline{ILLEGAL}$ has been sampled low by the SSRT Mark3 for the current message. $\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{BUSY}$, and $\overline{SSFLAG}$ (Subsystem Flag) will be sampled from their respective Status input pins approximately 2 µs following the mid-parity bit zero crossing of the received Command Word. This time is 400 ns maximum following after the L_BRO, T/$\overline{R}$, SA4-0, and WC/MC/CWC4-0 outputs have been presented valid.

PROTOCOL SELF-TEST

The SSRT Mark3 includes a comprehensive, autonomous off-line self-test of its internal protocol logic. The test includes a comprehensive test of all registers, Manchester encoder and decoders, transmitter failsafe timer, protocol logic, and the internal FIFO.

This test is completed in approximately 32,000 clock cycles. That is, about 1.6 ms with a 20 MHz clock, 2.0 ms at 16 MHz, 2.7 ms at 12 MHz, and 3.2 ms at 10 MHz. While the SSRT Mark3 is performing its off-line self-test, it will ignore (and therefore not respond to) all messages received from the 1553 bus.

Unless disabled by means of the SSRT Mark3's Auto-Config feature, the protocol self-test will be performed following the SSRT

Mark3's power turn-on (i.e., when $\overline{\text{MSTCLR}}$ is released high). If the Auto-Config feature is used and Auto-Config bit 5 is set to logic "0", then a failure of the protocol self-test following power turn-on will result in the SSRT Mark3 not going online. If bit 5 is set to logic "0" and the protocol self-test passes following power turn-on, the SSRT Mark3 will go online.

The protocol self-test will also be performed following receipt of an Initiate self-test mode command from the 1553 bus. If an Initiate self-test mode command is received by the SSRT Mark3, and Auto-Config bit 5 is set to logic "0", then a failure of the protocol self-test following will result in the SSRT Mark3 going offline.

If the protocol self-test fails: (1) the Terminal Flag bit will be set to logic "1" in the SSRT Mark3 status word; (2) bit 8 in the SSRT Mark3's BIT word, BIT Test Fail, will be set to logic "1"; (3) the SSRT Mark3's $\overline{\text{RTFAIL}}$ output will be asserted to logic "0".

AUTO-CONFIGURATION

The SSRT Mark3 includes an auto-configuration feature, which allows various optional features to be enabled or disabled. Auto-configuration may be enabled or disabled by means of the input signal $\overline{\text{AUTO\_CFG}}$. If $\overline{\text{AUTO\_CFG}}$ is connected to logic "1", then the auto-configure option is disabled, and the six configuration parameters revert to their default values.

Note that the default condition for each configuration parameter is enabled (for the MIL-STD-1553A/B protocol selection, -1553**B** is the default).

If $\overline{\text{AUTO\_CFG}}$ is connected to logic "0", then the configuration parameters are transferred over D5-D0 by means of a DMA read data transfer. The transfer occurs during the time that the RTACTIVE **and** $\overline{\text{DTACK}}$ outputs are logic "0", following $\overline{\text{MSTCLR}}$ transitioning from logic "0" to logic "1" and a successful $\overline{\text{DT\_REQ}}$-to-$\overline{\text{DTGRT}}$ handshake.

Note that if $\overline{\text{DTGRT}}$ is hardwired to logic "0", the handshake process is not necessary (i.e., $\overline{\text{DTACK}}$ and RTACTIVE will both be asserted to logic "0" one clock cycle following $\overline{\text{DT\_REQ}}$).

Each of the configuration parameters is **enabled** if the SSRT Mark3 reads a value of logic "1" for the respective data bit.

The auto-configuration parameters are defined by TABLE 2.

The timing signals pertaining to Auto-Configuration mode are illustrated in Figure 12.

CLOCK INPUT

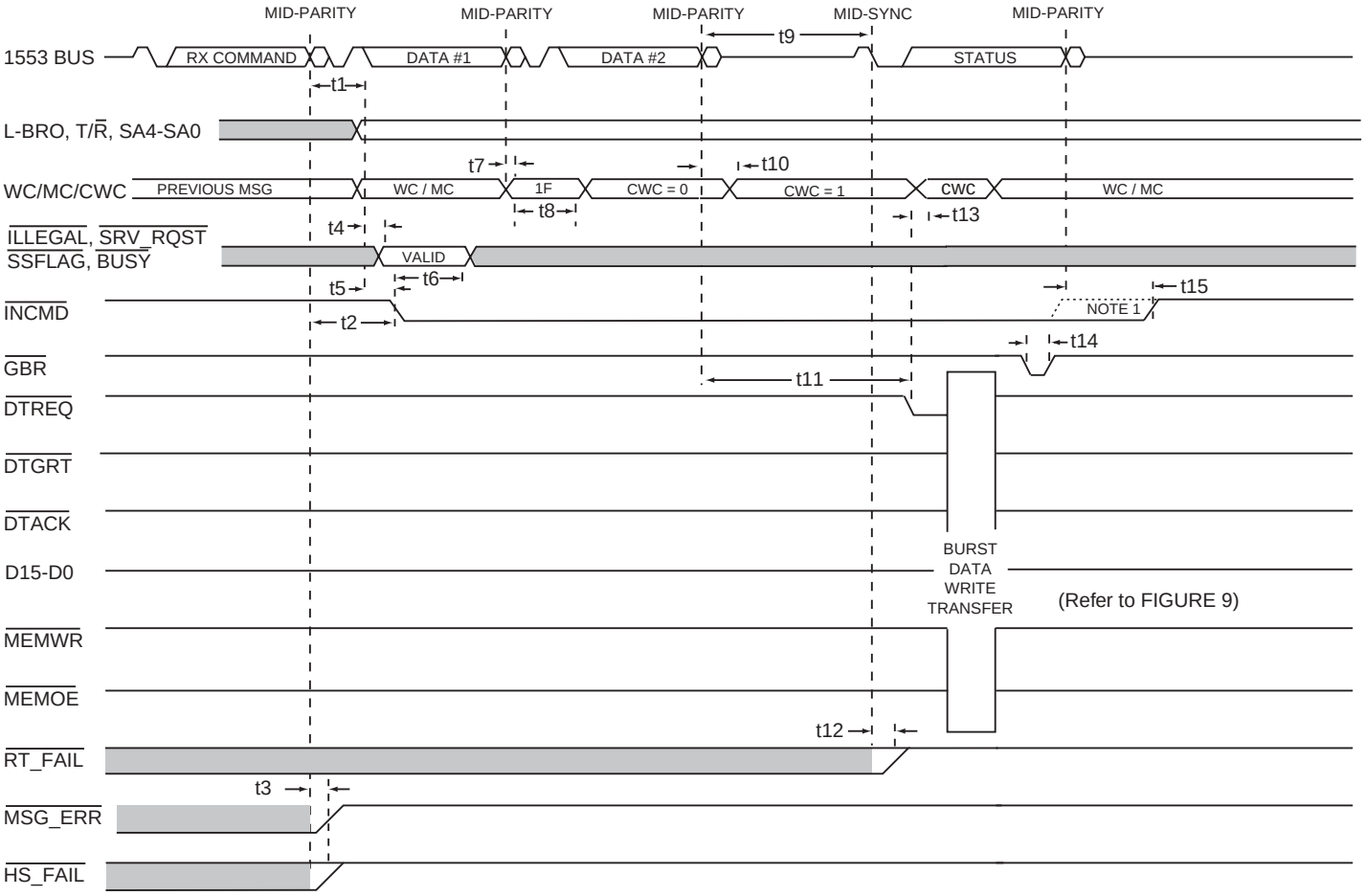
The SSRT Mark3 may be operated from one of four clock frequencies: 10, 12, 16, or 20 MHz. The selected clock frequency must be designated by means of the input signals CLK_SEL_1 and CLK_SEL_0, as shown in TABLE 3.

TABLE 2. AUTO-CONFIGURATION PARAMETERS

BIT	FUNCTION	DESCRIPTION
5	RT GOES ONLINE IF SELF-TEST FAILS	If logic "0", the RT will become enabled only if the self-test passes. If auto-config is not used, or if this bit is logic "1", or if the power-up self-test passes, then the RT will go online following self-test.
4	RTFAIL-to-TERMINAL FLAG AUTO-WRAP	If the loop test fails for a particular message, the Terminal flag bit will be set in the SSRT Mark3's status response for the subsequent non-broadcast message.
3	MIL-STD-1553$\overline{\text{A}}$/B (-B is logic "1", or the default).	In MIL-STD-1553B mode, subaddress 31 is a mode code subaddress, and mode codes are implemented in full accordance with MIL-STD-1553B. In MIL-STD-1553A mode, subaddress 31 is a non-mode code subaddress, and no data words are transmitted or anticipated to be received for mode code messages.
2	SUBADDRESS 30 WRAPAROUND	Subaddress 30 wraparound is enabled. That is, the data words for a receive message to subaddress 30 are stored in the internal FIFO, and not transferred to the external system. For a subsequent transmit message to subaddress 30, the transmitted data words are read from the internal FIFO, rather than from the external system.
1	BURST MODE	Enables burst mode (using the internal FIFO) for received data words. In burst mode, for a receive message, all data words are transferred to the external system in a contiguous burst following reception of the last data word.
0	POWER-UP SELF-TEST ENABLE	If enabled, the SSRT Mark3 will perform self-test following the rising edge of $\overline{\text{MSTCLR}}$.

TABLE 3. CLOCK FREQUENCY SELECTION

CLK_SEL_1	CLK_SEL_0	CLOCK FREQUENCY
0	0	10 MHz
0	1	20 MHz
1	0	12 MHz
1	1	16 MHz



RT RECEIVE COMMAND (BURST MODE)

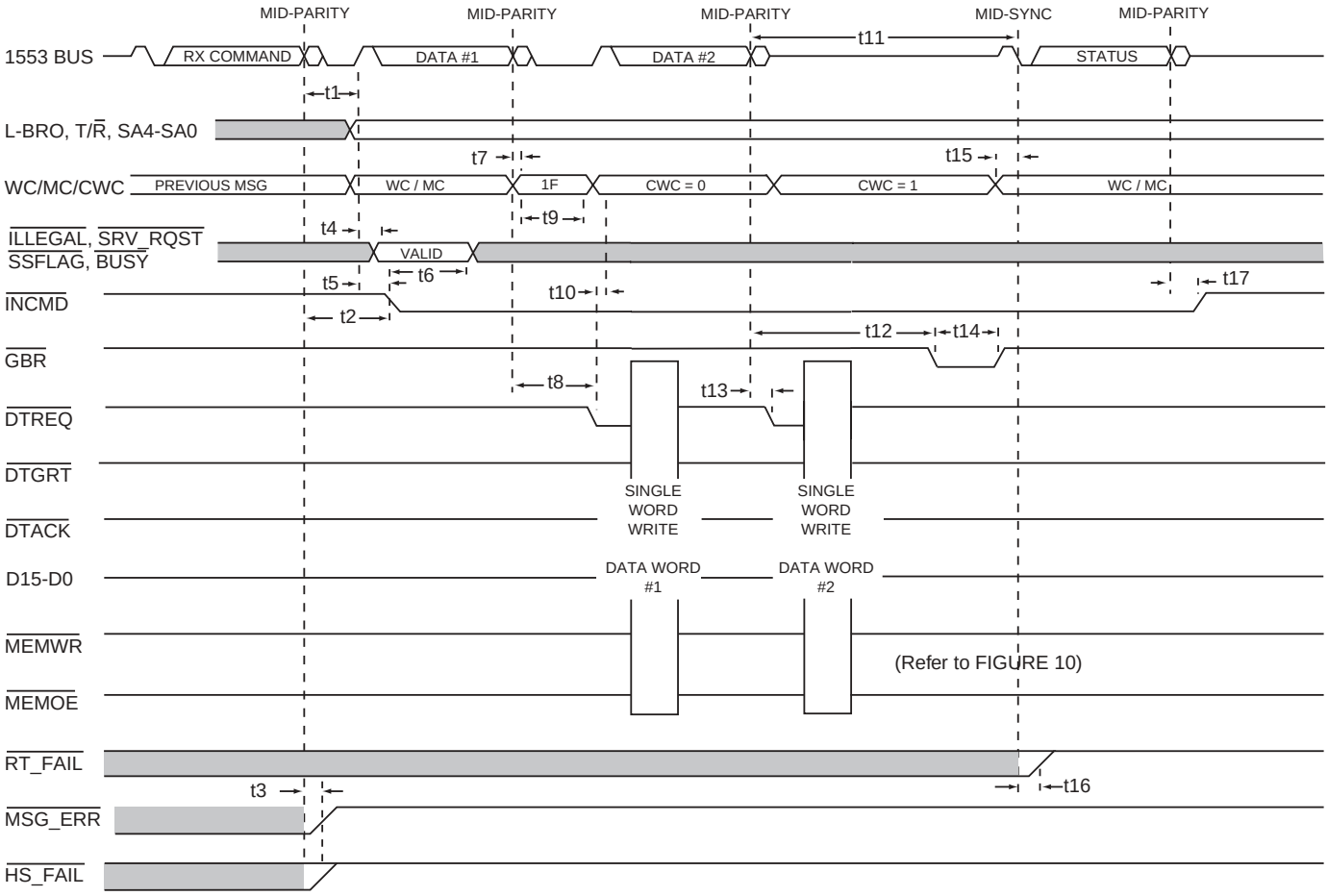
NOTE 1 : If the RX message is a Broadcast message then the rising edge of $\overline{\text{INCMD}}$ is referenced from the rising edge of $\overline{\text{GBR}}$.

FIGURE 3. RT RECEIVE COMMAND (BURST MODE) TIMING

TABLE FOR FIGURE 3. RT RECEIVE COMMAND TIMING (BURST MODE)						
REF	DESCRIPTION	CLOCK FREQUENCY	RESPONSE TIME			UNITS
			MIN	TYP	MAX	
t1	Mid-parity crossing of received command word delay to SA4-SA0, L-BRO, T/$\overline{R}$ Bit, and WC/MC valid	ALL		1.5		µs
t2	Mid-parity crossing of received command word delay to falling edge of $\overline{INCMD}$	ALL		2		µs
t3	Mid-parity crossing of received command word delay to $\overline{MSG\_ERR}$ and $\overline{HS\_FAIL}$ rising	ALL		1.5		µs
t4	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ input access time from SA4-SA0, L-BRO, T/$\overline{R}$, and CWC/MC valid	ALL			400	ns
t5	L_BRO, T/$\overline{R}$, SA4-0, and WC/MC4-0 valid prior to $\overline{INCMD}$ low.	ALL	500			ns
t6	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ hold time following falling edge of $\overline{INCMD}$	ALL	300			ns
t7	Mid-parity crossing of first data word to WC/CWC valid data of 1Fh	ALL		1		µs
t8	Duration of WC/CWC data value of 1Fh	ALL		200		ns
t9	RT Response time.	ALL	4	6.5	7	µs
t10	CWC transition to next word following mid-parity of subsequent received data words.	ALL		1		µs
t11	Mid-parity crossing of last data word to $\overline{DTREQ}$ falling edge (requesting data word burst write transfer)	ALL	4	4.5	5.25	µs
t12	Mid-Sync crossing of Status response to $\overline{RT\_FAIL}$ rising	ALL		1.5		µs
t13	CWC valid following falling edge of $\overline{DTREQ}$	ALL			30	ns
t14	$\overline{GBR}$ pulse width (see Note 1)	20 MHz		100		ns
		16 MHz		125		ns
		12 MHz		167		ns
		10 MHz		200		ns
t15	Mid-parity crossing of status word to $\overline{INCMD}$ rising	ALL		3		µs

NOTE:

(1) If the RX message is a Broadcast message then the rising edge of $\overline{INCMD}$ is referenced from the rising edge of $\overline{GBR}$.



RT RECEIVE COMMAND (NON-BURST MODE)

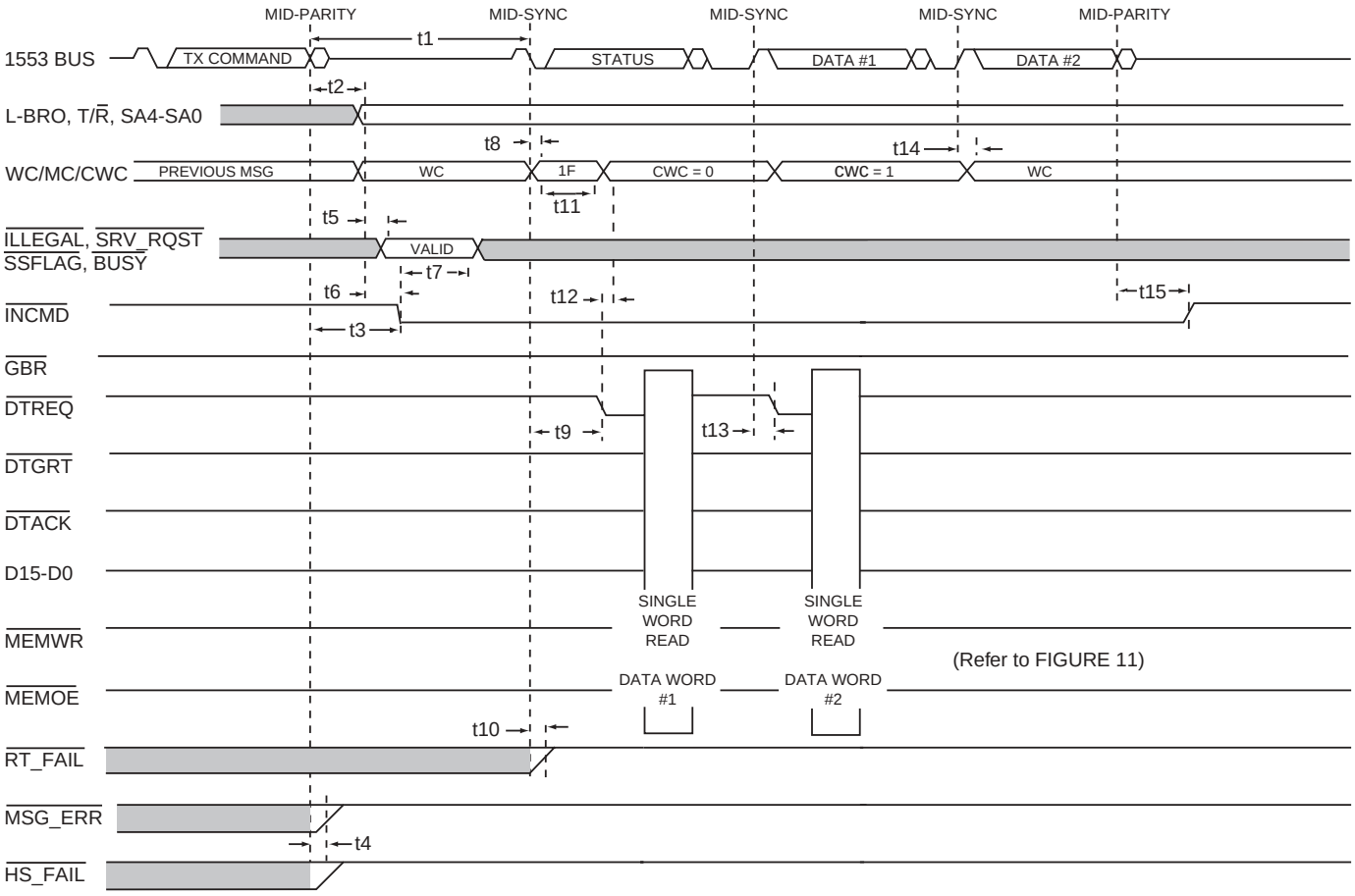
FIGURE 4. RT RECEIVE COMMAND (NON-BURST MODE) TIMING

TABLE FOR FIGURE 4. RT RECEIVE COMMAND TIMING (NON-BURST MODE)						
REF	DESCRIPTION	CLOCK FREQUENCY	RESPONSE TIME			UNITS
			MIN	TYP	MAX	
t1	Mid-parity crossing of received command word delay to SA4-SA0, L-BRO, T/$\overline{R}$ Bit, and WC/MC valid	ALL		1.5		µs
t2	Mid-parity crossing of received command word delay to falling edge of $\overline{INCMD}$	ALL		2		µs
t3	Mid-parity crossing of received command word delay to $\overline{MSG\_ERR}$ and HS_FAIL rising	ALL		1.5		µs
t4	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ input access time from SA4-SA0, L-BRO, T/$\overline{R}$, and CWC/MC valid	ALL			400	ns
t5	RT Sub-Address, L-BRO, and T/$\overline{R}$ Bit setup time prior to $\overline{INCMD}$ low	ALL	500			ns
t6	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ valid time following falling edge of $\overline{INCMD}$	ALL	300			ns
t7	Mid-parity crossing to WC/CWC value of 1Fh	ALL		1		µs
t8	Mid-parity crossing of first data word to $\overline{DTREQ}$ falling edge	20 MHz		1.2		µs
		16 MHz		1.25		µs
		12 MHz		1.33		µs
		10 MHz		1.4		µs
t9	WC/CWC data value of 1Fh held	20 MHz		200		ns
		16 MHz		250		ns
		12 MHz		333		ns
		10 MHz		400		ns
t10	CWC valid following falling edge of $\overline{DTREQ}$	ALL			30	ns
t11	RT Response time.	ALL	4	6.5	7	µs
t12	Delay from following mid-parity of last received data word to $\overline{GBR}$ low. (see Notes 1, 2)	ALL	4			µs
t13	Mid-parity crossing of all data words, except first data word, to $\overline{DTREQ}$ falling edge	ALL		1		µs
t14	$\overline{GBR}$ pulse width	20 MHz		100		ns
		16 MHz		125		ns
		12 MHz		167		ns
		10 MHz		200		ns
t15	CWC transition to WC prior to Mid-Sync crossing of Status response.	20 MHz		75		ns
		16 MHz		94		ns
		12 MHz		125		ns
		10 MHz		150		ns
t16	Mid-Sync crossing of status response to $\overline{RT\_FAIL}$ rising	ALL		1.5		µs
t17	Mid-parity crossing of status word to $\overline{INCMD}$ rising	ALL		3.0		µs

NOTES:

(1) Assumes that $\overline{DTGRT}$ is tied to logic "0". If $\overline{DTGRT}$ is not connected to logic "0", the minimum time to drive $\overline{GBR}$ active low will increase by the amount of the $\overline{DTGRT}$ (low) - to - $\overline{DTGRT}$ (low) delay.

(2) The transceiver delays are measured at a range of 150ns to 450ns for the receiver and 100ns to 250ns for the transmitter.



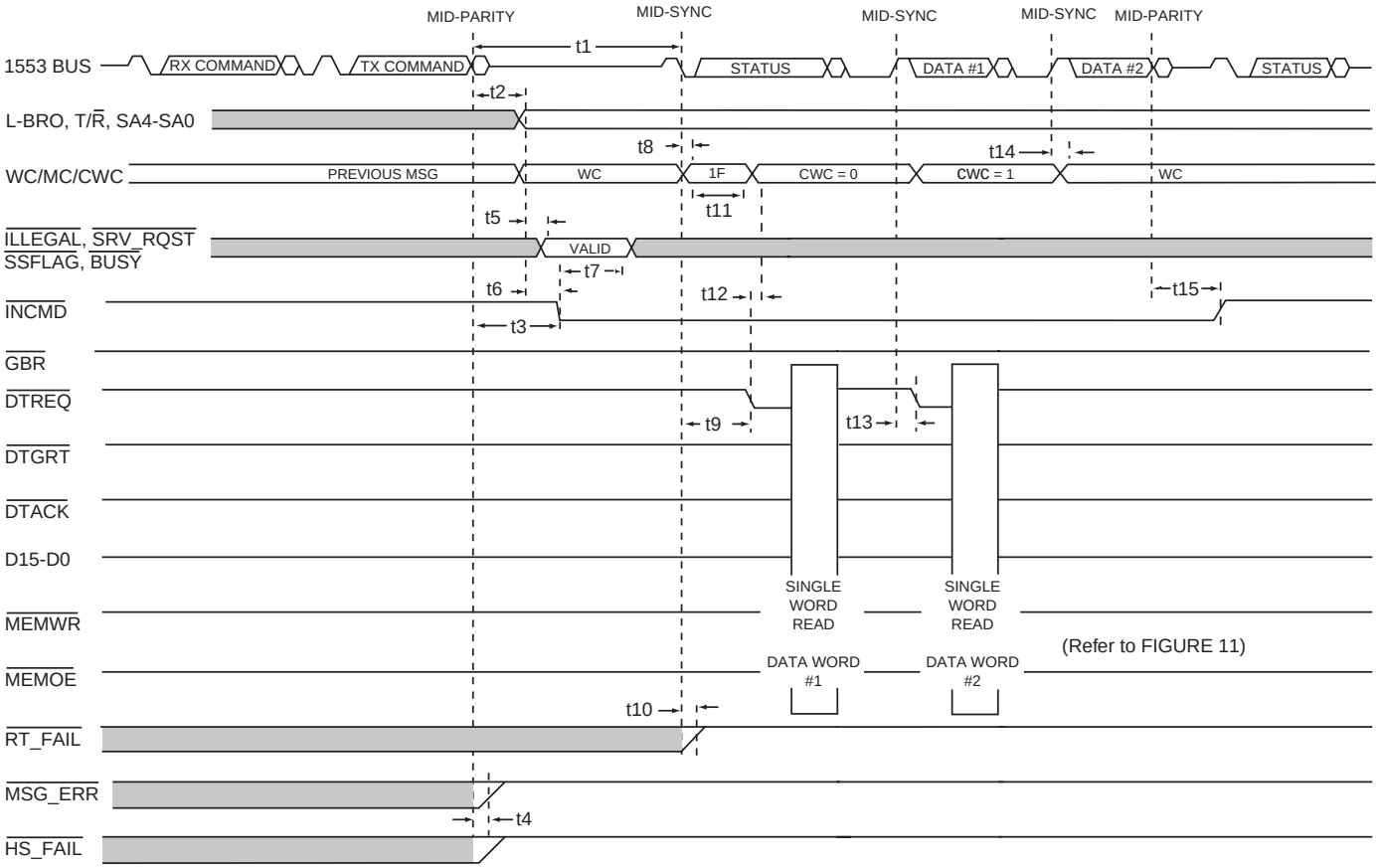
RT TRANSMIT COMMAND

FIGURE 5. RT TRANSMIT COMMAND TIMING

TABLE FOR FIGURE 5. RT TRANSMIT COMMAND TIMING						
REF	DESCRIPTION	CLOCK FREQUENCY	VALUE			UNITS
			MIN	TYP	MAX	
t1	RT Response time.	ALL	4	6.5	7	µs
t2	Mid-parity crossing of received command word delay to L-BRO, T/$\overline{R}$ Bit, SA4-SA0, and WC/MC valid	ALL		1.5		µs
t3	Mid-parity crossing of received command word delay to falling edge of $\overline{INCMD}$	ALL		2		µs
t4	Mid-Parity crossing of receive command word delay to $\overline{MSG\_ERR}$ and $\overline{HS\_FAIL}$ rising	ALL		1.5		µs
t5	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ input access time from SA4-SA0, L-BRO, T/$\overline{R}$ Bit, and CWC/MC valid	ALL			400	ns
t6	L-BRO, T/$\overline{R}$, SA4-0, and WC/MC4-0 setup time prior to $\overline{INCMD}$ low	ALL	500			ns
t7	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ hold time following falling edge of $\overline{INCMD}$	ALL	300			ns
t8	Mid-Sync crossing of status word to WC/CWC valid data of 1Fh	ALL		6.5		µs
t9	Mid-Sync crossing of status word to $\overline{DTREQ}$ falling edge	20 MHz		6.75		µs
		16 MHz		6.81		µs
		12 MHz		6.92		µs
		10 MHz		7		µs
t10	Mid-Sync crossing of Status response to $\overline{RT\_FAIL}$ rising (see Note 1)	ALL		1.5		µs
t11	Duration of WC/CWC value of 1Fh	20 MHz		200		ns
		16 MHz		250		ns
		12 MHz		333		ns
		10 MHz		400		ns
t12	CWC valid following falling edge of $\overline{DTREQ}$	ALL			30	ns
t13	Mid-Sync crossing of received data word to $\overline{DTREQ}$ falling edge	20 MHz		1.75		µs
		16 MHz		1.81		µs
		12 MHz		1.92		µs
		10 MHz		2		µs
t14	Mid-Sync crossing of last received data word for CWC to transition to WC	20 MHz		1.55		µs
		16 MHz		1.56		µs
		12 MHz		1.59		µs
		10 MHz		1.6		µs
t15	Mid-Parity crossing of status word to $\overline{INCMD}$ rising	ALL		3		µs

NOTE:

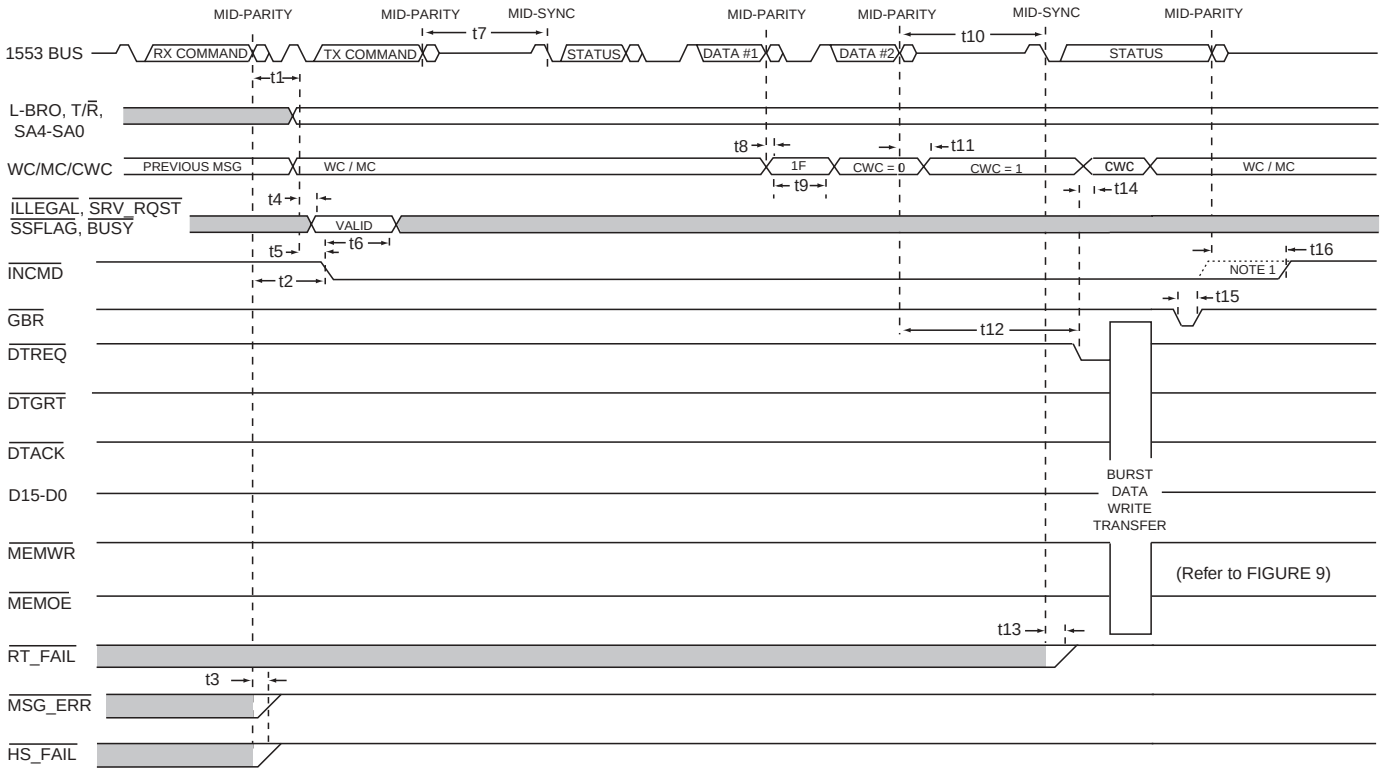
(1) Assuming that $\overline{RTFAIL}$ was previously low.



RT - RT TRANSMIT COMMAND

FIGURE 6. RT - RT TRANSMIT TIMING

TABLE FOR FIGURE 6. RT-RT TRANSMIT COMMAND TIMING						
REF	DESCRIPTION	CLOCK FREQUENCY	VALUE			UNITS
			MIN	TYP	MAX	
t1	RT - RT response timeout for transmitting RT.	ALL	17.5	18.5	19.5	µs
t2	Mid-parity crossing of received command word delay to L-BRO, T/$\overline{R}$ Bit, SA4-SA0, and WC/MC valid	ALL		1.5		µs
t3	Mid-parity crossing of received command word delay to falling edge of $\overline{INCMD}$	ALL		2		µs
t4	Mid-Parity crossing of received command word delay to $\overline{MSG\_ERR}$ and $\overline{HS\_FAIL}$ rising	ALL		1.5		µs
t5	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ input access time from SA4-SA0, L-BRO, T/$\overline{R}$, and CWC/MC valid	ALL			400	ns
t6	L-BRO, T/$\overline{R}$, SA4-0, and WC/MC4-0 setup time prior to $\overline{INCMD}$ low	ALL	500			ns
t7	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ hold time following falling edge of $\overline{INCMD}$	ALL	300			ns
t8	Mid-Sync crossing of status word to WC/CWC valid data of 1Fh	ALL		6.5		µs
t9	Mid-Sync crossing of status word to $\overline{DTREQ}$ falling edge	20 MHz		6.75		µs
		16 MHz		6.81		µs
		12 MHz		6.92		µs
		10 MHz		7		µs
t10	Mid-Sync crossing of Status response to $\overline{RT\_FAIL}$ rising	ALL		1.5		µs
t11	Duration of WC/CWC value of 1Fh	20 MHz		200		ns
		16 MHz		250		ns
		12 MHz		333		ns
		10 MHz		400		ns
t12	CWC valid following falling edge of $\overline{DTREQ}$	ALL			30	ns
t13	Mid-Sync crossing of received data word to $\overline{DTREQ}$ falling edge	20 MHz		1.75		µs
		16 MHz		1.81		µs
		12 MHz		1.92		µs
		10 MHz		2		µs
t14	Mid-Sync crossing of last received data word for CWC to transition to WC	20 MHz		1.55		µs
		16 MHz		1.56		µs
		12 MHz		1.59		µs
		10 MHz		1.6		µs
t15	Mid-Parity crossing of status word to $\overline{INCMD}$ rising	ALL		3		µs



RT - RT RECEIVE COMMAND (BURST MODE)

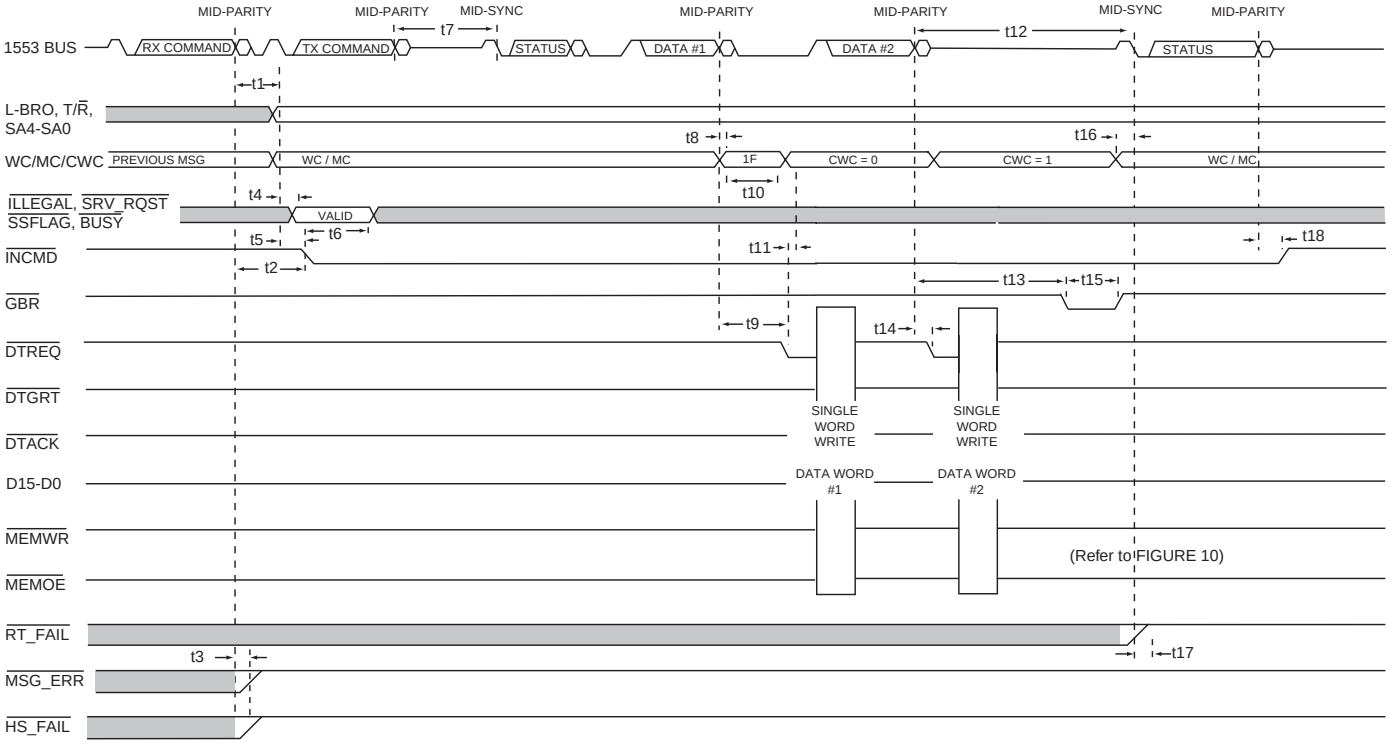
NOTE 1 : If the RX message is a Broadcast message then the rising edge of $\overline{\text{INCMD}}$ is referenced from the rising edge of $\overline{\text{GBR}}$.

FIGURE 7. RT - RT RECEIVE (BURST-MODE) TIMING

TABLE FOR FIGURE 7. RT-RT RECEIVE COMMAND TIMING (BURST MODE)						
REF	DESCRIPTION	CLOCK FREQUENCY	RESPONSE TIME			UNITS
			MIN	TYP	MAX	
t1	Mid-parity crossing of received command word delay to SA4-SA0, L-BRO, T/$\overline{R}$ Bit, and WC/MC valid	ALL		1.5		µs
t2	Mid-parity crossing of received command word delay to falling edge of $\overline{INCMD}$	ALL		2		µs
t3	Mid-parity crossing of received command word delay to $\overline{MSG\_ERR}$ and $\overline{HS\_FAIL}$ rising	ALL		1.5		µs
t4	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ input access time from SA4-SA0, L-BRO, T/$\overline{R}$, and CWC/MC valid	ALL			400	ns
t5	L_BRO, T/$\overline{R}$, SA4-0, and WC/MC4-0 valid prior to $\overline{INCMD}$ low.	ALL	500			ns
t6	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ hold time following falling edge of $\overline{INCMD}$	ALL	300			ns
t7	RT - RT response timeout for transmitting RT.	ALL	17.5	18.5	19.5	µs
t8	Mid-parity crossing of first data word to WC/CWC valid data of 1Fh	ALL		1		µs
t9	Duration of WC/CWC data value of 1Fh	ALL		200		ns
t10	RT Response time.	ALL	4	6.5	7	µs
t11	CWC transition to next word following mid-parity of subsequent received data words.	ALL		1		µs
t12	Mid-parity crossing of last data word to $\overline{DTREQ}$ falling edge (requesting data word burst write transfer)	ALL	4	4.5	5.25	µs
t13	Mid-Sync crossing of Status response to $\overline{RT\_FAIL}$ rising	ALL		1.5		µs
t14	CWC valid following falling edge of $\overline{DTREQ}$	ALL			30	ns
t15	$\overline{GBR}$ pulse width (see Note 1)	20 MHz		100		ns
		16 MHz		125		ns
		12 MHz		167		ns
		10 MHz		200		ns
t16	Mid-parity crossing of status word to $\overline{INCMD}$ rising	ALL		3		µs

NOTE:

(1) If the RX message is a Broadcast message then the rising edge of $\overline{INCMD}$ is referenced from the rising edge of $\overline{GBR}$.



RT - RT RECEIVE COMMAND (NON-BURST MODE)

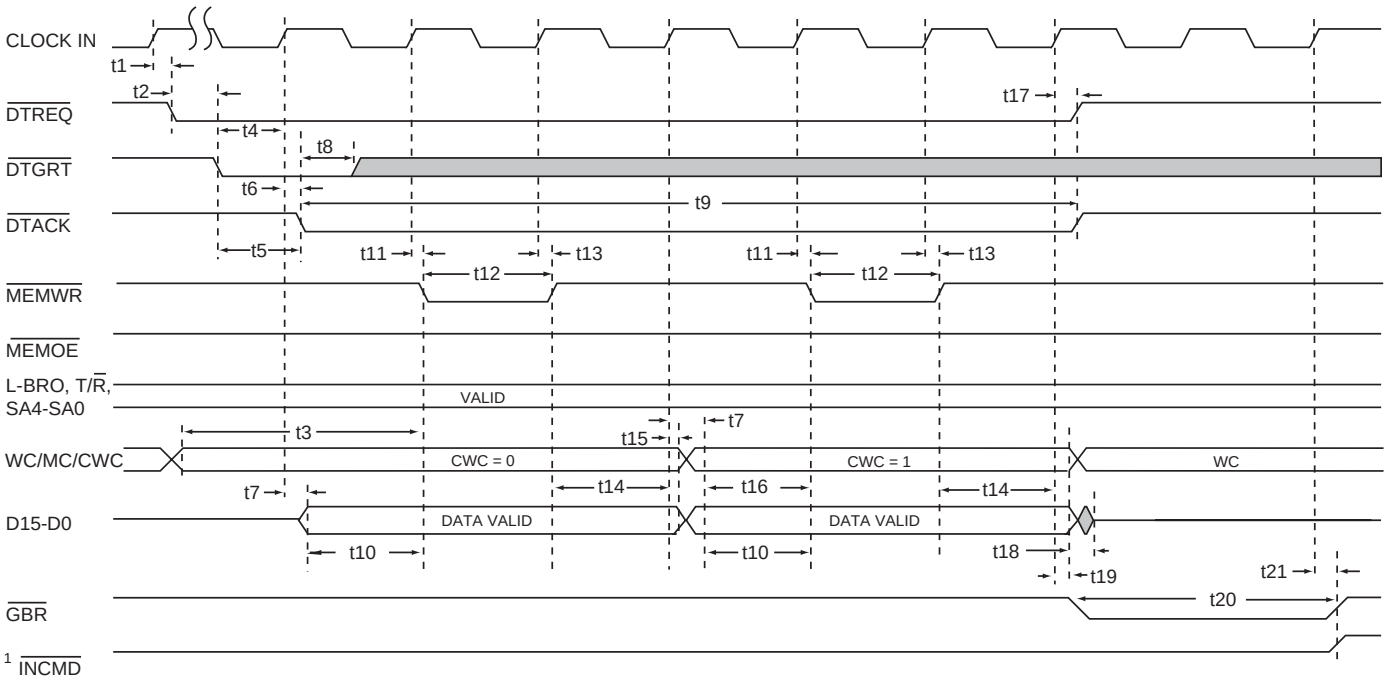
FIGURE 8. RT - RT RECEIVE (NON-BURST-MODE) TIMING

TABLE FOR FIGURE 8. RT-RT RECEIVE COMMAND TIMING (NON-BURST MODE)						
REF	DESCRIPTION	CLOCK FREQUENCY	RESPONSE TIME			UNITS
			MIN	TYP	MAX	
t1	Mid-parity crossing of received command word delay to SA4-SA0, L-BRO, T/$\overline{R}$ Bit, and WC/MC valid	ALL		1.5		µs
t2	Mid-parity crossing of received command word delay to falling edge of $\overline{INCMD}$	ALL		2		µs
t3	Mid-parity crossing of receive command word delay to $\overline{MSG\_ERR}$ and $\overline{HS\_FAIL}$ rising	ALL		1.5		µs
t4	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ input access time from SA4-SA0, L-BRO, T/$\overline{R}$, and CWC/MC valid	ALL			400	ns
t5	RT Sub-Address, L-BRO, and T/$\overline{R}$ Bit setup time prior to $\overline{INCMD}$ low	ALL	500			ns
t6	$\overline{ILLEGAL}$, $\overline{SRV\_RQST}$, $\overline{SSFLAG}$, $\overline{BUSY}$ valid time following falling edge of $\overline{INCMD}$	ALL	300			ns
t7	RT - RT response timeout for transmitting RT.	ALL	17.5	18.5	19.5	µs
t8	Mid-parity crossing to WC/CWC value of 1Fh	ALL		1		µs
t9	Mid-parity crossing of first data word to $\overline{DTREQ}$ falling edge	20 MHz		1.2		µs
		16 MHz		1.25		µs
		12 MHz		1.33		µs
		10 MHz		1.4		µs
t10	WC/CWC data value of 1Fh held	20 MHz		200		ns
		16 MHz		250		ns
		12 MHz		333		ns
		10 MHz		400		ns
t11	CWC valid following falling edge of $\overline{DTREQ}$	ALL			30	ns
t12	RT Response time.	ALL	4	6.5	7	µs
t13	Delay from following mid-parity of last received data word to $\overline{GBR}$ low. (see Notes 1, 2)	ALL	4			µs
t14	Mid-parity crossing of all data words, except first data word, to $\overline{DTREQ}$ falling edge	ALL		1		µs
t15	$\overline{GBR}$ pulse width	20 MHz		100		ns
		16 MHz		125		ns
		12 MHz		167		ns
		10 MHz		200		ns
t16	CWC transition to WC prior to Mid-Sync crossing of Status response.	20 MHz		75		ns
		16 MHz		94		ns
		12 MHz		125		ns
		10 MHz		150		ns
t17	Mid-Sync crossing of status response to $\overline{RT\_FAIL}$ rising	ALL		1.5		µs
t18	Mid-parity crossing of status word to $\overline{INCMD}$ rising	ALL		3.0		µs

NOTES:

(1) Assumes that $\overline{DTGRT}$ is tied to logic "0". If $\overline{DTGRT}$ is not connected to logic "0", the minimum time to drive $\overline{GBR}$ active low will increase by the amount of the $\overline{DTGRT}$ (low) - to - $\overline{DTGRT}$ (low) delay.

(2) The transceiver delays are measured at a range of 150ns to 450ns for the receiver and 100ns to 250ns for the transmitter.



DMA WRITE - BURST MODE
(SHOWN FOR TWO DATA WORDS)

1 $\overline{\text{INCMD}}$ rising edge is shown for the case of a RX Broadcast command message.
For the non-Broadcast case, $\overline{\text{INCMD}}$ rising edge is after the Mid-Parity crossing of the RT STATUS response.

FIGURE 9. DMA WRITE TRANSFER (BURST-MODE) TIMING

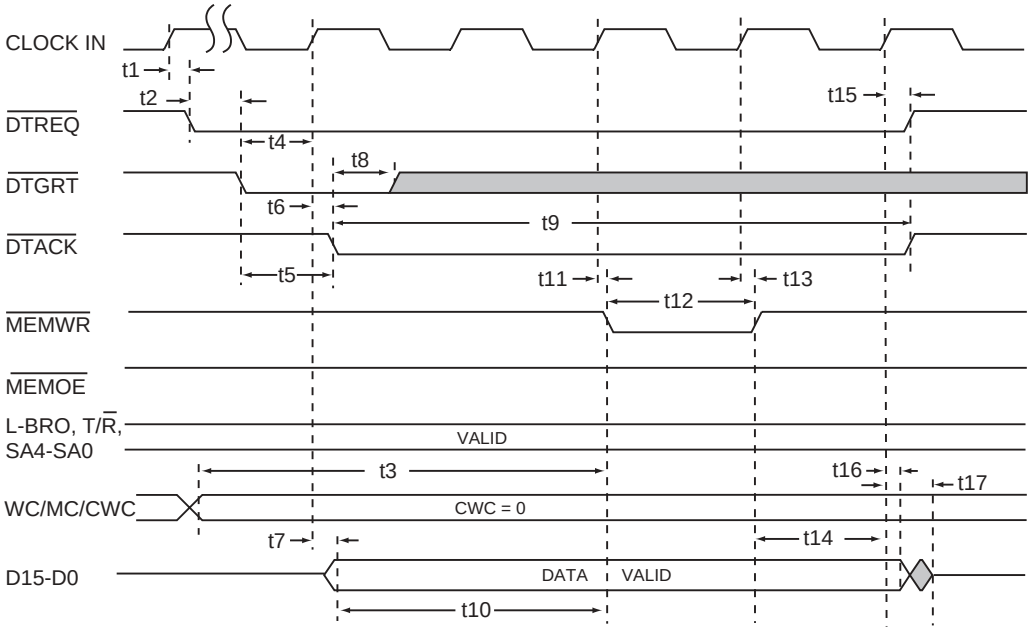
TABLE FOR FIGURE 9. SSRT Mark3 DMA WRITE (BURST MODE) TIMING						
REF	DESCRIPTION	CLOCK FREQUENCY	VALUE @3.3 VOLTS			UNITS
			MIN	TYP	MAX	
t1	CLOCK IN rising to $\overline{\text{DTREQ}}$ low	ALL			40	ns
t2	$\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low	ALL			10	µs
t3	CWC setup time prior to $\overline{\text{MEMWR}}$ falling for first word of burst transfer (see Note 1)	20 MHz	60			ns
		16 MHz	85			ns
		12 MHz	127			ns
		10 MHz	160			ns
t4	$\overline{\text{DTGRT}}$ low setup prior to CLOCK IN rising edge	ALL	15			ns
t5	$\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low	20 MHz			105	ns
		16 MHz			118	ns
		12 MHz			138	ns
		10 MHz			155	ns
t6	CLOCK IN rising to $\overline{\text{DTACK}}$ low	ALL			40	ns
t7	Data output valid following CLOCK IN	ALL			40	ns
t8	$\overline{\text{DTGRT}}$ hold time following $\overline{\text{DTACK}}$ falling	ALL			30	ns
t9	$\overline{\text{DTACK}}$ low pulse width (based on a two data word transfer) (see Note 2)	20 MHz	290	300		ns
		16 MHz	365	375		ns
		12 MHz	490	500		ns
		10 MHz	590	600		ns
t10	Data output setup time prior to $\overline{\text{MEMWR}}$ low	20 MHz	10			ns
		16 MHz	22			ns
		12 MHz	43			ns
		10 MHz	60			ns
t11	CLOCK IN rising to $\overline{\text{MEMWR}}$ low	ALL			40	ns
t12	$\overline{\text{MEMWR}}$ low pulse width	20 MHz	40	50		ns
		16 MHz	52.5	62.5		ns
		12 MHz	73.3	83.3		ns
		10 MHz	90	100		ns
t13	CLOCK IN rising to $\overline{\text{MEMWR}}$ high	ALL			40	ns
t14	Data output and CWC hold time following $\overline{\text{MEMWR}}$ high	20 MHz	10			ns
		16 MHz	23			ns
		12 MHz	43			ns
		10 MHz	60			ns
t15	Data output hold time following CLOCK IN rising	ALL	15			ns
t16	CWC (all but first data word) setup time prior to $\overline{\text{MEMWR}}$ low	20 MHz	10			ns
		16 MHz	23			ns
		12 MHz	43			ns
		10 MHz	60			ns
t17	CLOCK IN rising to $\overline{\text{DTREQ}}$ and $\overline{\text{DTACK}}$ high	ALL			40	ns
t18	Data output signal Tri-State following CLOCK IN rising	ALL			40	ns
t19	CLOCK IN rising to $\overline{\text{GBR}}$ falling edge	ALL			40	ns
t20	$\overline{\text{GBR}}$ low pulse width	20 MHz	90	100		ns
		16 MHz	115	125		ns
		12 MHz	157	167		ns
		10 MHz	190	200		ns
t21	$\overline{\text{INCMD}}$ rising following CLOCK IN rising (see Note 3)	ALL			40	ns

NOTES:

(1) Assumes $\overline{\text{DTGRT}}$ is low at the time that $\overline{\text{DTREQ}}$ is asserted low. If not, then this time will increase by the amount of the $\overline{\text{DTREQ}}$ (low) - to - $\overline{\text{DTGRT}}$ (low) delay.

(2) $\overline{\text{DTACK}}$ pulse width is 3 clock cycles per data word transfer.

(3) Rising edge of $\overline{\text{INCMD}}$ will immediately follow the rising edge of $\overline{\text{GBR}}$ only for a broadcast message. For a non-broadcast message, the rising edge of $\overline{\text{INCMD}}$ will occur after the mid-parity crossing of the RT status response. This additional delay time is approximately 96 clock cycles: 9.6 µs at 10 MHz, 8 µs at 12 MHz, 6.0 µs at 16 MHz, or 4.8 µs at 20 MHz.



NON-BURST DMA WRITE

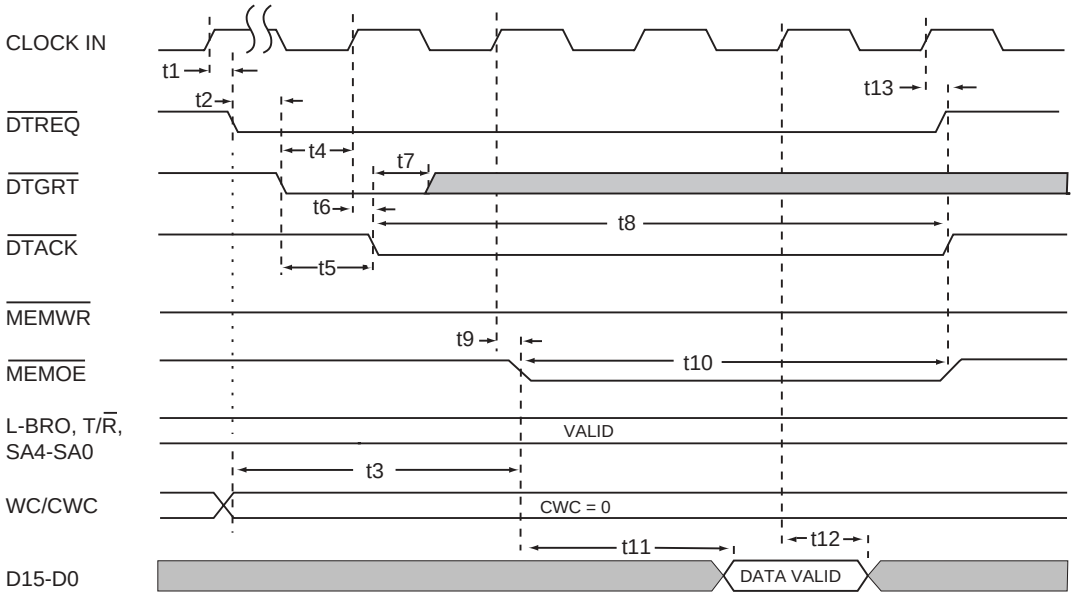
NOTE: With the DTGRT pin tied to GND, the time from DTREQ to DTACK is 1 clock cycle.

FIGURE 10. DMA WRITE TRANSFER (NON-BURST-MODE) TIMING

TABLE FOR FIGURE 10. SSRT Mark3 DMA WRITE TIMING (NON-BURST)						
REF	DESCRIPTION	CLOCK FREQUENCY	VALUE @3.3 VOLTS			UNITS
			MIN	TYP	MAX	
t1	CLOCK IN rising to $\overline{\text{DTREQ}}$ low	ALL			40	ns
t2	$\overline{\text{DTREQ}}$ (low) - to - $\overline{\text{DTGRT}}$ (low) delay time	ALL			10	µs
t3	CWC setup time prior to $\overline{\text{MEMWR}}$ falling (see Note)	20 MHz	110			ns
		16 MHz	148			ns
		12 MHz	210			ns
		10 MHz	260			ns
t4	$\overline{\text{DTGRT}}$ low setup prior to CLOCK IN rising	ALL	15			ns
t5	$\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low	20 MHz			105	ns
		16 MHz			118	ns
		12 MHz			138	ns
		10 MHz			155	ns
t6	CLOCK IN rising to $\overline{\text{DTACK}}$ low	ALL			40	ns
t7	Data output valid following CLOCK IN rising	ALL			40	ns
t8	$\overline{\text{DTGRT}}$ hold time following $\overline{\text{DTACK}}$ falling	ALL			30	ns
t9	$\overline{\text{DTACK}}$ low pulse width	20 MHz		200		ns
		16 MHz		250		ns
		12 MHz		333		ns
		10 MHz		400		ns
t10	Data output setup time prior to $\overline{\text{MEMWR}}$ low	20 MHz	60			ns
		16 MHz	85			ns
		12 MHz	127			ns
		10 MHz	160			ns
t11	CLOCK IN rising to $\overline{\text{MEMWR}}$ low	ALL			40	ns
t12	$\overline{\text{MEMWR}}$ low pulse width	20 MHz	40	50		ns
		16 MHz	52.5	62.5		ns
		12 MHz	73.3	83.3		ns
		10 MHz	90	100		ns
t13	CLOCK IN rising to $\overline{\text{MEMWR}}$ high	ALL			40	ns
t14	Data output hold time following $\overline{\text{MEMWR}}$ high	20 MHz	10			ns
		16 MHz	23			ns
		12 MHz	43			ns
		10 MHz	60			ns
t15	CLOCK IN rising to $\overline{\text{DTREQ}}$ and $\overline{\text{DTACK}}$ high	ALL			40	ns
t16	Data output hold time following CLOCK IN rising	ALL	15			ns
t17	Data output signal Tri-State following CLOCK IN rising	ALL			40	ns

NOTES:

(1) Assumes that $\overline{\text{DTGRT}}$ is low at the time $\overline{\text{DTREQ}}$ is asserted low. If not, these values can increase by the delay time from $\overline{\text{DTREQ}}$ (low) - to - $\overline{\text{DTGRT}}$ (low).



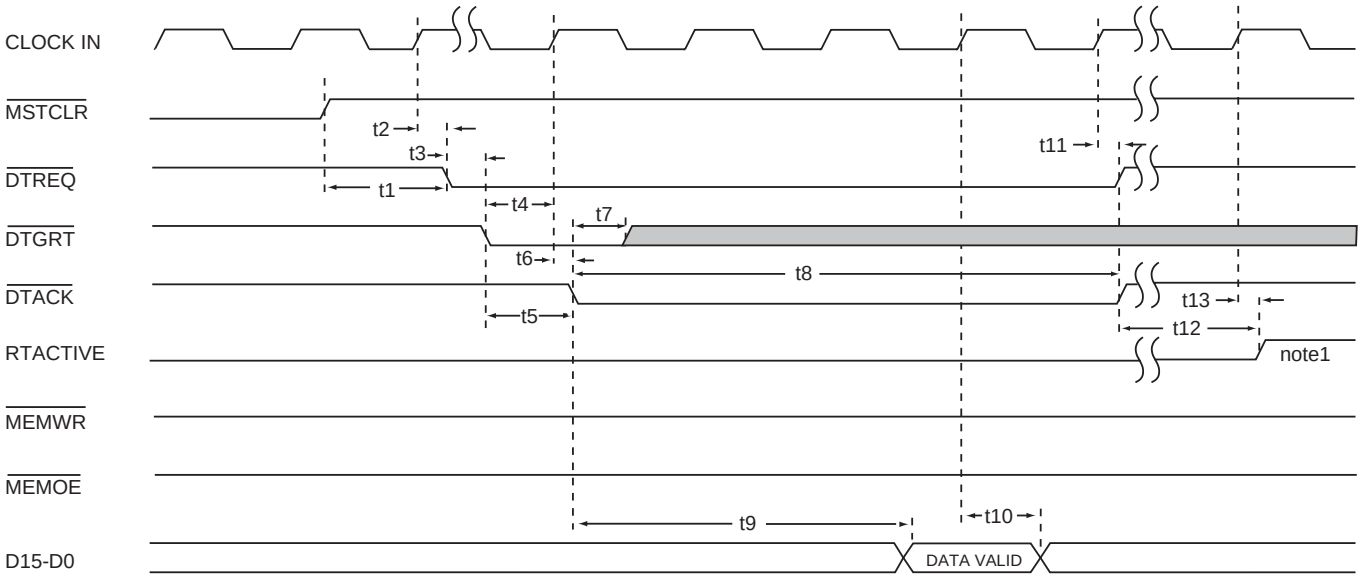
DMA SINGLE WORD READ

FIGURE 11. DMA READ TRANSFER TIMING

TABLE FOR FIGURE 11. SSRT Mark3 DMA READ TIMING						
REF	DESCRIPTION	CLOCK FREQUENCY	VALUE @3.3 VOLTS			UNITS
			MIN	TYP	MAX	
t1	CLOCK IN rising to $\overline{\text{DTREQ}}$ low	ALL			40	ns
t2	$\overline{\text{DTREQ}}$ (low) - to - $\overline{\text{DTGRT}}$ delay time	ALL			10	µs
t3	CWC setup time prior to $\overline{\text{MEMOE}}$ falling	20 MHz	60			ns
		16 MHz	85			ns
		12 MHz	127			ns
		10 MHz	160			ns
t4	$\overline{\text{DTGRT}}$ low setup prior to CLOCK IN rising	ALL			10	ns
t5	$\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low	20 MHz			105	ns
		16 MHz			118	ns
		12 MHz			138	ns
		10 MHz			155	ns
t6	CLOCK IN rising to $\overline{\text{DTACK}}$ low	ALL			40	ns
t7	$\overline{\text{DTGRT}}$ hold time following $\overline{\text{DTACK}}$ falling	ALL			30	ns
t8	$\overline{\text{DTACK}}$ low pulse width	20 MHz		200		ns
		16 MHz		250		ns
		12 MHz		333		ns
		10 MHz		400		ns
t9	CLOCK IN rising to $\overline{\text{MEMOE}}$ low	ALL			40	ns
t10	$\overline{\text{MEMOE}}$ low pulse width	20 MHz		150		ns
		16 MHz		188		ns
		12 MHz		250		ns
		10 MHz		300		ns
t11	Time for input data to become valid following falling edge of $\overline{\text{MEMOE}}$	20 MHz			70	ns
		16 MHz			95	ns
		12 MHz			136	ns
		10 MHz			170	ns
t12	Data input hold time following CLOCK IN rising (see Note)	ALL	30			ns
t13	CLOCK IN rising to $\overline{\text{DTREQ}}$, $\overline{\text{DTACK}}$, and $\overline{\text{MEMOE}}$ high	ALL			40	ns

NOTE:

(1) The SSRT Mark3's data sampling time occurs one clock cycle prior to the rising edge of $\overline{\text{MEMOE}}$.



AUTO-CONFIGURATION - DMA SINGLE WORD READ

Note1: RTACTIVE asserted high 1 clock following $\overline{\text{DTACK}}$ high assuming self-test is not enabled.
When self-test is enabled RTACTIVE is delayed in the amount of 't12'.
See the table reference for details.

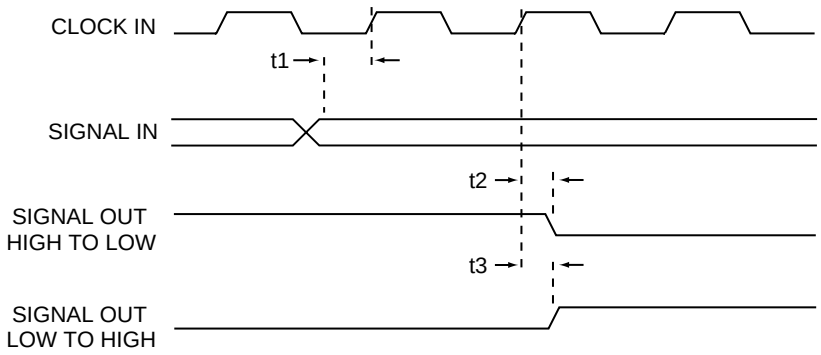
FIGURE 12. AUTO-CONFIGURATION - DMA READ TRANSFER TIMING

TABLE FOR FIGURE 12. AUTO-CONFIGURATION - DMA READ TIMING						
REF	DESCRIPTION	CLOCK FREQUENCY	VALUE @3.3 VOLTS			UNITS
			MIN	TYP	MAX	
t1	$\overline{\text{MSTCLR}}$ high delay to $\overline{\text{DTREQ}}$ low	20 MHz	35	50	65	ns
		16 MHz	47.5	62.5	77.5	ns
		12 MHz	68.3	83.3	98.3	ns
		10 MHz	85	100	115	ns
t2	CLOCK IN rising to $\overline{\text{DTREQ}}$ low	ALL			40	ns
t3	$\overline{\text{DTREQ}}$ (low) - to - $\overline{\text{DTGRT}}$ delay time	ALL			10	µs
t4	$\overline{\text{DTGRT}}$ low setup prior to CLOCK IN rising	ALL			10	ns
t5	$\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low	20 MHz			105	ns
		16 MHz			118	ns
		12 MHz			138	ns
		10 MHz			155	ns
t6	CLOCK IN rising to $\overline{\text{DTACK}}$ low	ALL			40	ns
t7	$\overline{\text{DTGRT}}$ hold time following $\overline{\text{DTACK}}$ falling	ALL			30	ns
t8	$\overline{\text{DTACK}}$ low pulse width	20 MHz	185	200	215	ns
		16 MHz	235	250	265	ns
		12 MHz	318	333	348	ns
		10 MHz	385	400	415	ns
t9	Time for input data to become valid following falling edge of $\overline{\text{DTACK}}$	20 MHz			120	ns
		16 MHz			157	ns
		12 MHz			220	ns
		10 MHz			270	ns
t10	Data input hold time following sampling time (see Note 1)	ALL	30			ns
t11	CLOCK IN rising to $\overline{\text{DTREQ}}$, $\overline{\text{DTACK}}$, and $\overline{\text{MEMOE}}$ high	ALL			40	ns
t12	RTACTIVE high delayed from $\overline{\text{DTACK}}$ high (see Note 2)	20 MHz		1.6		ms
		16 MHz		2.0		ms
		12 MHz		2.7		ms
		10 MHz		3.2		ms
t13	CLOCK IN rising to RTACTIVE high	ALL			40	ns

NOTES:

(1) During Auto-Configuration the SSRT Mark3 samples data three clock cycles following the falling edge of $\overline{\text{DTACK}}$.

(2) If self-test mode is not enabled, then RTACTIVE will go active high 1 clock cycle following the rising edge of $\overline{\text{DTACK}}$.
If self-test is enabled then RTACTIVE will be delayed from going active high in accordance with 't12'.



CLOCK EDGE TO SIGNAL IN / OUT TIMING

FIGURE 13. CLOCK EDGE SIGNAL TIMING

TABLE FOR FIGURE 13. SSRT Mark3 CLOCK EDGE TO SIGNAL IN / OUT VALID TIMING

REF	DESCRIPTION	VALUE @3.3 VOLTS			UNITS
		MIN	TYP	MAX	
t1	SIGNAL INPUT setup time prior to CLOCK IN rising edge	15			ns
t2	CLOCK IN rising edge to SIGNAL OUTPUT driven low (see Note)			40	ns
t3	CLOCK IN rising edge to SIGNAL OUTPUT driven high (see Note)			40	ns

NOTE:

(1) Assumes a 50 pf external load. For loading above 50pf, the validity of output signals is delayed by an additional 0.14 ns/pf typ, 0.28ns/pf max.

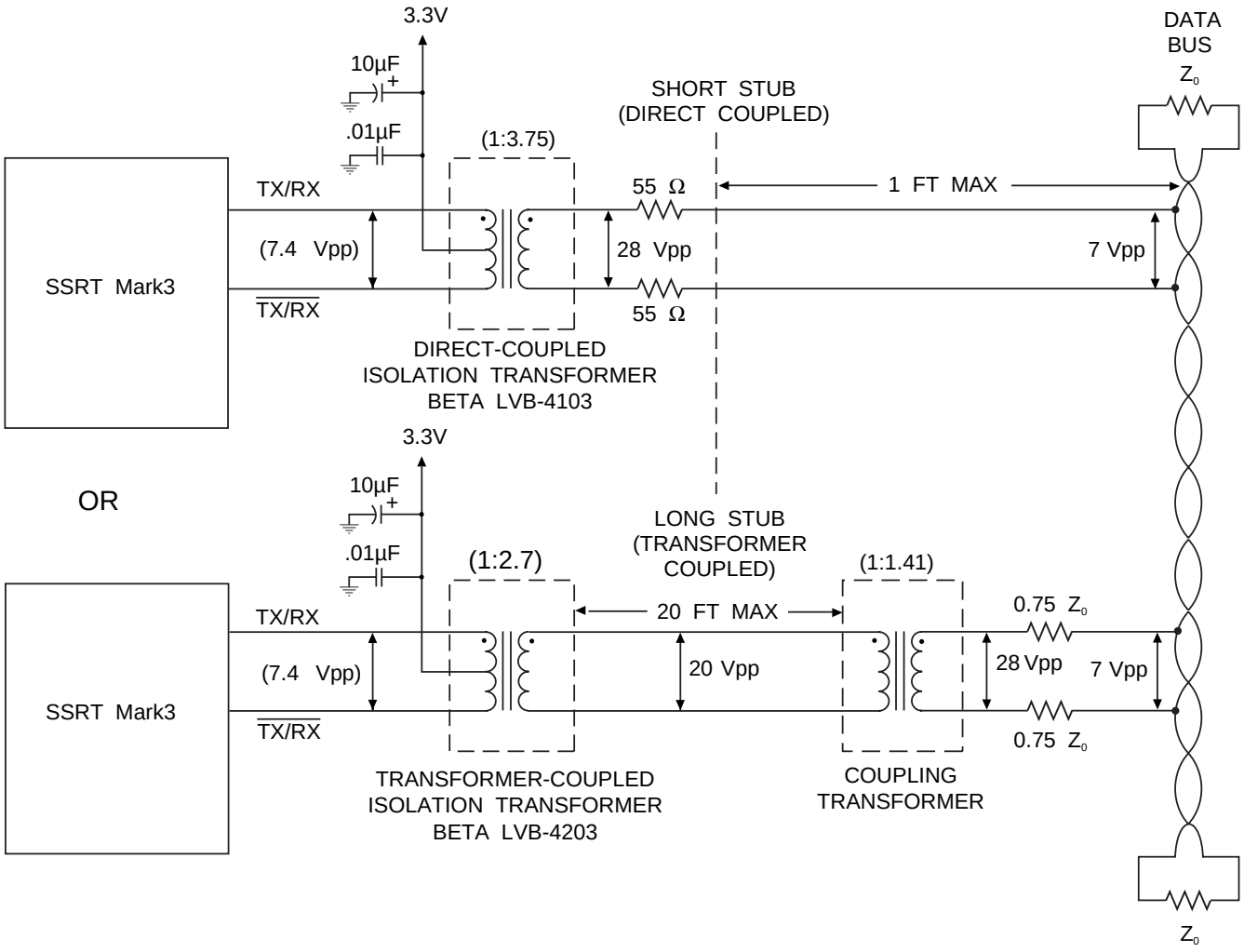
INTERFACE TO MIL-STD-1553 BUS

The SSRT Mark3 is the world's first MIL-STD-1553 terminal powered entirely by 3.3 volts. Unique isolation transformer turns ratios, single output winding transformers and new interconnection methods are required in order to meet mandated MIL-STD-1553 differential voltage levels.

FIGURE 14 illustrates the two possible interface methods between the SSRT Mark3 series and a MIL-STD-1553 bus. Connections for both direct (short stub, 1:3.75) and transformer (long stub, 1:2.7) coupling, as well as nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

The new isolation transformers for the SSRT Mark3 series now contain only one set of output windings. Different isolation transformers are now required for a direct or transformer coupled, MIL-STD-1553 Bus implementation.

The center tap of the primary winding (the side of the transformer that connects to the SSRT Mark3) must be directly connected to the +3.3 volt plane. Additionally a 10uf, low inductance tantalum capacitor and a 0.01uf ceramic capacitor must be mounted as close as possible and with the shortest leads to the center tap of the transformer(s) and the ground plane.



NOTES:

1. Transformer center tap capacitors: use a 10µF tantalum for low inductance, and a 0.01µF ceramic. Both must be mounted as close as possible, and with the shortest leads to the center tap of the transformer(s) and ground.
2. Connect the Mark3 hybrid grounds as directly as possible to the 3.3V ground plane.
3. Z_0 = 70 to 85 Ohms.

FIGURE 14. SSRT Mark3 INTERFACE TO MIL-STD-1553 BUS

PULSE TRANSFORMERS

In selecting isolation transformers to be used with the SSRT Mark3 , there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is a function of the coupling method. For Transformer Coupled applications, it is a maximum of 5.0 µH. For Direct it is a maximum of 10.0 µH, and is measured as follows:

The side of the transformer that connects to the SSRT Mark3 is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding. This inductance must be less than 5.0 µH (Transformer Coupled) and 10.0 µH (Direct Coupled). Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 5.0 µH (Transformer Coupled) and 10.0 µH (Direct Coupled).

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH (Transformer Coupled) and 2.0 µH (Direct Coupled).

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:3.75 direct coupled, and 1:2.7 transformer coupled. TABLE 4 provides a listing of many of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

TABLE 4. BTTC TRANSFORMERS FOR USE WITH SSRT Mark3

TRANSFORMER CONFIGURATION	(BTTC LEGACY PART NO.)	BTTC PART NO.
Single epoxy transformer, through-hole, transformer coupled, 0.625" X 0.630", 0.300" max height, +130° C max	(B-3372)	LVB-4203
Single epoxy transformer, through-hole, direct coupled, 0.625" X 0.630", 0.300" max height, +130° C max	(B-3383)	LVB-4103
Single epoxy transformer, surface mount, transformer coupled, 0.625" X 0.625", 0.130" max height, +85° C max	(B-3389)	LVB-4213
Single epoxy transformer, surface mount, direct coupled, 0.625" X 0.625", 0.130" max height, +85° C max	(B-3390)	LVB-4113
Single epoxy transformer, surface mount, transformer coupled, 0.625" X 0.630", 0.300" max height, +130° C max	(B-3391)	LVB-4223
Single epoxy transformer, surface mount, direct coupled, 0.625" X 0.630", 0.300" max height, +130° C max	(B-3392)	LVB-4123

Notes:
1. SMT (Surface Mount) body package size (a" x b") does not include leads.

The list of approved transformers for use with SSRT Mark3 is constantly being updated. Please contact Beta Transformer Technology Corporation for the latest transformer configuration information.

1553 BUS CONNECTIONS

The isolation transformers should be placed as physically close as possible to the respective TX/RX pins on the SSRT Mark3. In addition, the distance from the isolation transformers to any connectors or cables leaving the board should be as short as possible. In addition to limiting the voltage drops in the analog signal traces when transmitting, reducing the hybrid-to-transformer and transformer-to-connector spacing serves to minimize crosstalk from other signals on the board.

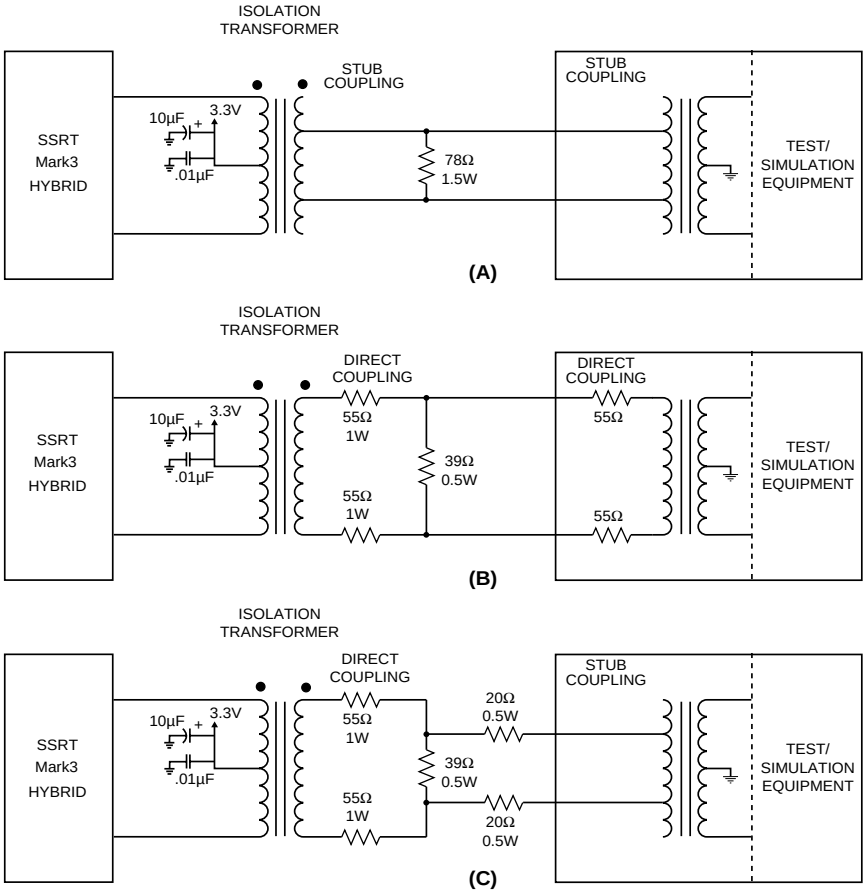
The general practice in connecting the stub side of a transformer (or direct) coupled terminal to an external system connector is to make use of 78 ohm twisted-pair shielded cable. This minimizes impedance discontinuities. The decision of whether to isolate or make connections between the center tap of the isolation transformer's secondary, the stub shield, the bus shield, and/or chassis ground must be made on a system basis, as determined by an analysis of EMI/RFI and lightning considerations.

In most systems, it is specified that the 1553 terminal's input impedance must be measured at the system connector. This is despite the fact that the MIL-STD-1553B requirement is for it to be measured looking directly in from the bus side of the isolation transformer.

The effect of a relatively long stub cable will be to reduce the measured impedance (looking in from the bus). In order to keep the impedance above the required level of 1000 ohms (for transformer-coupled stubs), the length of any cable between the 1553 RT and the system connector should be minimized.

"SIMULATED BUS" (LAB BENCH) INTERCONNECTIONS

For purposes of software development and system integration, it is generally not necessary to integrate the required couplers, terminators, etc., that comprise a complete MIL-STD-1553B bus. In most instances, a simplified electrical configuration will suffice. The three connection methods illustrated in FIGURE 15 allow the SSRT Mark3 to be interfaced over a "simulated bus" to simulation and test equipment. It is important to note that the termination resistors indicated are necessary in order to ensure reliable communications between the SSRT Mark3 and the simulation/test equipment.



(A) TRANSFORMER COUPLED TO TRANSFORMER COUPLED
(B) DIRECT COUPLED TO DIRECT COUPLED
(C) DIRECT COUPLED TO TRANSFORMER COUPLED

FIGURE 15. "SIMULATED BUS" (LAB BENCH) INTERCONNECTIONS

SIMPLE SYSTEM INTERFACE

FIGURE 16 illustrates the capability of the SSRT Mark3 to interface to a system with no host processor in burst mode. In this example, only one set of external latches is needed to buffer the data words written by the SSRT Mark3 to the external system. In burst mode, all received data words are stored in the internal FIFO until the last word is received. At this point, the SSRT Mark3 will transfer the entire contents of the FIFO to the system if the message is validated. In this case, GBR_L will be driven low for two clock cycles following the burst transfer cycle.

If the received message is not valid, the FIFO data will not be transferred to the external system and GBR_L will remain high.

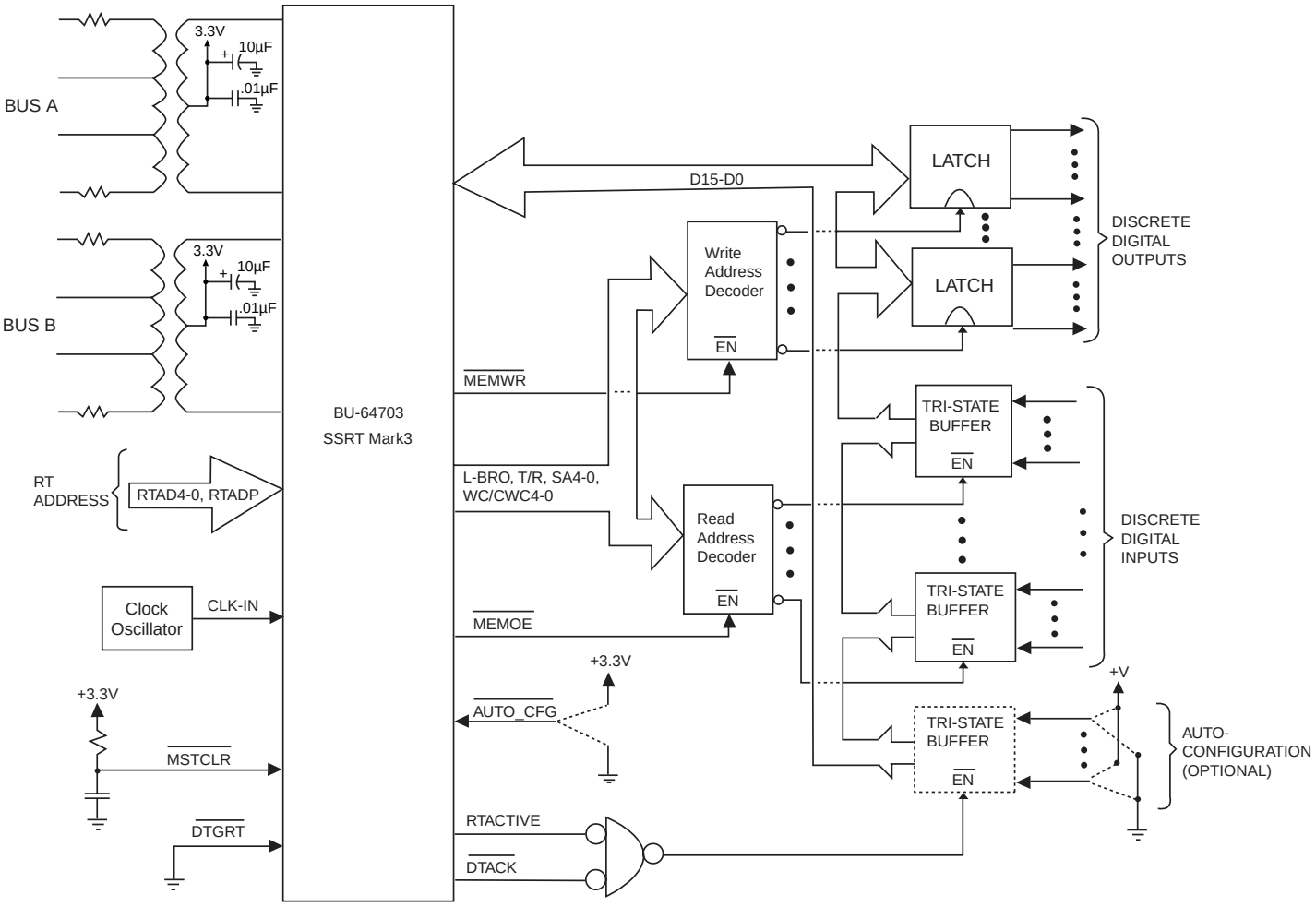


FIGURE 16. SSRT Mark3-TO-SIMPLE SYSTEM INTERFACE (Shown for BURST MODE)

BIT WORD

The SSRT Mark3 provides an internally formulated Built-In-Test word (BIT word). This word is transmitted to the BC in response to a Transmit BIT Word Mode Code Command. The BIT word bit functions and descriptions are provided in TABLE 5.

TABLE 5. INTERNAL BUILT-IN-TEST (BIT) WORD DEFINITION

BIT	FUNCTION	DESCRIPTION
15 (MSB)	TRANSMITTER TIMEOUT	Set if the SSRT Mark3's failsafe timer detected a fault condition. The transmitter timeout circuit will automatically shut down the CH. A or CH. B transmitter if it transmits for longer than 660.5 µs.
14 13	CH. B LOOP TEST FAILURE CH. A LOOP TEST FAILURE	A loopback test is performed on the transmitted portion of every non-broadcast message. A validity check is performed on the received version of every word transmitted by the SSRT Mark3. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of the last word does not match the transmitted version and/or the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, parity), or a failsafe timeout occurs on the respective channel, the LOOP TEST FAILURE bit for the respective bus channel will be set.
12	HANDSHAKE FAILURE	If this bit is set, it indicates that the subsystem had failed to respond with the DMA handshake input $\overline{\text{DTGRT}}$ asserted within 10 µs after the SSRT Mark3 has asserted $\overline{\text{DTREQ}}$.
11 10	TRANSMITTER SHUTDOWN B TRANSMITTER SHUTDOWN A	If either of these bits are logic "1", this indicates that the respective 1553 transmitter has been shut down by means of a Transmitter shutdown mode command.
9	TERMINAL FLAG INHIBITED	Set to logic "1" if the SSRT Mark3's Terminal flag RT status bit has been disabled by an Inhibit terminal flag mode code command. Will revert to logic "0" if an Override inhibit terminal flag mode code command is received.
8	BIT TEST FAIL	Set to logic "1" to denote that the SSRT Mark3 has failed its off-line protocol self-test. This bit will be logic "0" if the self-test passed or had not been performed.
7	HIGH WORD COUNT	Set to logic "1" if the previous message had a high word count error.
6	LOW WORD COUNT	Set to logic "1" if the previous message had a low word count error.
5	INCORRECT SYNC TYPE RECEIVED	If set, indicates that the SSRT Mark3 detected a Command sync in a received Data Word.
4	INVALID WORD MANCHESTER/PARITY ERROR RECEIVED	Indicates that the SSRT Mark3 received one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.
3	RT-RT TRANSFER RESPONSE ERROR (no gap, data, sync, address mismatch)	This bit is set if the SSRT Mark3 is the receiving RT for an RT-to-RT transfer and one or more of the following errors occurs: (1) If the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.
2	RT-RT TRANSFER NO RESPONSE TIMEOUT	If set, indicates that, for the previous message, the SSRT Mark3 was the receiving RT for an RT-to-RT transfer and that the transmitting RT either did not respond or responded later than the SSRT Mark3 RT-to-RT timeout time. The SSRT Mark3's RT-to-RT response timeout time is defined as the time from the mid-bit crossing of the parity bit of the transmit Command Word to the mid-sync crossing of the transmitting RT status word. The value of the SSRT Mark3's RT-to-RT response timeout time is in the range from 17.5 to 19.5 µs.
1	RT-RT TRANSFER - T/R ERROR ON SECOND COMMAND OR INVALID ADDRESS	If the SSRT Mark3 is the receiving RT for an RT-to-RT transfer, if this bit is set, it indicates one or more of the following error conditions in the transmit Command Word: (1) T/R bit = logic "0"; (2) subaddress = 00000 or 11111; (3) same RT Address field as the receive Command Word.
0 (LSB)	COMMAND WORD CONTENTS ERROR	Indicates that a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) The Command Word is a non-mode code, broadcast, transmit command; (2) a message with a T/R bit of "0", a subaddress/mode field of 00000 or 11111, and a mode code field with a value between 00000 and 01111; (3) a mode code command that is not permitted to be broadcast (e.g., Transmit Status) is sent to the broadcast address 11111.

Note:

Bits 15 through 9 are cleared only following a RESET input or receipt of a Reset Remote Terminal mode command. Bits 8 through 0 are updated as a result of every message processed.

MODE CODES

The SSRT Mark3 fully implements all 13 of the dual redundant MIL-STD-1553B mode codes. Four of the mode codes, Transmit vector word, Synchronize (with data), Selected transmitter shutdown, and Override transmitter shutdown, involve data transfers with the subsystem. For the Transmit last command mode command, the data word transmitted is from the SSRT Mark3's last command internal register. For the Transmit BIT word mode command, the SSRT Mark3's internally formulated BIT Word is transmitted. TABLE 6 provides a summary of the 1553B mode codes supported by the SSRT Mark3.

SUMMARY OF RESPONSES TO MODE CODE MESSAGES

The SSRT Mark3's responses to mode codes, including responses to various error conditions, are summarized in TABLE 6.

TABLE 6. MODE CODE SUMMARY

T/$\overline{R}$ BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST ALLOWED
0	00000-01111	Undefined	No	No
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001-01111	RESERVED	No	TBD
1	10000	Transmit Vector Word	From Subsystem	No
0	10001	Synchronize with Data	To Subsystem	Yes
1	10010	Transmit Last Command	From Internal Register	No
1	10011	Transmit BIT Word	From Internal Register	No
0	10100	Selected Transmitter Shutdown (see Note)	To Subsystem	Yes
0	10101	Override Selected Transmitter Shutdown (see Note)	To Subsystem	Yes
1	10110-11111	RESERVED	From Subsystem	TBD
0	10110-11111	RESERVED	To Subsystem	TBD

Note:

For the Selected transmitter shutdown and Override transmitter shutdown mode commands, the SSRT Mark3 responds with Clear Status but no action is taken.

DETAILED MODE CODES FUNCTIONAL DESCRIPTION

The applicable Mode Codes for the SSRT Mark3 are described below:

DYNAMIC BUS CONTROL (T/$\overline{R}$ = 1; 00000)
MESSAGE SEQUENCE = DBC + STATUS
The SSRT Mark3 responds with Status showing non-acceptance of the mode code command.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).
5. **Broadcast Address.** No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

SYNCHRONIZE WITHOUT DATA WORD (T/$\overline{R}$ = 1; 00001)
MESSAGE SEQUENCE = SYNC + STATUS
The SSRT Mark3 responds with Status.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

TRANSMIT STATUS WORD (T/$\overline{R}$ = 1; 00010)
MESSAGE SEQUENCE = TRANSMIT STATUS + STATUS
The Status register is **not** updated before it is transmitted and contains the resulting status from the previous command (assuming that it was not a Transmit status or Transmit last command mode command).
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word)
3. **T/$\overline{R}$ bit Set to Zero.** No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).
5. **Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Contents Error (BIT Word).

INITIATE SELF-TEST (T/$\overline{R}$ = 1; 00011)
MESSAGE SEQUENCE = SELF TEST + STATUS
If the command was non-broadcast, the SSRT Mark3 responds with Status. If the command was either non-broadcast or broadcast, the SSRT Mark3 will go offline and perform its internal off-line protocol self-test. The self-test exercises the SSRT Mark3's encoder and decoders, registers, transmitter watchdog timer, and protocol logic. This test is completed in approximately 32,000 clock cycles. That is, about 1.6 ms with a 20 MHz clock, 2.0 ms at 16 MHz, 2.7 ms at 12 MHz, and 3.2 ms at 10 MHz.
While the SSRT Mark3 is performing its off-line self-test, it will ignore (and therefore not respond to) all messages received from the 1553 bus. The bus controller may determine the result of the self-test by means of a Transmit BIT word mode command. If the self-test passes, bit 8 of the SSRT Mark3's BIT word (BIT Test Fail) will be logic "0"; if the self-test fails, this bit will be logic "1". In addition, if self-test fails, the terminal flag status word bit will be set to logic “1” in response to the next non-broadcast message.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).
5. **Loopback Test Failure.** Set Terminal Flag bit in internal Status register (Status Word for next non-broadcast command), Current Channel (A or B) Loop Test Failure and CH A/B Loop Test Failure (BIT Word), assert $\overline{\text{RTFAIL}}$ output.

TRANSMITTER SHUTDOWN (T/$\overline{R}$ = 1; 00100)

MESSAGE SEQUENCE =SHUTDOWN + STATUS

This command is only used with dual redundant bus systems. The SSRT Mark3 responds with Status. Following the Status transmission, the SSRT Mark3 inhibits any further transmission from the alternate redundant channel. Once shutdown, the transmitter can only be reactivated by an Override Transmitter Shutdown or Reset RT mode command, or Hardware Reset (MSTRCLR input). Note that the receivers on both channels are always active, even when the transmitters are inhibited.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

OVERRIDE TRANSMITTER SHUTDOWN (T/$\overline{R}$ = 1; 00101)

MESSAGE SEQUENCE = OVERRIDE SHUTDOWN + STATUS

This command is only used with dual redundant bus systems. The SSRT Mark3 responds with Status. At the end of the Status transmission, the SSRT Mark3 reactivates the transmitter of the alternate redundant bus. If the command was broadcast, the Broadcast Command Received Status Word bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

INHIBIT TERMINAL FLAG BIT (T/$\overline{R}$ = 1; 00110)

MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG + STATUS

The SSRT Mark3 responds with Status and inhibits further setting of the Terminal Flag bit in its internal Status Word register. Once the Terminal Flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT mode code commands, or by Reset. If the command was broadcast, the Broadcast Received bit is set, the state of the Terminal Flag bit in the internal Status Word register remains unchanged and Status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

OVERRIDE INHIBIT TERMINAL FLAG BIT (T/$\overline{R}$ = 1; 00111)

MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG + STATUS

The SSRT Mark3 responds with Status and re-enables the Terminal Flag bit in its internal Status register. If the command was a broadcast, the Broadcast Command Received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

RESET REMOTE TERMINAL (T/$\overline{R}$ = 1; 01000)

MESSAGE SEQUENCE = RESET REMOTE TERMINAL + STATUS

The SSRT Mark3 responds with Status and internally resets. The Message Error and Broadcast Command Received bits of the internal Status register are reset to 0. The internal BIT Word Register is reset to 0. If either of the 1553 transmitters has been shut down, the shutdown condition is overridden. If the Terminal Flag bit has been inhibited, the inhibit is overridden.

If the command is received as a broadcast, the Broadcast Command Received bit is set and the Status Word is suppressed. Also, if the command is received as a broadcast and the Terminal Flag bit had been set as a result of the Loopback test of the previous message, the Terminal Flag bit is not reset to zero.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

RESERVED MODE CODES (T/$\overline{R}$ = 1; 01001 - 01111)

MESSAGE SEQUENCE = RESERVED MODE COMMAND + STATUS

The SSRT Mark3 responds with status. If the command has been illegalized by means of the illegalization table, the Message Error Status Word bit will be set.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

TRANSMIT VECTOR WORD (T/$\overline{R}$ = 1; 10000)

MESSAGE SEQUENCE = TRANSMIT VECTOR WORD + STATUS VECTOR WORD

The SSRT Mark3 transmits a Status Word followed by a vector word. The vector word is read from the external subsystem.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).
4. **T/R bit Set to Zero plus one Data Word**. The SSRT Mark3 will respond with Status
5. **Zero T/$\overline{R}$ bit and Broadcast Address, no Data Word.** No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Low Word Count (BIT word).
6. **Zero T/$\overline{R}$ bit and Broadcast Address, plus one Data Word.** No Status response. Set Broadcast Command Received bits (Status Word)
7. **Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT word).

SYNCHRONIZE WITH DATA WORD (T/$\overline{R}$ = 0; 10001)

MESSAGE SEQUENCE = SYNCHRONIZE COMMAND/DATA WORD + STATUS

The SSRT Mark3 will write the received 16 bit data word to the external subsystem.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Correct Command Not Followed by Data Word.** No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word)
3. **Command Followed by too many Data Words.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT word).
4. **Command T/$\overline{R}$ bit set to One followed by Data Word.** No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit set to One not followed by Data Word.** The SSRT Mark3 replies with Status plus one Data Word. The Data Word is read from the subsystem (or single-word data block for subaddress 0000 or 1111).
6. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status Word); Set Command Word Contents Error (BIT word).

TRANSMIT LAST COMMAND (T/$\overline{R}$ = 1; 10010)

MESSAGE SEQUENCE = TRANSMIT LAST COMMAND + STATUS/LAST COMMAND

The Status register is not updated before transmission. It contains the Status from the previous command. The Data Word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND or TRANSMIT STATUS WORD mode command).

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).
3. **T/$\overline{R}$ bit Set to Zero, no Data Word.** No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).
4. **T/$\overline{R}$ bit Set to Zero, plus one Data Word.** The SSRT Mark3 will respond with Status. The Data Word is transferred to the internal register.
5. **Zero T/$\overline{R}$ bit and Broadcast Address, no Data Word.** No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error(BIT Word).
6. **Zero T/$\overline{R}$ bit and Broadcast Address, one Data Word.** No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to the internal register.
7. **Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT Word).

TRANSMIT BIT WORD (T/$\overline{R}$ = 1; 10011)

MESSAGE SEQUENCE = TRANSMIT BIT WORD + STATUS/BIT WORD

The SSRT Mark3 responds with Status followed by the Built-in Test (BIT) word.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).
3. **T/$\overline{R}$ bit Set to Zero, no Data Word.** No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).
4. **T/R bit Set to Zero, plus one Data Word.** The SSRT Mark3 will respond with Status. The Data Word is transferred to internal registers.
5. **Zero T/$\overline{R}$ bit and Broadcast Address, no Data Word.** No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error (BIT Word).
6. **Zero T/$\overline{R}$ bit and Broadcast Address, one Data Word.** No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to internal registers.
7. **Broadcast Address.** No Status response. Set Message Error and Broadcast Command received bits (Status Word), Command Word contents Error (BIT Word).

SELECTED TRANSMITTER SHUTDOWN (T/$\overline{R}$ = 0; 10100)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN/DATA + STATUS

The Data Word received is transferred to the subsystem and Status is transmitted. No other action is taken by the SSRT Mark3. No transmitters are shut down as a result of this mode command. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No Status response. Set Message Error bit (Status Word), and Low Word Count Bit (BIT Word). No status response. Bits Set: message error (SW), High Word Count, Illegal Mode Code (BIT Word)
3. **Command Followed by too many Data Words.** No Status response. Set Message Error bit (Status Word), and High Word Count Bit (BIT Word).
4. **Command T/$\overline{R}$ bit Set to One followed by one Data Word.** No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to One not followed by Data Word.** The SSRT Mark3 replies with Status plus one Data Word. The Data Word is read from the subsystem.
6. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Command Contents Error (BIT Word).

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (T/$\overline{R}$ = 0; 10101)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN/DATA + STATUS

The Data Word received is transferred to the subsystem. No transmitters that have been previously shut down are reactivated as a result of this command. No other action is taken by the SSRT Mark3. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).
3. **Command Followed by too many Data Words.** No Status response. Set Message Error bit (Status Word), and High Word Count bit (BIT Word).
4. **Command T/$\overline{R}$ bit Set to One followed by Data Word.** No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to One not followed by Data Word.** The SSRT Mark3 replies with Status plus one Data Word. The Data Word is read from the subsystem.
6. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Command Contents Error (BIT Word).

RESERVED MODE CODES (T/$\overline{R}$ = 1; 11111)

MESSAGE SEQUENCE (when T/$\overline{R}$ = 1) = RESERVED MODE CODE STATUS/DATA
(when T/$\overline{R}$ = 0) = RESERVED MODE CODE DATA + STATUS

For a RESERVED receive Command, the SSRT Mark3 stores the Data Word to the subsystem. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed. For a RESERVED transmit Command Word, the SSRT Mark3 responds with Status plus a single Data Word. The Data Word is read from the subsystem.

ERROR CONDITIONS (T/$\overline{R}$ = 1)

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. **Broadcast Command.** No Status response. Set Message Error bit (status word), and Command Word Contents Error (BIT Word).

ERROR CONDITIONS (T/$\overline{R}$ = 0)

1. **Invalid Command.** No response, command ignored.
2. **Command not followed by Contiguous Data Word.** No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).
3. **Command followed by too many Data Words.** No Status response. Set Message Error bit (Status Word), and High Word Count (BIT word).

TABLE 7. POWER AND GROUND

SIGNAL NAME	PIN	DESCRIPTION
+3.3V_Xcvr	10	Transceiver power.
+3.3V_Logic	30	Logic power.
	51	
	69	
Gnd_Xcvr	22	Transceiver Ground.
	79	
Gnd_Logic	14	Logic Ground.
	31	
	50	
	70	
	77	

TABLE 8. MIL-STD-1553 ISOLATION TRANSFORMER INTERFACE

SIGNAL NAME	PIN	DESCRIPTION
TX/RX-A (I/O)	3	Analog transmit/receive input/output signals. Connect directly to 1553 isolation transformers.
$\overline{\text{TX/RX-A}}$ (I/O)	5	
TX/RX-B (I/O)	15	
$\overline{\text{TX/RX-B}}$ (I/O)	17	

TABLE 9. DATA BUS (16)

SIGNAL NAME	PIN	DESCRIPTION
D15 (I/O) (MSB)	59	16-bit bi-directional data bus. When the SSRT Mark3 is writing data to the external system, these signals are active outputs. At all other times, these signals are high impedance inputs.
D14 (I/O)	56	
D13 (I/O)	54	
D12 (I/O)	55	
D11 (I/O)	58	
D10 (I/O)	60	
D09 (I/O)	57	
D08 (I/O)	52	
D07 (I/O)	53	
D06 (I/O)	41	
D05 (I/O)	49	
D04 (I/O)	43	
D03 (I/O)	48	
D02 (I/O)	47	
D01 (I/O)	42	
D00 (I/O) (LSB)	46	

TABLE 10. COMMAND / ADDRESS BUS		
SIGNAL	**PIN**	**DESCRIPTION**
L_BRO (O)	1	Latched Broadcast. This two-state output signal is latched following receipt of a new command word. For a broadcast command, this signal outputs a value of logic "1". For a non-broadcast message, this signal will output logic "0".
T / $\overline{R}$	2	Transmit/Receive. This two-state output signal is latched following receipt of a new command word. For a transmit message, this signal will output a value of logic "1". For a receive message, this signal will output logic "0".
SA4 (O)	75	Subaddress. These five two-state output signals are latched following receipt of a new command word. They provide the subaddress field of the received command word.
SA3 (O)	7	
SA2 (O)	12	
SA1 (O)	27	
SA0 (O)	74	
WC / MC / CWC4 (O) (MSB)	78	Word Count/Mode Code/Current Word Count. Following receipt of a new command word, these five two-state output signals provide the contents of the command word's Word Count/Mode Code field. For a non-mode code receive message, the contents of WC/CWC are updated and incremented to reflect the value of the current data word being transferred to the system (in non-burst mode), or to the internal FIFO (in burst mode). CWC increments from 0 to the value of the Word Count field - 1 during the message. At the end of a non-mode code receive message in burst mode, the contents of CWC will then increment from 0 to the value of the word count field -1, as each word is transferred from the internal FIFO to the external system over D15-D0. In burst mode, it takes three clock cycles to transfer each word to the external system. For a non-mode code transmit command, the value of CWC starts from 0 and increments to the value of Word Count - 1, as each word is read from the external system and transferred to the SSRT Mark3. For a mode code command, the WC/CWC outputs the command word mode code field, which remains latched through the end of the message (until receipt of a subsequent command word).
WC / MC / CWC3 (O)	13	
WC / MC / CWC2 (O)	19	
WC / MC / CWC1 (O)	33	
WC / MC / CWC0 (O) (LSB)	18	

TABLE 11. DMA HANDSHAKE AND TRANSFER CONTROL SIGNALS		
SIGNAL	**PIN**	**DESCRIPTION**
$\overline{DTREQ}$ (O)	29	Data Transfer Request. Active low level output signal used to request use of the external system data bus (D15-D0).
$\overline{DTGRT}$ (I)	72	Data Transfer Grant. Input from the external subsystem that must be asserted low in response to the SSRT Mark3 asserting $\overline{DTREQ}$ low in order to enable the SSRT Mark3 to read data from or write data to the external subsystem. The maximum allowable time from $\overline{DTREQ}$ to $\overline{DTGRT}$ is 10 µs. If the SSRT Mark3's DMA handshake isn't required, $\overline{DTGRT}$ may be hardwired to logic "0".
$\overline{DTACK}$ (O)	35	Data Transfer Acknowledge. Active low output signal used to indicate the SSRT Mark3's acceptance of the system data bus (D15-D0), in response to a data transfer grant ($\overline{DTGRT}$). The SSRT Mark3's data transfers over D15-D0 will be framed by the time that $\overline{DTACK}$ is asserted low. If $\overline{AUTO\_CFG}$ is strapped to logic "0", there will be a $\overline{DTREQ}$/$\overline{DTGRT}$ handshake cycle after the rising edge of $\overline{MSTCLR}$, following power turn-on. After $\overline{DTGRT}$ is sampled low, $\overline{DTACK}$ and RTACTIVE will then be asserted low to enable configuration data to be read from an external tri-state buffer. For transmit messages, or receive messages in non-burst mode, or for receive messages to subaddress 30 assuming that Subaddress 30 Autowrap is disabled, $\overline{DTACK}$ will be asserted low to indicate the transfer of individual words between the external system and the SSRT Mark3. For receive messages in burst mode assuming a valid received message, $\overline{DTACK}$ will be asserted low after the $\overline{DTREQ}$-to-$\overline{DTGRT}$ handshake following the receipt of the last received data word. It will remain low for the duration of the DMA burst write transfer from the SSRT Mark3 to the external system. The total time for a burst write transfer is three clock cycles times the number of data words.
$\overline{HS\_FAIL}$ (O)	63	Handshake Fail. If this signal is asserted low, this indicates a handshake timeout condition. That is, the system did not respond with a $\overline{DTGRT}$ in time, following the SSRT Mark3's assertion of $\overline{DTREQ}$.
$\overline{MEMOE}$ (O)	20	Memory Output Enable. $\overline{MEMOE}$ two-state output signal is used to enable data inputs from the external system to be enabled on to D15-D0. $\overline{MEMOE}$ pulses low for three clock cycles for each data word read from the external system. The SSRT Mark3 latches the data one clock cycle prior to the rising edge of $\overline{MEMOE}$.
$\overline{MEMWR}$ (O)	28	Memory Write. Active low two-state output signal (one clock cycle wide) asserted low during SSRT Mark3 write cycles. Used to transfer data from the SSRT Mark3 to the external system. The external system may latch data on either the falling or rising edge of $\overline{MEMWR}$.

TABLE 12. RT ADDRESS		
SIGNAL	**PIN**	**DESCRIPTION**
RTAD4 (I) (MSB)	40	RT Address inputs.
RTAD3 (I)	39	
RTAD2 (I)	24	
RTAD1 (I)	45	
RTAD0 (I) (LSB)	38	
RTADP (I)	44	Remote Terminal Address Parity. This input signal must provide an **odd** parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an odd number of logic "1"s from among RTAD4-RTAD0 and RTADP.
RT_AD_LAT (I)	36	RT Address Latch. If RT_AD_LAT is connected to logic "0", then the SSRT Mark3 is configured to accept a hardwired RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4-RTAD0 and RTADP will be latched internally by the SSRT Mark3 on the rising edge of RT_AD_LAT.
$\overline{\text{RT\_AD\_ERR}}$ (O)	6	Remote Terminal Address Error. Output Signal that reflects the parity combination of the RTAD[4:0] inputs and RTADP input. A high level indicates odd (correct) parity. A low level indicates even (incorrect) parity. **Note**, if $\overline{\text{RT\_AD\_ERR}}$ is low, then the SSRT Mark3 will **not** recognize any valid Command Word received to its own RT address.

TABLE 13. RT STATUS WORD INPUTS		
SIGNAL	**PIN**	**DESCRIPTION**
$\overline{\text{ILLEGAL}}$ (I)	68	Illegal. Input to the SSRT Mark3 that is sampled after the Command Word transfer. A logic "0" will cause the Message Error bit in the status response to be set (logic "1"), while a logic "1" on this input will have no effect on the Message Error bit.
$\overline{\text{SRV\_RQST}}$ (I)	66	Service Request. When this input is logic "0", the Service request bit in the SSRT Mark3's status word will be logic "1". When this input is logic "1", the Service request bit in the SSRT Mark3's status word will be logic "0".
$\overline{\text{SSFLAG}}$ (I)	37	Subsystem Flag. If this input is asserted low, the Subsystem Flag bit will be set in the SSRT Mark3's Status Word.
$\overline{\text{BUSY}}$ (I)	61	Busy. If this input is asserted low, the Busy bit will be set to logic "1" in the SSRT Mark3's Status Word. If the Busy bit in the status word is logic "1", the SSRT Mark3 will not transmit any data words, except for a Transmit last command or Transmit BIT word mode command. For a receive command, if the SSRT Mark3 is Busy, it will still transfer data words to the external system (although these transfers may be blocked by means of external logic).

TABLE 14. RT ACTIVITY AND MESSAGE STATUS INDICATORS		
SIGNAL	**PIN**	**DESCRIPTION**
RTACTIVE (O)	62	RT Active. This signal will be low (logic "0") following power turn-on, and when the SSRT Mark3 is reading its Auto-configure word or is performing its internal self-test. After the self-test passes, or if the Auto-configure option is not used, or if Auto-configure is used but bit 5 of the Auto-configure word is logic "1" (meaning for the RT **to always** go online), RTACTIVE will then transition to logic "1". When this occurs, the SSRT Mark3 will begin processing messages over the 1553 bus. If Auto-configure is enabled, and bit 5 of the Auto-configure word is logic "0" and the self-test fails, then RTACTIVE will remain at logic "0". In this case, the SSRT Mark3 will remain offline and not process any 1553 messages. A failed self test will cause RTFAIL_L to be asserted low (logic “0"). If the auto-configure option is used, the external system should enable the configuration bits on D5-D0 when RTACTIVE and $\overline{\text{DTACK}}$ are both outputting logic "0".
$\overline{\text{INCMD}}$	32	In-command. This two-state output is asserted low whenever a message is being processed by the SSRT Mark3.
$\overline{\text{GBR}}$ (O)	67	Good Block Received. Low level two-state output pulse (2 clock cycles wide) that is used to indicate to the external system that a valid, legal, non-mode receive command with the correct number of valid data words has been received and transferred to the external system. For non-burst mode, this pulse will occur after the last data word is transferred. Assuming a $\overline{\text{DTREQ}}$-to-$\overline{\text{DTGRT}}$ time of 0, this will be approximately 4 µs following the mid-parity bit crossing of the last received data word. For burst mode, the $\overline{\text{GBR}}$ pulse will begin synchronous with the rising edge of $\overline{\text{DTACK}}$ at the end of the burst write transfer.
$\overline{\text{MSG\_ERR}}$ (O)	34	Message Error. Active low level two-state output signal used to flag to the external system that there was a message error on the 1553 bus communication (word, gap, or word count error) for a particular message. This output goes low upon detecting the error and is reset following the receipt of the next valid command word (to the RT) from the 1553 bus, or if $\overline{\text{MSTCLR}}$ is asserted low. If this output goes low, all further servicing of the current message is aborted.
$\overline{\text{RTFAIL}}$ (O)	64	Remote Terminal Fail. This two-state output signal will be asserted low following a failure of the built-in self-test performed following power turn-on or as the result of the receipt of an Initiate self-test mode command. The built-in off-line self-test includes tests of the Manchester encoder and decoders, transmitter failsafe timer, and RT protocol logic. In addition, $\overline{\text{RTFAIL}}$ will be asserted low following a failure of the on-line loop test for any non-broadcast message. The on-line loop test verifies the validity of the received version of all transmitted words (sync, Manchester encoding, bit count, parity), and includes a bit-by-bit comparison and verification of the last transmitted word. If asserted to logic "0", $\overline{\text{RTFAIL}}$ will clear to logic "1" when the SSRT Mark3 begins transmission of its status word in response to a subsequent valid non-broadcast message.

TABLE 15. CONTROL INPUTS		
SIGNAL	**PIN**	**DESCRIPTION**
$\overline{\text{MSTCLR}}$ (I)	25	Master Clear. Negative true Reset input, asserted low following power turn-on. When coming out of a “reset” condition, note that the risetime of $\overline{\text{MSTCLR}}$ must be less than 10 µs.
$\overline{\text{AUTO\_CFG}}$ (I)	76	Auto-configure input. If connected to logic "1", then the auto-configure option is disabled, and the six configuration parameters revert to their default values as listed in TABLE 2. Note that the default condition for each configuration parameter is **enabled** (for the MIL-STD-1553A/B protocol selection, -1553B is the default). If $\overline{\text{AUTO\_CFG}}$ is connected to logic "0", then the configuration parameters are transferred over D5-D0 during a DMA read data transfer, when RTACTIVE and DTACK are logic "0", following MSTCLR transitioning from logic "0" to logic "1". Each of the configuration parameters is enabled if the SSRT Mark3 reads a value of logic "1" for the respective data bit.
BRO_ENA (I)	71	Broadcast Enable. If this input is logic "1", the SSRT Mark3 will recognize RT address 31 as the broadcast address. If this input is logic "0", the SSRT Mark3 will not recognize RT address 31 as the broadcast address; however, in this configuration, RT address 31 may be used as a standard RT address.
TX_INH (I)	65	Transmitter inhibit input for the MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of the Channel A and Channel B transmitters, a value of logic "1" should be applied to this input.

TABLE 16. CLOCK INPUT

SIGNAL	PIN	DESCRIPTION
CLK_IN (I)	26	Clock Input. The clock frequency must be designated by means of the CLK_SEL_1 and CLK_SEL_0 inputs.
CLK_SEL_1 (I)	73	These two inputs are used to designate the SSRT Mark3's clock frequency, as follows: **CLK_SEL_1** **CLK_SEL_0** **Clock Frequency** 0 0 10 MHz 0 1 20 MHz 1 0 12 MHz 1 1 16 MHz
CLK_SEL_0 (I)	80	

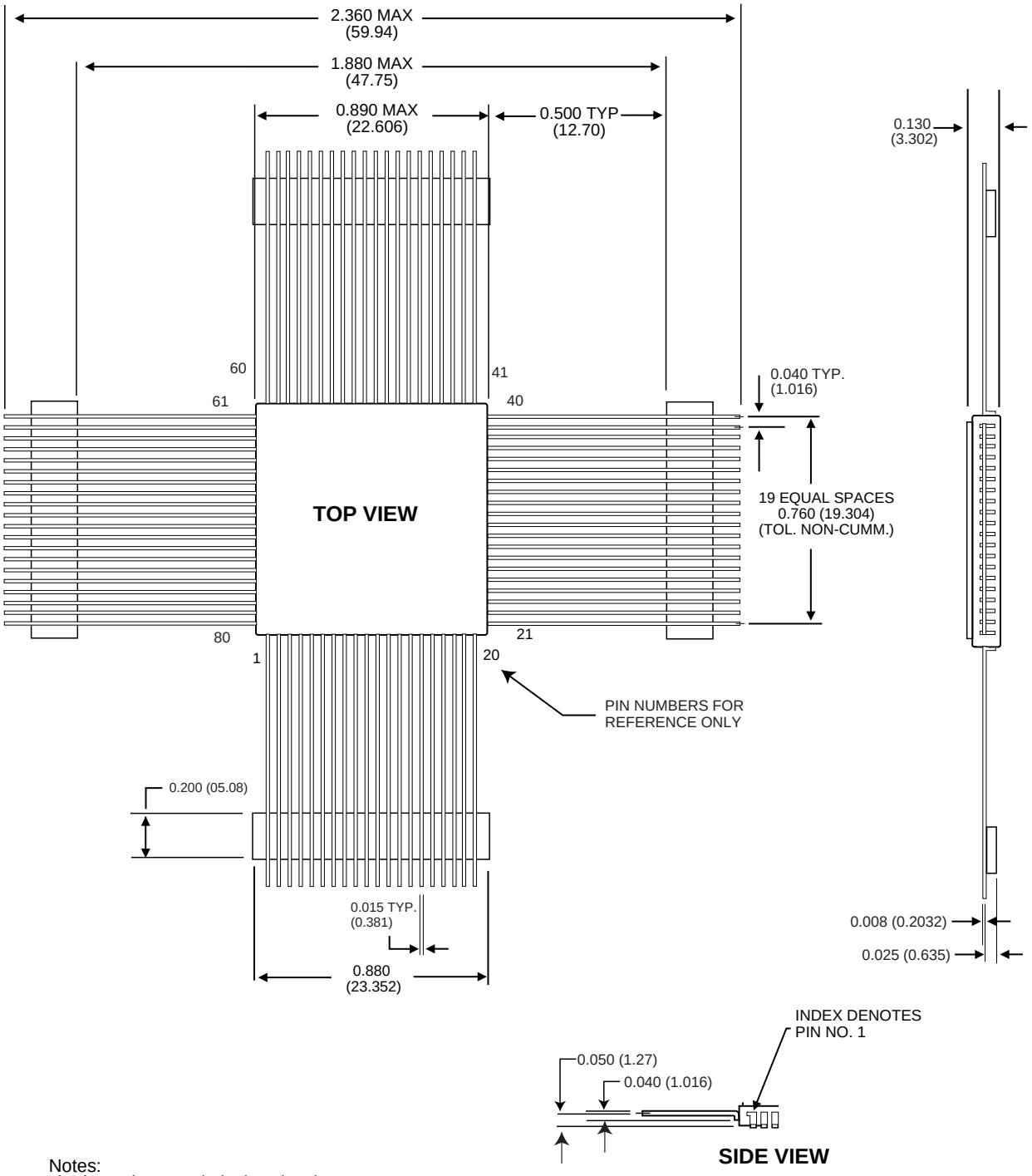
TABLE 17. FACTORY TEST (NO USER CONNECTIONS)

SIGNAL	PIN	DESCRIPTION
NC	4	For factory test only. Do not connect for normal operation.
	8	
	9	
	11	
	16	
	21	
	23	

PIN FUNCTIONS

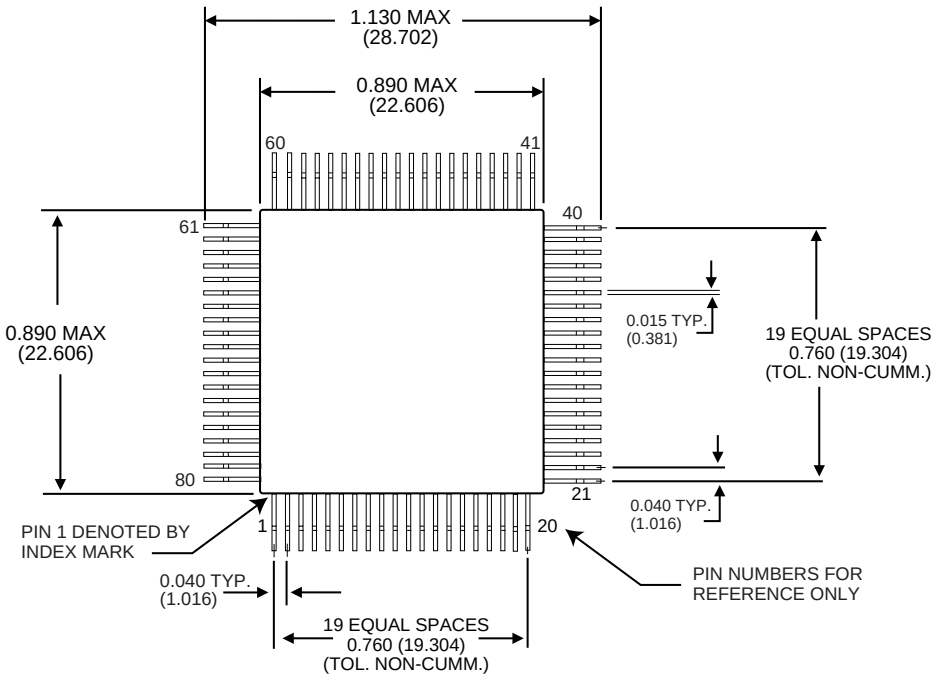
TABLE 18. "GULL WING" AND FLAT PACKAGE PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	L_BRO	21	N/C	41	D6	61	$\overline{\text{BUSY}}$
2	T/$\overline{\text{R}}$	22	GROUND_XCVR	42	D1	62	RTACTIVE
3	TX/RX_A	23	N/C	43	D4	63	$\overline{\text{HS\_FAIL}}$
4	N/C	24	RTAD2	44	RTADP	64	$\overline{\text{RT\_FAIL}}$
5	$\overline{\text{TX/RX\_A}}$	25	$\overline{\text{MSTCLR}}$	45	RTAD1	65	TX_INH
6	$\overline{\text{RT\_AD\_ERR}}$	26	CLOCK_IN	46	D0	66	$\overline{\text{SRV\_RQST}}$
7	SA3	27	SA1	47	D2	67	$\overline{\text{GBR}}$
8	N/C	28	$\overline{\text{MEMWR}}$	48	D3	68	$\overline{\text{ILLEGAL}}$
9	N/C	29	$\overline{\text{DTREQ}}$	49	D5	69	+3.3V_LOGIC
10	+3.3 V_XCVR	30	+3.3V_LOGIC	50	GROUND_LOGIC	70	GROUND_LOGIC
11	N/C	31	GROUND_LOGIC	51	+3.3V_LOGIC	71	$\overline{\text{BRO\_ENA}}$
12	SA2	32	$\overline{\text{INCMD}}$	52	D8	72	$\overline{\text{DTGRT}}$
13	WC3	33	WC1	53	D7	73	CLK_SEL_1
14	GROUND_LOGIC	34	$\overline{\text{MSG\_ERR}}$	54	D13	74	SA0
15	TX/RX_B	35	$\overline{\text{DTACK}}$	55	D12	75	SA4
16	N/C	36	RT_AD_LAT	56	D14	76	$\overline{\text{AUTO\_CFG}}$
17	$\overline{\text{TX/RX\_B}}$	37	$\overline{\text{SSFLAG}}$	57	D9	77	GROUND_LOGIC
18	WC0	38	RTAD0	58	D11	78	WC4
19	WC2	39	RTAD3	59	D15	79	GROUND_XCVR
20	$\overline{\text{MEMOE}}$	40	RTAD4	60	D10	80	CLK_SEL_0

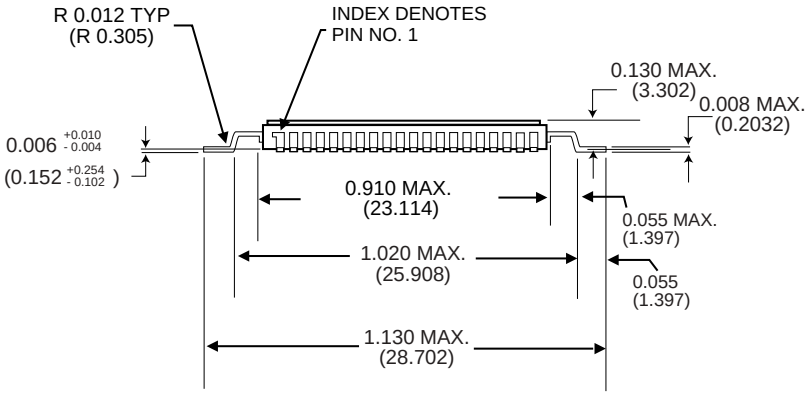


Notes:
1) Dimensions are in inches (mm).

FIGURE 17. BU-64703FX FLAT PACKAGE MECHANICAL OUTLINE



TOP VIEW



SIDE VIEW

Notes:
1) Dimensions are in inches (mm).

FIGURE 18. BU-64703GX GULL WING PACKAGE MECHANICAL OUTLINE

ORDERING INFORMATION

BU-64703XX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = Standard Testing
- 2 = MIL-STD-1760 Amplitude Compliant (Not available with Voltage/Transceiver Option 9)

Process Requirements:
- 0 = Standard DDC practices, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

Temperature Range/Data Requirements:**
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 6 = Custom Part (Reserved)
- 7 = Custom Part (Reserved)
- 8 = 0°C to +70°C with Variables Test Data

Voltage/Transceiver Option:
- 8 = +3.3 Volts rise/fall times = 100 to 300 ns (-1553B)
- 9 = +3.3 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible) (Not available with Test Criteria Option "2" MIL-STD-1760 Amplitude Compliant)

Package Type:
- F = Flat Pack
- G = "Gull Wing" (Formed Lead)
- B = 324-ball BGA Package (Consult factory)

Logic Voltage
- 3 = 3.3 Volt

Product Type:
- BU-6470 = RT only with simple (non-processor) interface

*Standard DDC Processing with burn-in and full temperature test—see TABLE below.

** Temperature range refers to "Case Temperature".

STANDARD DDC PROCESSING

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, TABLE 1	—

NOTES

The information in this Preliminary data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

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