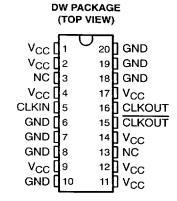
# TNETA1530 155.52-MHz CLOCK-GENERATION DEVICE

SDNS016E - FEBRUARY 1994 - REVISED APRIL 1996

- Generates a 155.52-MHz Clock From a 19.44-MHz TTL Clock
- Provides Differential Pseudo-ECL (PECL) Outputs
- Operates From a Single 5-V Power Supply
- Packaged in 20-Pin Plastic Small-Outline (DW) Package

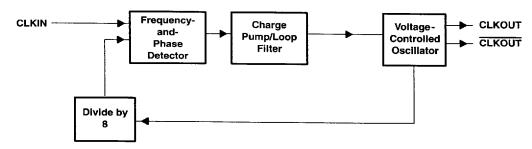
#### description

The TNETA1530 is a 155.52-MHz clockgeneration device that utilizes a TTL-clock input at 19.44 MHz. The 155.52-MHz clock is provided on differential pseudo-ECL (PECL) outputs. The device operates from a single 5-V power supply. An internal second-order low-pass filter is used to reduce jitter.



NC - No internal connection

### functional block diagram



#### **Terminal Functions**

TERMINAL					
NAME	NO.	VO	DESCRIPTION		
CLKIN	5	Ī	19.44-MHz TTL-input clock	-	
CLKOUT	16	0	155.52-MHz PECL-output clock true		
CLKOUT	15	0	155.52-MHz PECL-output clock complement		
GND	6, 7, 8, 10, 18, 19, 20		Ground (0-V reference)		
NC	3, 13		No internal connection. Leave floating.		
VCC	1, 2, 4, 9, 11, 12, 14, 17		Supply voltage		



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# TNETA1530 155.52-MHz CLOCK-GENERATION DEVICE

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> (see Note 1)	–0.5 V to 7 V
Input voltage range, V <sub>1</sub>	–1.2 V to 7 V
Operating free-air temperature range, T <sub>A</sub>	40 C to 85°C
Storage temperature range, T <sub>sto</sub>	65 C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, an functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is no implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

### recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.75	5	5.25	٧
VIH	High-level input voltage	TTL (see Note 2)	2			٧
VIL	Low-level input voltage	TTL (see Note 2)			0.8	V
lк	Input clamp current	TTL			-18	mA
TA	Operating free-air temperature		-40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

# electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS	MIN TYP	MAX	UNIT
Vон	High-level output voltage	V <sub>CC</sub> = 5 V,	See Note 3	V <sub>CC</sub> - 0.	925	٧
VOL	Low-level output voltage	V <sub>CC</sub> = 5 V,	See Note 3	V <sub>CC</sub> - 1.	650	٧
VO(PP)	Output voltage swing, PECL	$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V},$	See Note 3	525		mV
VIK	Input clamp voltage	V <sub>CC</sub> = 4.75 V,	I∟ = −18 mA		-1.2	٧
łj	Input current, TTL	V <sub>CC</sub> = 5.25 V,	$V_I = V_{CC}$ or GND		±1	μΑ
lcc	Supply current	V <sub>CC</sub> = 5.25 V, Outputs open	f = 155.52 MHz,	50		mA
	Supply current	V <sub>CC</sub> = 5.25 V, See Note 3	f = 155.52 MHz,		75	lin,

NOTE 3: These outputs are terminated with a  $50\Omega$  resistor to  $V_{CC}-2$  V.

# operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty cycle, generated clock	See Note 3	45%	50%	55%	
RMS jitter, generated clock			13	32	ps
Peak-to-peak jitter, generated clock			90	320	ps

NOTE 3: These outputs are terminated with a 50  $\Omega$  resistor to V<sub>CC</sub>-2 V.



1007 017 102 50% 033000 - 572270, 12770 70200

8961724 0109586 016