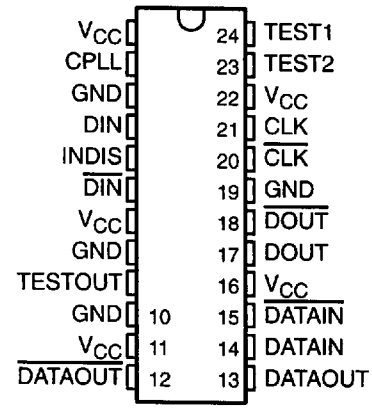
TNETA1555
155.52-MBIT/S CLOCK-RECOVERY DEVICE

SDNS001B – SEPTEMBER 1992 – REVISED DECEMBER 1994

- **Recovers a 155.52-MHz Clock Signal From a 155.52-Mbit/s STS-3/STM-1 NRZ Data Stream**
- **Accepts Pseudo-ECL (PECL) Input Voltage Levels on the Input Data Stream**
- **Provides a Separate Pseudo-ECL-to-True-ECL Converter for an Additional Data Signal Requiring Conversion**
- **Requires a Single 5-V Supply**

DW PACKAGE
(TOP VIEW)



description

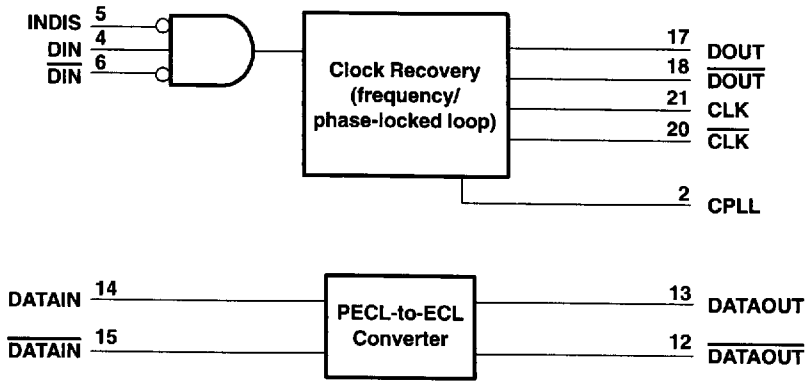
The TNETA1555 device recovers an embedded clock signal from a 155.52-Mbit/s STS-3/STM-1 nonreturn-to-zero (NRZ) data stream using a frequency/phase-locked loop. The device accepts PECL (ECL signals referenced to 5 V instead of GND) input-voltage levels. The recovered clock and dat outputs are PECL compatible. The serial data input and recovered clock and data outputs are differential to provide maximum noise immunity.

The input disable (INDIS) disconnects the incoming serial data stream from the clock-recovery circuitry. When the INDIS input is high, the data output is forced low and the clock-recovery circuitry maintains the output frequency present at the time the input was disabled for a specific amount of time. This time is dependent upon the value of the capacitor in the loop filter.

A PECL-to-ECL converter is included in the device for those applications where an interface between the two different voltage levels is required. An example of such an application is an optical transmitter that requires ECL input voltage levels and a parallel-to-serial converter with pseudo-ECL-level outputs.

The TNETA1555 requires only a positive 5-V supply (5 V ± 5 %) for operation. The device is characterized for operation over a temperature range of −40°C to 85°C.

functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{CLK}$, CLK	20, 21	O	Recovered clock output. PECL compatible.
CPLL	2	I	Capacitor connection for phase-locked-loop filter (C_{PLL} = 0.1 μF recommended)
DATAIN, $\overline{DATAIN}$,	14, 15	I	PECL-compatible input for PECL-to-ECL converter
$\overline{DATAOUT}$, DATAOUT	12, 13	O	ECL-compatible output for PECL converter
DIN, $\overline{DIN}$	4, 6	I	Serial data input. PECL compatible.
$\overline{DOUT}$, DOUT	18, 17	O	Serial data output. PECL compatible.
GND	3, 8, 10, 19		Ground (0-V reference)
INDIS	5	I	Input disable terminal (TTL compatible). The device ignores the input data when INDIS is active and forces DOUT low and $\overline{DOUT}$ high.
TESTOUT	9	O	Manufacturing test output. Leave open.
TEST2	23	I	Manufacturing test input. Tied to GND.
TEST1	24	I	Manufacturing test input. Tied to GND.
V_{CC}	1, 7, 11, 16, 22		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, TTL ..... −1.2 V to 7 V
Input voltage range, ECL ..... −5.5 V to 0 V
Input voltage range, pseudo-ECL ..... 0 V to 7 V
Operating free-air temperature range, T_A ..... −40 C to 85°C
Storage temperature range, T_{stg} ..... −65 C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage, TTL	2			V
V_{IL}	Low-level input voltage, TTL			0.8	V
I_{IK}	Input clamp current, TTL			−18	mA
V_{IH}	High-level input voltage, PECL (see Note 2)	V_{CC} −1.1		V_{CC} −0.8	V
V_{IL}	Low-level input voltage, PECL (see Note 2)	V_{CC} −1.9		V_{CC} −1.5	V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DOUT, $\overline{\text{DOUT}}$, CLK, $\overline{\text{CLK}}$	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	V_{CC} –1.03		V_{CC} –0.85	V
		DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V,	See Notes 2 and 4	–1.02		–0.75	
V_{OL}	Low-level output voltage	DOUT, $\overline{\text{DOUT}}$, CLK, $\overline{\text{CLK}}$	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	V_{CC} –1.85		V_{CC} –1.62	V
		DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V,	See Notes 2 and 4	–1.81		–1.58	
V_{IK}	Input clamp voltage	INDIS	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
I_I	Input current	INDIS	V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
I_{IH}	High-level input current	DIN, $\overline{\text{DIN}}$, DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V,	V_I = 4.45 V			50	µA
I_{IL}	Low-level input current	DIN, $\overline{\text{DIN}}$, DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V,	V_I = 3.35 V			50	µA
I_{CC}	Supply current		V_{CC} = 5.25 V, Outputs open	f_i = 155.52 Mbit/s,		71	100	mA
			V_{CC} = 5.25 V, See Note 5	f_i = 155.52 Mbit/s,		112	150	mA

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. These outputs are terminated through a 50-Ω resistor to V_{CC} –2 V.
4. These outputs are terminated through a 50-Ω resistor to –2 V.
5. DOUT, $\overline{\text{DOUT}}$, CLK, and $\overline{\text{CLK}}$ are each terminated with a 50-Ω resistor to V_{CC} –2 V. DATAOUT and $\overline{\text{DATAOUT}}$ are each terminated with a 50-Ω resistor to –2 V.

operating characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

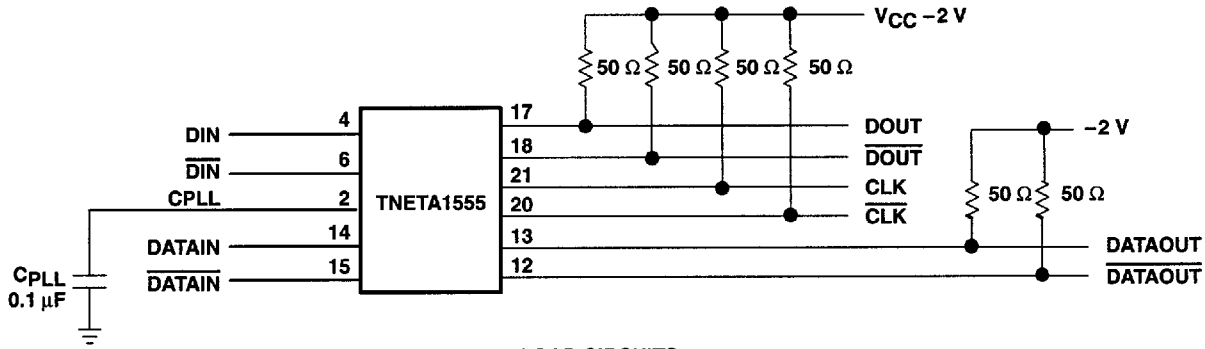
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Acquisition time	See Note 6	C_{PLL} = 330 pF		1		ms
		C_{PLL} = 0.1 µF		3		
Deviation of clock sampling point, t_{csp}	See Figure 1		–800		800	ps
RMS jitter, recovered clock	See Note 7			1.5°	4°	°RMS
Input data rate				155.52		Mb/s
Duty cycle, recovered clock	See Note 3		45%		55%	
Maximum number of consecutive bits (1 or 0) in input data stream	See Note 8		100	450		

NOTES: 3. These outputs are terminated through a 50-Ω resistor to V_{CC} –2 V.
6. Acquisition time is the time required to achieve a valid clock output while applying a 2^7 –1 pseudo-random bit sequence.
7. RMS jitter is measured with a 2^{31} –1 pseudo-random bit sequence.
8. This measurement is made with a 2^{13} –1 pseudo-random bit sequence with string substitution.

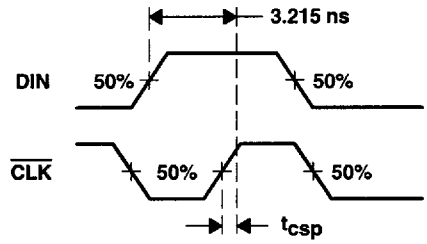
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	DATAIN or $\overline{\text{DATAIN}}$	DATAOUT or $\overline{\text{DATAOUT}}$	1.5	4.5	ns
t_{PHL}	DATAIN or $\overline{\text{DATAIN}}$	DATAOUT or $\overline{\text{DATAOUT}}$	1.5	4.5	ns

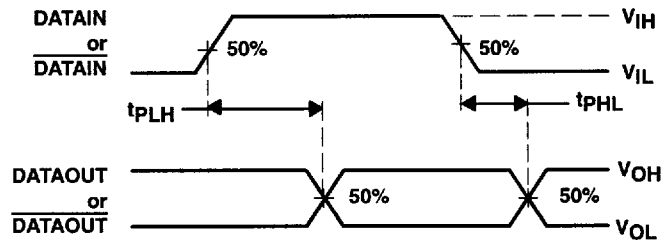
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUITS



VOLTAGE WAVEFORMS
OUTPUT CLOCK AND DATA TIMING



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Figure 1. Load Circuits and Voltage Waveforms

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APPLICATION INFORMATION

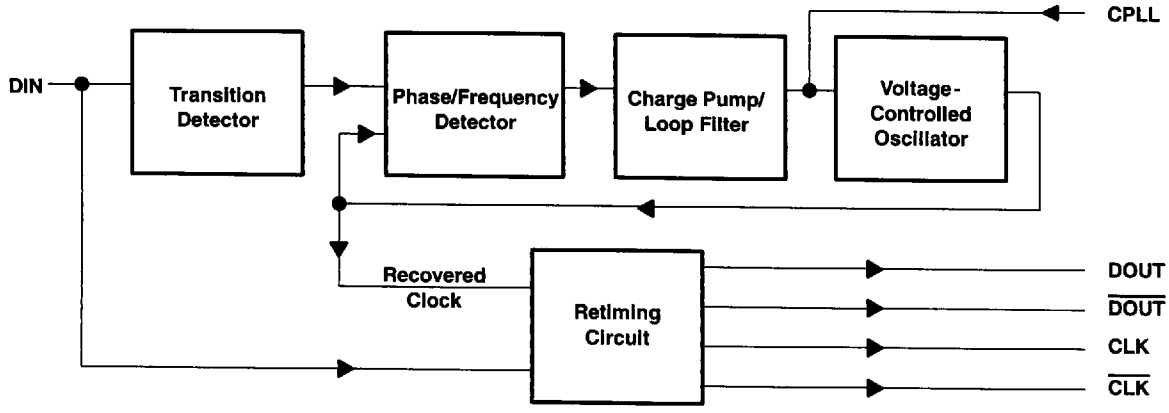
introduction

The TNETA1555 provides clock recovery and data retiming on a nonreturn to zero (NRZ) serial-input data stream. The device uses an analog phase-locked loop (APLL) with an integrated voltage controlled oscillator (VCO) to recover the imbedded clock signal from incoming data. A loop-filter capacitor is the only external component required for the proper operation of the device. The TNETA1555 is designed for operation with a 155.52-Mbit/s serial-input data stream. The device has pseudo-ECL compatible inputs and outputs and operates from a single 5-V supply. Pseudo-ECL levels are referenced to 5 V instead of ground.

Since the incoming 155.52-Mbit/s serial-input data stream does not contain a 155.52-MHz frequency component, a transition detector, shown on the clock-recovery block diagram, is used as a frequency doubler to generate this frequency. The output of the transition detector is passed to a phase/frequency detector where it is compared to the output of the VCO. The phase/frequency detector is actually comprised of two circuits. One circuit provides a coarse frequency-detection capability and a second provides a finer phase adjustment. The phase/frequency detector compares the signal from the transition detector to the VCO output and generates signals to either increase or decrease the VCO frequency, depending upon whether the VCO frequency is less than or greater than the frequency of the signal from the transition detector. The up/down pulses are sent to the charge pump/loop filter for conversion to a bias voltage that sets the VCO output frequency.

The process of comparing the input signal frequency and the VCO output frequency is continuous and eventually results in the VCO output frequency equaling the frequency of the input signal. The device also allows the VCO output to react to changes in the input signal due to jitter. The recovered clock output is sent from the VCO to the retiming circuit where the input data is retimed to the recovered clock. The retiming circuit centers the output clock in the middle of the output data.

clock-recovery block diagram



performance measurements

Measuring the performance of a clock-recovery circuit involves determining how well the circuit operates in the presence of jitter. Jitter is defined as the short-term variations of digital signals significant instants from their ideal positions in time.† For testing purposes, jitter is usually generated by modulating a digital data sequence with a sinusoidal waveform of a known frequency. This results in a digital data stream where the widths of the individual data pulses vary with time. The amount of pulse-width variation can be changed by altering the frequency and amplitude of the modulating signal, which changes the amount of jitter in the data stream. The following paragraphs describe the test results obtained from the TNETA1555 for various performance measurements.

† Bellcore technical reference TR-TSY-000499 Issue 3, December 1989, page 7-1.

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RMS jitter

This test provides a measure of the internal jitter performance of the clock-recovery circuit. A data stream with very low jitter (all data generators have a small amount of jitter) is input to the clock-recovery device, and the jitter of the recovered clock is measured. A $2^{31}-1$ pseudo-random bit sequence (PRBS) is used for the input data stream. For this test, the worst-case jitter performance was measured with V_{CC} = 4.75 V at an operating free-air temperature of 85°C. Table 1 summarizes these test results.

Table 1. Worst-Case RMS Jitter Measurement, V_{CC} = 4.75 V, T_A = 85°C

Device No.	1	2	3	4	5	6	7	8	9
Jitter (° RMS)	3.5	3.2	3.5	3.3	3.1	3.5	3.1	3.0	3.4

jitter tolerance

Jitter tolerance is a measure of the ability of the clock-recovery circuit to tolerate an input signal without experiencing a bit error. For this test, the Bellcore SONET category II jitter-tolerance mask was used (Bellcore specification TR-NWT-000253). The worst-case performance was measured with V_{CC} = 5.25 V at an operating free-air temperature of 85°C. Table 2 and Figure 2 show the results of this test.

Table 2. Jitter Tolerance Values Used in the Graph of Figure 2

Frequency H_Z	Bellcore	TNETA1555
10	15	N.A.
30	15	N.A.
300	1.5	10
1k	1.5	10
2k	1.5	10
5k	0.81	10
10k	0.3	1
20k	0.15	1
50k	0.15	1
100k	0.15	0.658
200k	0.15	0.382
500k	0.15	0.34
1M	0.15	0.536
2M	0.15	0.515
3.5M	0.15	0.486
4M	0.15	0.493

APPLICATION INFORMATION

jitter tolerance (continued)

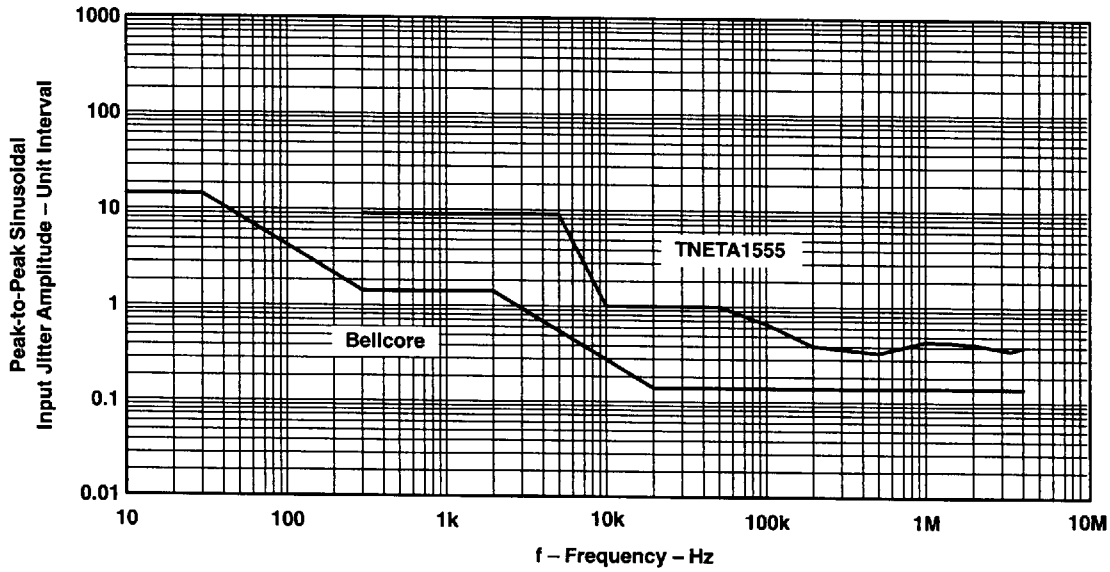


Figure 2. Jitter Tolerance (Worst Case)

transitionless bit periods

The SONET/SDH specifications do not use a line code that limits the number of transitionless bit periods in a bit stream to a specific number. Instead, a scrambler is used to provide some randomization of the line signal. As long as the output data stream does not match the output of the scrambler, this technique works fairly well. However, it is possible for the scrambled data stream to contain a large number of transitionless bit periods, depending upon the data being transmitted. It is important that the clock-recovery device handle large numbers of transitionless bit periods without causing a bit error. Figures 3 and 4 show the results of tests conducted on the TNETA1555 for transitionless bit periods. The y-axis shows the number of transitionless bit periods that the devices can accept before a bit error is recorded on the bit-error rate tester.

APPLICATION INFORMATION

transitionless bit periods (continued)

MAXIMUM NUMBER OF HIGH BITS WITHOUT A BIT ERROR

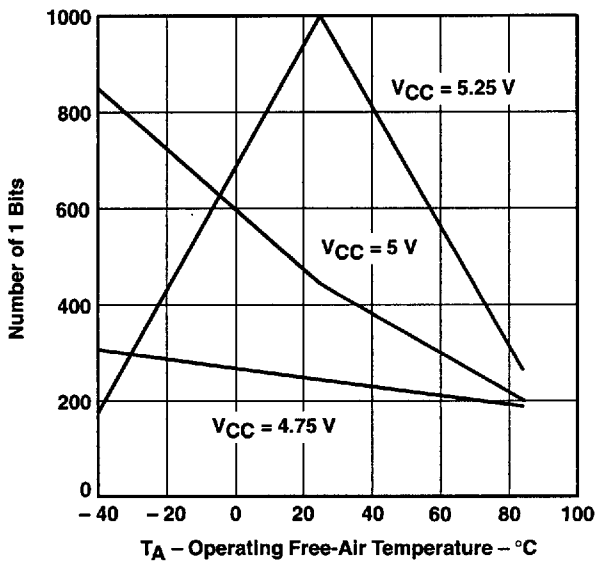


Figure 3

MAXIMUM NUMBER OF LOW BITS WITHOUT A BIT ERROR

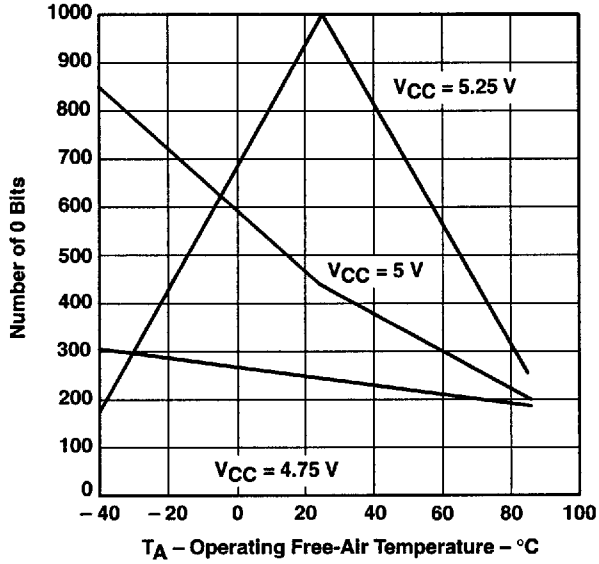


Figure 4

jitter transfer (peaking and bandwidth)

SONET/SDH regenerator interfaces are required to meet jitter-transfer requirements. Jitter transfer is the ratio of measured output jitter to applied input jitter, and it is measured in decibels. Meeting the jitter-transfer requirement in SONET/SDH regenerators requires either a clock-recovery circuit with a voltage-controlled crystal oscillator (VCXO) or a similar technique that provides extremely low jitter. The TNETA1555 provides a typical jitter-transfer bandwidth of approximately 2 MHz. This is where the device begins to attenuate the input jitter so that the output jitter is less than the input jitter. The device exhibits minimal jitter peaking when a capacitor of approximately 0.1 μF is used in the loop filter. The peaking is less than 0.3 dB, which is the resolution of the test equipment used to measure this parameter.

external connections

loop-filter capacitor

The capacitor for the loop filter is connected from terminal 2 of the TNETA1555 to ground. It is recommended that a 0.1-μF chip capacitor be used. A smaller capacitor reduces the amount of acquisition time required for the device to lock on to the input data stream while it increases the amount of jitter peaking that can occur. A larger capacitor results in a longer acquisition time and does not provide any noticeable increase in jitter performance.

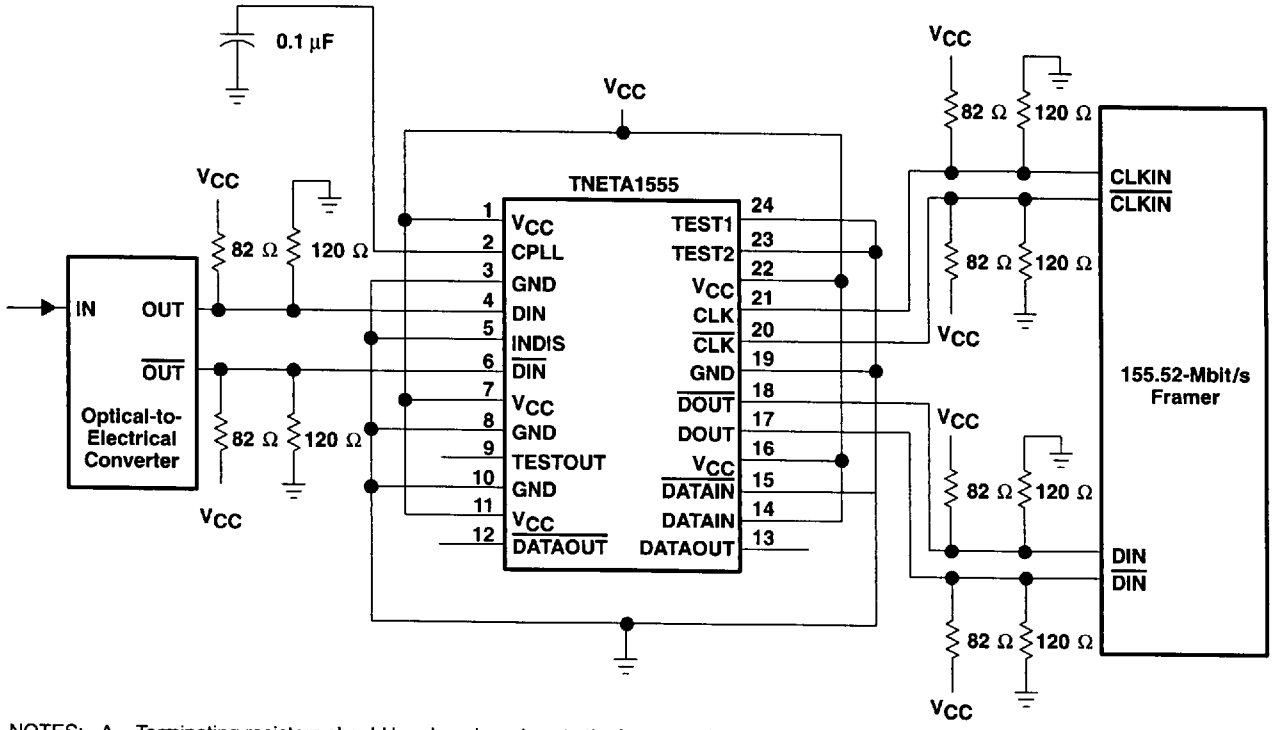
signal connections

Figure 5 shows a typical connection between the TNETA1555, an optical-to-electrical converter, and a framer device. The TNETA1555 accepts pseudo-ECL compatible signals at the serial data inputs DIN and $\overline{\text{DIN}}$. The retimed pseudo-ECL clock outputs are provided at outputs $\overline{\text{CLK}}$ and CLK. The pseudo-ECL inputs and outputs require a 50-Ω termination to V_{CC} –2 V (or a Thevenin equivalent). The Thevenin equivalent circuit consists of an 82-Ω resistor to V_{CC} and 120-Ω resistor to ground.

APPLICATION INFORMATION

signal connections (continued)

A separate pseudo-ECL to ECL converter is also provided on the TNETA1555. The pseudo-ECL inputs require a 50-Ω to V_{CC} –2 V termination (or a Thevenin equivalent) and the ECL outputs require a 50-Ω to –2 V termination (or its equivalent). Figure 6 shows the external connections for the pseudo-ECL to ECL converter.



NOTES: A. Terminating resistors should be placed as close to the input terminal as possible.
B. The 0.1-µF bypass capacitors should be connected from the V_{CC} terminals to ground.

Figure 5. TNETA1555 External Connections (PECL-to-ECL converter not used)

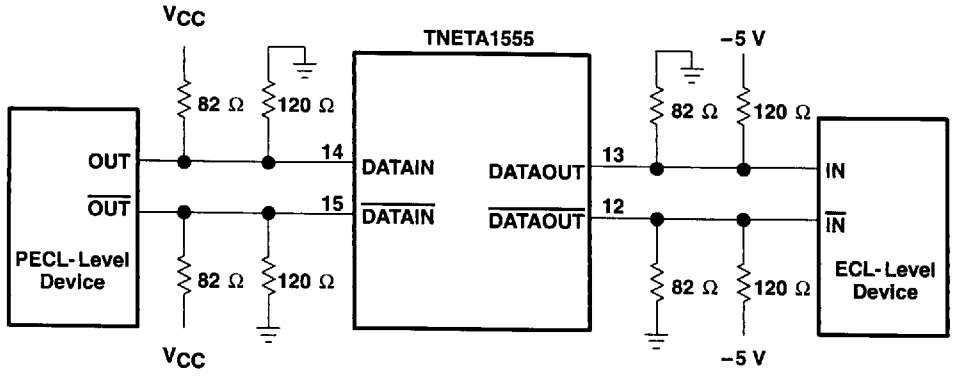


Figure 6. External Connections for PECL-to-ECL Converter

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