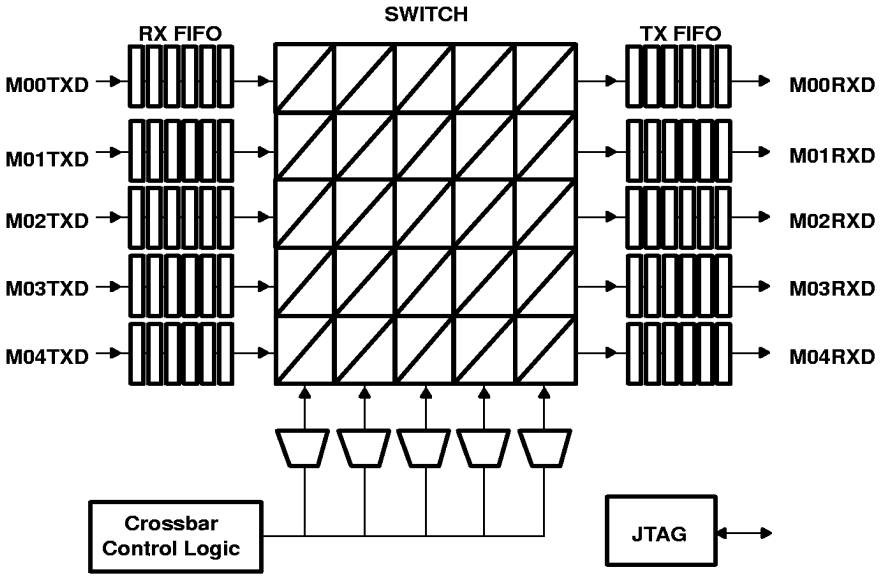
- 5-Port Gigabit Crossbar Switch
- IEEE Std 802.3 Compliant With 1000-Mbit/s GMII-Compatible Interface
- Internal 32-bit Bus Provides up to 3 Gbit/s of Internal Bandwidth Per Port
- Frame-Based Round-Robin Arbitration for Maximum Fairness and Throughput
- Support for TNETX4020/TNETX4090 Extended-Port Pretagging
- 8 kbytes of Internal FIFO RAM Per Port (4 kbytes for Transmit and 4 kbytes for Receive)
- Back-Pressure Flow Control Per Port
- Fabricated in 2.5-/3.3-V Low-Voltage Technology
- Electrostatic-Discharge Human-Body Model Protection (2 kV per JEDEC JESD22–A114A)
- IEEE Std 1149.1 (JTAG) Interface (3.3-V Signals)
- Packaged in 160-Pin Plastic Quad Flatpack

description

The TNETX5105 is a 5-port 1000-Mbit/s non-blocking Ethernet crossbar switch, which provides a cost-effective method of building a high-port-density-switching solution. The device supports extended-port pretagging for glueless connectivity and a direct interface to the Texas Instruments (TI™) TNETX4090, TNETX4020, and future switch offerings.

The TNETX5105 provides five 1000-Mbit/s gigabit media independent interface (GMII)-compatible interfaces. The internal 32-bit bus provides up to 3 Gbit/s of bandwidth per port; this allows designers to build a non-blocking system. The TNETEX5105 combines full-duplex flow control and round-robin arbitration to prevent frame loss and to ensure that no port suffers from head-of-line blocking.

functional block diagram



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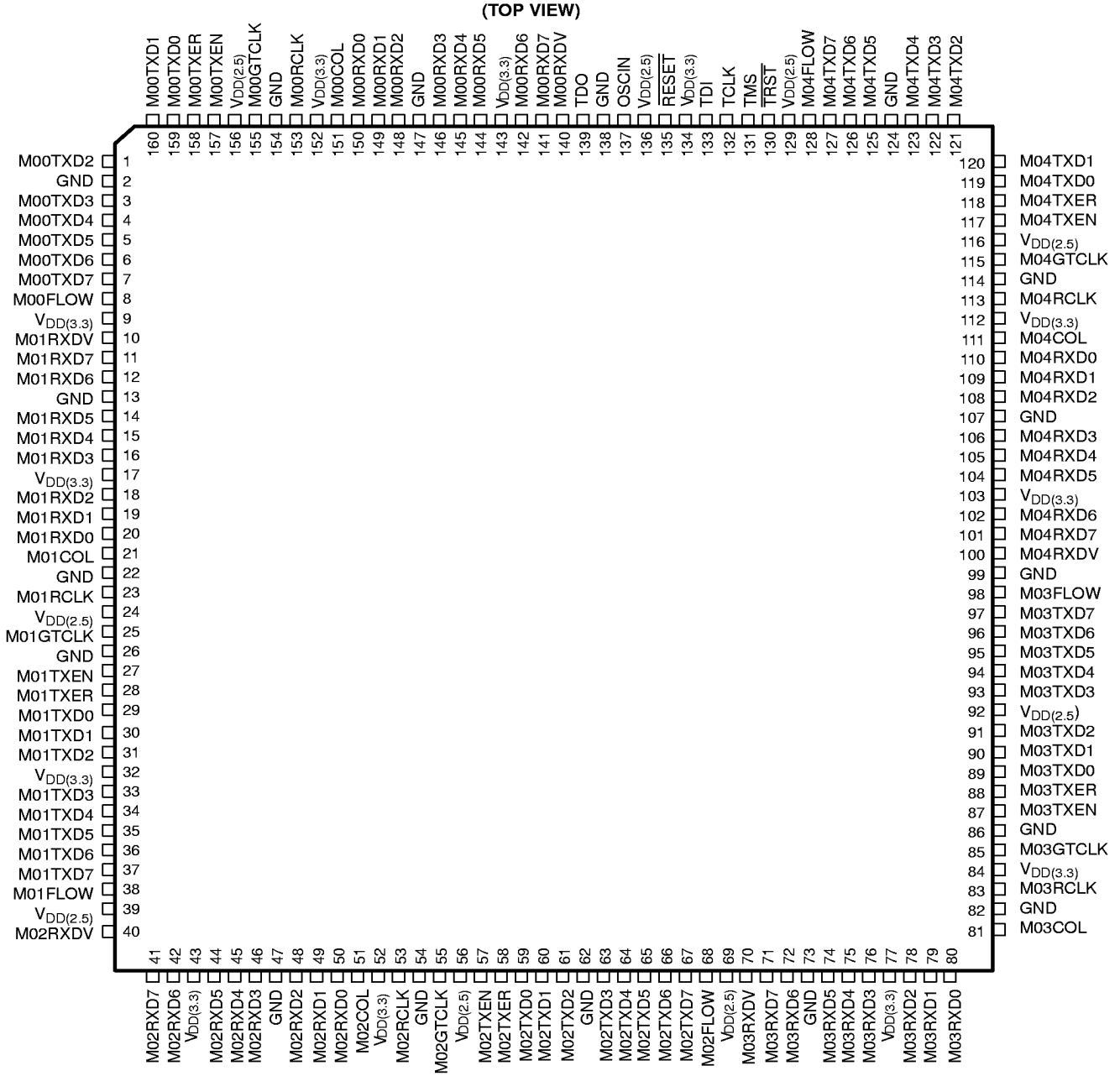
PCE PACKAGE
(TOP VIEW)



NC – No internal connection

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Terminal Functions

1000-Mbit/s MAC interface

TERMINAL NAME	TERMINAL NO.	I/O	INTERNAL RESISTOR†	DESCRIPTION
M00COL M01COL M02COL M03COL M04COL	151 21 51 81 111	O	None	Collision. When the amount of available RX FIFO memory is less than 1536 bytes, this signal is asserted high. These signals are used to stop the attached device from transmitting additional frames.
M00GTCLK M01GTCLK M02GTCLK M03GTCLK M04GTCLK	155 25 55 85 115	I	Pullup	Transmit clock. 125-MHz transmit clock input from attached device.
M00RCLK M01RCLK M02RCLK M03RCLK M04RCLK	153 23 53 83 113	O	None	Receive clock. 125-MHz receive clock source to the attached device.

† Internal resistors pull signals to known values. The system designer should determine if additional pullups or pulldowns are required in the system.

1000-Mbit/s MAC interface (continued)

TERMINAL NAME	TERMINAL NO.	I/O	INTERNAL RESISTOR†	DESCRIPTION
M00RXD7	141	O	None	Receive data. Byte receive data to the attached device. When MxxRXDV is asserted high, these signals carry valid receive data. Data on these signals is synchronous to MxxRCLK.
M00RXD6	142			
M00RXD5	144			
M00RXD4	145			
M00RXD3	146			
M00RXD2	148			
M00RXD1	149			
M00RXD0	150			
M01RXD7	11			
M01RXD6	12			
M01RXD5	14			
M01RXD4	15			
M01RXD3	16			
M01RXD2	18			
M01RXD1	19			
M01RXD0	20			
M02RXD7	41			
M02RXD6	42			
M02RXD5	44			
M02RXD4	45			
M02RXD3	46			
M02RXD2	48			
M02RXD1	49			
M02RXD0	50			
M03RXD7	71			
M03RXD6	72			
M03RXD5	74			
M03RXD4	75			
M03RXD3	76			
M03RXD2	78			
M03RXD1	79			
M03RXD0	80			
M04RXD7	101			
M04RXD6	102			
M04RXD5	104			
M04RXD4	105			
M04RXD3	106			
M04RXD2	108			
M04RXD1	109			
M04RXD0	110			
M00RXDV	140	O	None	Receive data valid. MxxRXDV (when high) indicates data on MxxRXD7–MxxRXD0 is valid. This signal is synchronous to MxxRCLK.
M01RXDV	10			
M02RXDV	40			
M03RXDV	70			
M04RXDV	100			

† Internal resistors pull signals to known values. The system designer should determine if additional pullups or pulldowns are required in the system.

1000-Mbit/s MAC interface (continued)

TERMINAL NAME	TERMINAL NO.	I/O	INTERNAL RESISTOR†	DESCRIPTION
M00TXD7	7	I	Pullup	Transmit data. Byte transmit data. When MxxTXEN is asserted high, these signals carry valid transmit data to the TNETX5105. Data on these signals is synchronous to MxxGTCLK.
M00TXD6	6			
M00TXD5	5			
M00TXD4	4			
M00TXD3	3			
M00TXD2	1			
M00TXD1	160			
M00TXD0	159			
M01TXD7	37			
M01TXD6	36			
M01TXD5	35			
M01TXD4	34			
M01TXD3	33			
M01TXD2	31			
M01TXD1	30			
M01TXD0	29			
M02TXD7	67			
M02TXD6	66			
M02TXD5	65			
M02TXD4	64			
M02TXD3	63			
M02TXD2	61			
M02TXD1	60			
M02TXD0	59			
M03TXD7	97			
M03TXD6	96			
M03TXD5	95			
M03TXD4	94			
M03TXD3	93			
M03TXD2	91			
M03TXD1	90			
M03TXD0	89			
M04TXD7	127			
M04TXD6	126			
M04TXD5	125			
M04TXD4	123			
M04TXD3	122			
M04TXD2	121			
M04TXD1	120			
M04TXD0	119			
M00TXEN	157	I	Pulldown	Transmit enable. MxxTXEN (when high) indicates valid transmit data on MxxTXD7–MxxTXD0. This signal is synchronous to MxxGTCLK.
M01TXEN	27			
M02TXEN	57			
M03TXEN	87			
M04TXEN	117			
M00TXER	158	I	Pulldown	Transmit error. MxxTXER allows coding errors to be propagated between the TNETX5105 and attached device. If this signal pulses high, the crossbar discards the current frame. This signal is synchronous to MxxGTCLK.
M01TXER	28			
M02TXER	58			
M03TXER	88			
M04TXER	118			
M00FLOW	8	I	Pulldown	Flow control. Transmission of new frames does not commence if this terminal is asserted high, indicating that the attached device is not able to receive additional data.
M01FLOW	38			
M02FLOW	68			
M03FLOW	98			
M04FLOW	128			

† Internal resistors pull signals to known values. The system designer should determine if additional pullups or pulldowns are required in the system.

IEEE Std 1149.1 (JTAG) interface

TERMINAL NAME	TERMINAL NO.	I/O	INTERNAL RESISTOR†	DESCRIPTION
$\overline{\text{TRST}}$	130	I	Pullup	Test reset. Asynchronous reset of the test-port controller.
TMS	131	I	Pullup	Test mode select. Controls the state of the test-port controller.
TCLK	132	I	Pullup	Test clock. Clocks state information and test data into and out of the device during operation of the test port.
TDI	133	I	Pullup	Test data input. Serially shifts test data and test instructions into the device during operation of the test port.
TDO	139	O	None	Test data output. Serially shifts test data and test instructions out of the device during operation of the test port.

control

TERMINAL NAME	TERMINAL NO.	I/O	INTERNAL RESISTOR†	DESCRIPTION
$\overline{\text{RESET}}$	135	I	None	Device reset. This signal should be asserted low for a minimum of two clock cycles after the power supplies have stabilized. The system clock must be operational while reset is held low.
OSCIN	137	I	Pullup	125-MHz system clock. This terminal is used to clock internal logic.

† Internal resistors pull signals to known values. The system designer should determine if additional pullups or pulldowns are required in the system.

power supply

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	2, 13, 22, 26, 47, 54, 62, 73, 82, 86, 99, 107, 114, 124, 138, 147, 154	Ground. The 0-V reference for the TNETX5105.
$V_{DD(3.3)}$	9, 17, 32, 43, 52, 77, 84, 103, 112, 134, 143, 152	3.3-V supply voltage. Power for the I/Os.
$V_{DD(2.5)}$	24, 39, 56, 69, 92, 116, 129, 136, 156	2.5-V supply voltage. Power for the core.

detailed description

receiver

Each receiver consists of a dribble-down buffer (DDB), 56-bit shift register, 4 kbytes of FIFO, and FIFO control logic. Data is received on the GMII bus through the DDB and aligned before being loaded into the shift register. The FIFO control logic transfers a word of data directly from the shift register to the FIFO. Once the entire frame is received and written to the FIFO, the length of the frame and routing information is written into the first word. This information is used later by the arbiter and transmitter.

The receiver discards any frame when any of the following is true:

- A frame is greater than 1536 bytes in size.
- A frame is less than 1 byte in size.
- The pretag xportvector field is equal to zero.
- TXER is sampled high at any time during frame reception (while TXEN is high)

flow control

If the available FIFO memory shrinks to less than 1536 bytes, the receiver asserts the MxxCOL terminal high, indicating to the connected device that it should stop transmitting until the arbiter frees up additional FIFO memory.

receive frame format (see Figure 1 and Table 1)

The TNETX5105 receives pretag information in eight cycles starting with the first cycle that MxxTXEN is high. The pretag takes the form of a 32-bit value that is divided into 8 nibbles. The nibbles are received on MxxTXD3 through MxxTXD0. The TNETX5105 discards frames that are received with an xportvector field equal to zero.

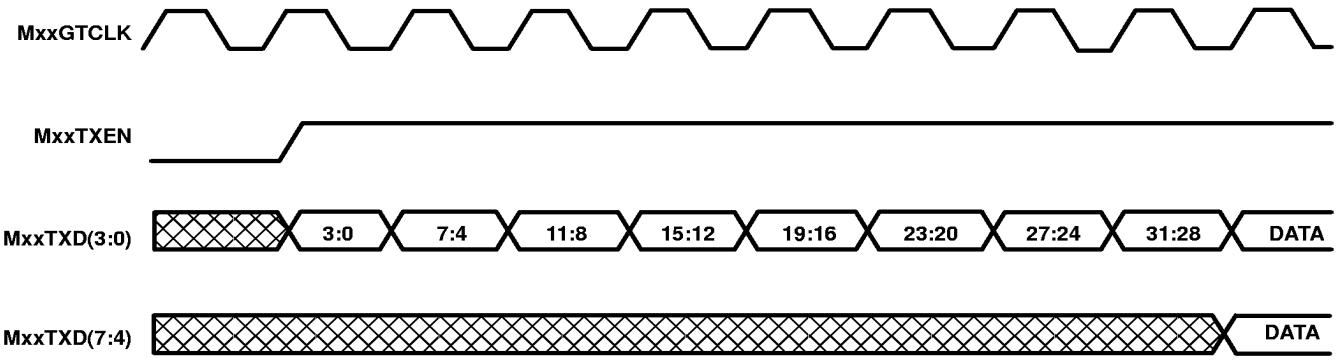

Figure 1. Receive Frame Format

Table 1. Received Pretag Bit Definitions

No.	Name	Functions
31–5	reserved	Reserved. These bits are ignored.
4–0	xportvector	Extended Destination Port Vector. A bit for each TNETX5105 port. A 1 in position *n* indicates the frame is destined for port *n*. Frames received with this field that are equal to zero are discarded. For example, if the pretag = 0xUUUUUU01, the frame is forwarded to port zero (U means undefined or don't care).

transmitter

Like the receiver, the transmitter is heavily pipelined. Each transmitter consists of a 4-kbyte FIFO, FIFO control logic, and an 56-bit shift register. Immediately after the arbiter writes a word of frame data to the FIFO, the data is read from the FIFO, aligned for minimum interpacket spacing, and loaded directly into a shifter register where it waits to be transmitted on the GMII interface.

If the available FIFO memory shrinks to less than 1536 bytes, further writes are prevented and the arbiter does not begin new frame transfers to that port.

If the MxxFLOW terminal is asserted, the transmitter completes the current frame transmission and waits until this terminal is deasserted before initiating the next transmission.

transmit frame format (see Figure 2 and Table 2)

The TNETX5105 provides transmit pretag information for eight cycles, commencing with the first cycle that MxxRXDV is high. The pretag takes the form of a 32-bit value, divided into 8 nibbles, with each nibble being replicated on MxxRXD3 through MxxRXD0 and MxxRXD7 through MxxRXD4.

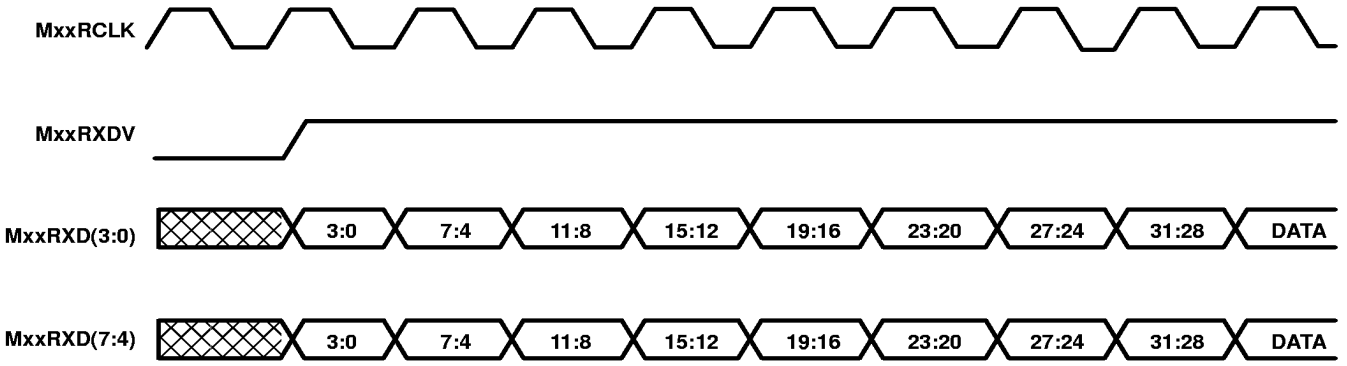

Figure 2. Transmit Frame Format

Table 2. Transmit Pretag Bit Definitions

No.	Name	Functions
31–4	reserved	Reserved. These bits are always zero.
3–0	cportcode	Source Port Code. Cportcode indicates which TNETX5105 port received the frame. Codes 000b through 100b indicate ports 0 through 4, respectively.

arbiter

The arbiter is composed of five major functional blocks as shown in Figure 3: multicast arbiter, destination arbiter, source arbiter, destination transfer machine, and source transfer machine. The arbiter is responsible for ensuring that frames are transferred from source ports to destination ports in a correct and timely manner.

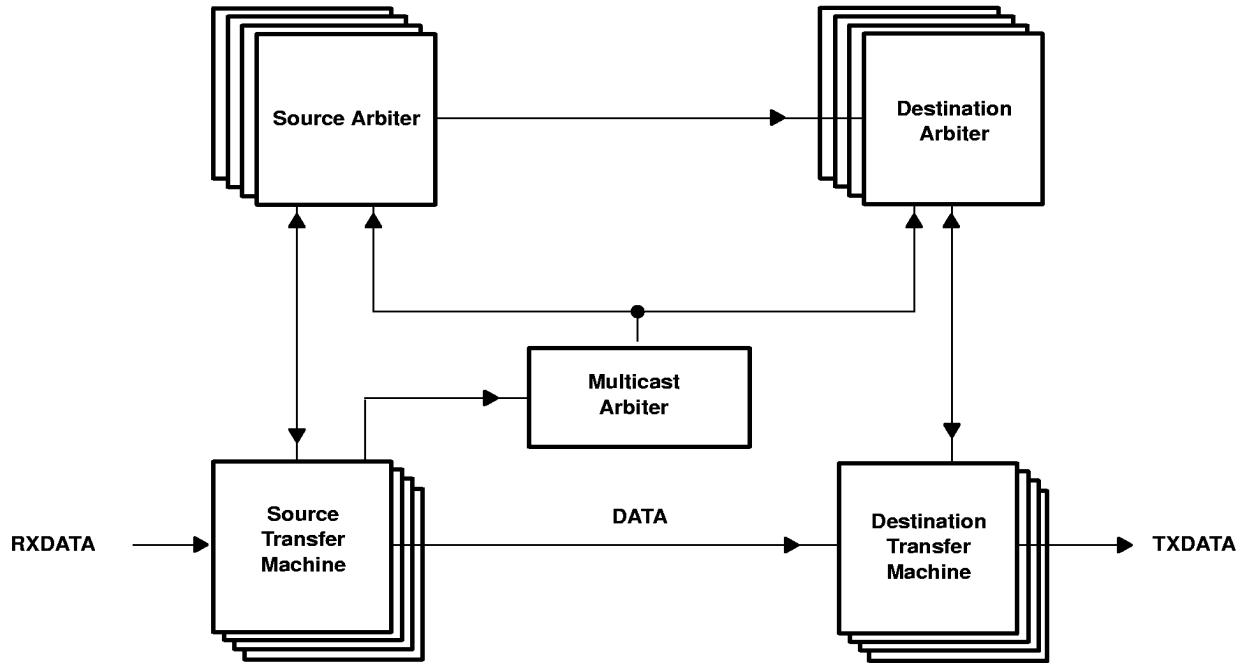

Figure 3. Arbiter Functional Block Diagram

multicast arbiter

The multicast arbiter determines if more than one port has a transfer request, and if so, arbitrates it to potential destination arbiters based on a round-robin scheme. If all ports on the crossbar switch have multicast requests, each port's request is considered in sequential order to ensure that multicast traffic does not create a lock-up condition and halt frame transfer through the crossbar switch. Arbitration of unicast traffic passes through unaffected.

destination arbiter

The destination arbiter receives requests from that multicast arbiter and determines the appropriate source port request to acknowledge.

source arbiter

The source arbiter receives transfer requests from the multicast arbiter and determines when to acknowledge the request, based on acknowledgements from all destination arbiters.

destination transfer machine

The destination transfer machine receives transfer information from the destination arbiter. This information contains the source port for the transfer and the time during which the transfer takes place.

source transfer machine

The source transfer machine is responsible for extracting the source port transfer request and sending it to the multicast arbiter.

JTAG interface

The TNETX3270 is fully IEEE Std 1149.1 compliant. It includes on-chip pullup resistors on the five JTAG terminals to eliminate the need for external resistors. All JTAG inputs and outputs are 3.3-V tolerant.

The following instructions are supported:

- EXTEST, BYPASS, and SAMPLE/PRELOAD
- HIGHZ and IDCODE
- Private (TI uses various private instructions for test purposes.)

The opcodes for the various instructions (6-bit instruction register) are shown in Table 3.

Table 3. JTAG Instruction Opcodes

INSTRUCTION TYPE	INSTRUCTION NAME	JTAG OPCODE
Mandatory	EXTEST	000000
Mandatory	SAMPLE/PRELOAD	000001
Optional	IDCODE	000100
Optional	HIGHZ	000101
Private	TI testing	Others
Mandatory	BYPASS	111111

HIGHZ instruction

When selected, the HIGHZ instruction causes all outputs and bidirectional signals to become high impedance. All pullup and pulldown resistors are disabled.

The JTAG interface has no specific timing requirements, but it works satisfactorily with TCLK running at up to 10 MHz. (Successful operation at higher frequencies may be possible, but is not recommended).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD(2.5)}$ (see Note 1) . . . . . –0.5 V to 2.7 V
Supply voltage range, $V_{DD(3.3)}$ (see Note 1) . . . . . –0.5 V to 3.6 V
Input voltage range, V_I . . . . . –0.5 V to $V_{DD(3.3)}$ + 0.4 V
Output voltage range, V_O . . . . . –0.5 V to $V_{DD(2.5)}$ + 0.5 V
Thermal impedance, junction-to-ambient package, $Z_{\theta JA}$: Airflow = 0 . . . . . 30°C/W
Airflow = 100 ft/min . . . . . 29°C/W
Thermal impedance, junction-to-case package, $Z_{\theta JC}$ . . . . . 15°C/W
Operating case temperature range, T_C . . . . . 0°C to 95°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
$V_{DD(2.5)}$	Supply voltage		2.3	2.5	2.7	V
$V_{DD(3.3)}$	Supply voltage		3	3.3	3.6	V
$I_{DD(2.5)}$	Supply current	$V_{DD(2.5)}$ = max, f = 125 MHz			600	mA
$I_{DD(3.3)}$	Supply current	$V_{DD(3.3)}$ = max, f = 125 MHz			180	mA
V_I	Input voltage		0		$V_{DD(3.3)}$	V
V_O	Output voltage		0		$V_{DD(3.3)}$	V
V_{IH}	High-level input voltage		2		$V_{DD(3.3)}$	V
V_{IL}	Low-level input voltage (see Note 2)		0		0.8	V
I_{OH}	High-level output current				–4	mA
I_{OL}	Low-level output current				4	mA

NOTE 2: The algebraic convention, in which the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	$V_{DD(3.3)}$–0.5			V
V_{OL}	Low-level output voltage	I_{OL} = rated			0.5	V
I_{OZ}	High-impedance-state output current	$V_O = V_{DD}$ or GND			±10	µA
I_{IH}	High-level input current	$V_I = V_{IH}$			1	µA
I_{IL}	Low-level input current	$V_I = V_{IL}$			–1	µA
I_{PU}, I_{PD}	Current source used as pullup and pulldown on I/O pins			50		µA
C_i	Capacitance, input			6		pF
C_o	Capacitance, output			6		pF

timing requirements

GMII

Figures 4–5 show the timing for the 1000-Mbit/s GMII when operating at 1000 Mbit/s.

MxxTXD7–MxxTXD0 is driven by the external device on the falling edge of MxxTCLK. MxxTXD7–MxxTXD0 timing must be met during clock periods in which MxxTXEN is asserted. MxxTXEN is asserted and deasserted by the external device on the falling edge of MxxGTCLK.

GMII receive (see Figure 4)

NO.			MIN	MAX	UNIT
1	$t_{su(MxxTXD)}$	Setup time, MxxTXD7–MxxTXD0 valid before MxxGTCLK↑	2		ns
1	$t_{su(MxxTXEN)}$	Setup time, MxxTXEN valid before MxxGTCLK↑	2		ns
1	$t_{su(MxxTXER)}$	Setup time, MxxTXER valid before MxxGTCLK↑	2		ns
2	$t_{h(MxxTXD)}$	Hold time, MxxTXD7–MxxTXD0 valid after MxxGTCLK↑	1		ns
2	$t_{h(MxxTXEN)}$	Hold time, MxxTXEN valid after MxxGTCLK↑	1		ns
2	$t_{h(MxxTXER)}$	Hold time, MxxTXER valid after MxxGTCLK↑	1		ns

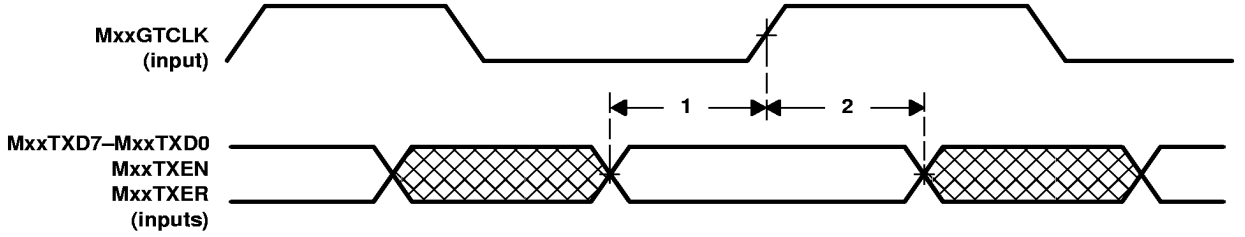

Figure 4. GMII Receive

operating characteristics over recommended operating conditions

GMII transmit (see Figure 5)

NO.			MIN	MAX	UNIT
1	$t_{d(MxxRXD)}$	Delay time, from MxxRCLK↑ to MxxRXD3–MxxRXD0 valid	1.5	4.5	ns
1	$t_{d(MxxRXDV)}$	Delay time, from MxxRCLK↑ to MxxRXDV valid	1.5	4.5	ns

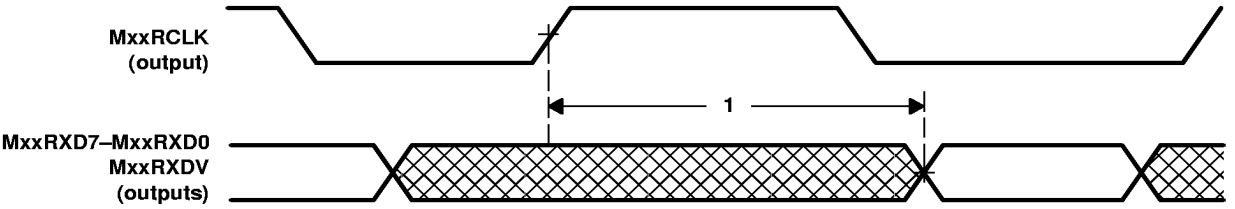

Figure 5. GMII Transmit

timing requirements (see Figure 6)

power-up, OSCIN, MxxGTCLK, MxxRCLK, and $\overline{\text{RESET}}$

NO.			MIN	NOM	MAX	UNIT
		Frequency drift, OSCIN/MxxGTCLK/MxxRCLK clocks			±100	ppm
1	$t_{c(OSCIN)}$	Cycle time, OSCIN/MxxGTCLK/MxxRCLK		8		ns
2	$t_{w(OSCINL)}$	Pulse duration, OSCIN/MxxGTCLK/MxxRCLK low	2.5			ns
3	$t_{w(OSCINH)}$	Pulse duration, OSCIN/MxxGTCLK/MxxRCLK high	2.5			ns
4	$t_{w(RESET)}$	Pulse duration, $\overline{\text{RESET}}$ low	32			ns
5	$t_{su(RESET)}$	Setup time, $\overline{\text{RESET}}$ low before OSCIN↑/MxxGTCLK↑/MxxRCLK↑	7			ns
6	$t_{h(RESET)}$	Hold time, $\overline{\text{RESET}}$ low after OSCIN↑/MxxGTCLK↑/MxxRCLK↑	3			ns
7	$t_{d(OSCIN)}$	Delay time, from OSCIN invalid to OSCIN valid (stable)	25			ms
8	$t_{d(RESET)}$	Delay time, from OSCIN/MxxGTCLK/MxxRCLK stable to $\overline{\text{RESET}}$↑	100			µs
9	$t_{t(OSCIN)}$	Transition time, OSCIN/MxxGTCLK/MxxRCLK rise and fall			1	ns

$\overline{\text{RESET}}$ must be held low at least 25 ms after both power supplies are stable and OSCIN/MxxGTCLK/MxxRCLK has reached its stable operating frequency. $\overline{\text{RESET}}$ can be set to 0 for a minimum of 200 µs to reset the device.

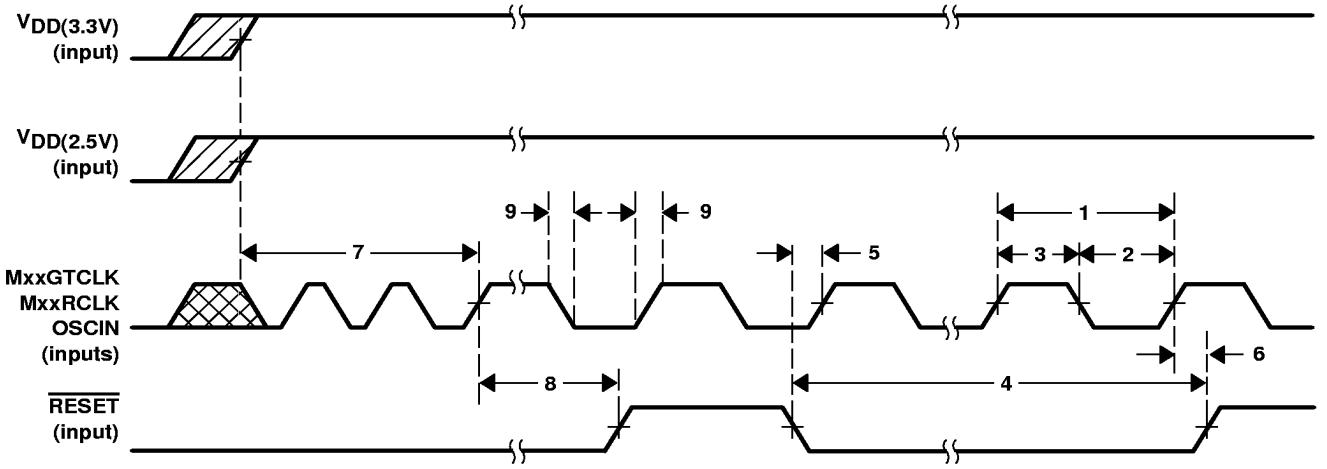

Figure 6. Power-Up, OSCIN, MxxGTCLK, MxxRCLK, and $\overline{\text{RESET}}$ Timing

PARAMETER MEASUREMENT INFORMATION

The following load circuits and voltage waveforms show the conditions used for measuring switching characteristics. Test points are illustrated schematically on the load circuits. Reference points are plotted on the voltage waveforms.

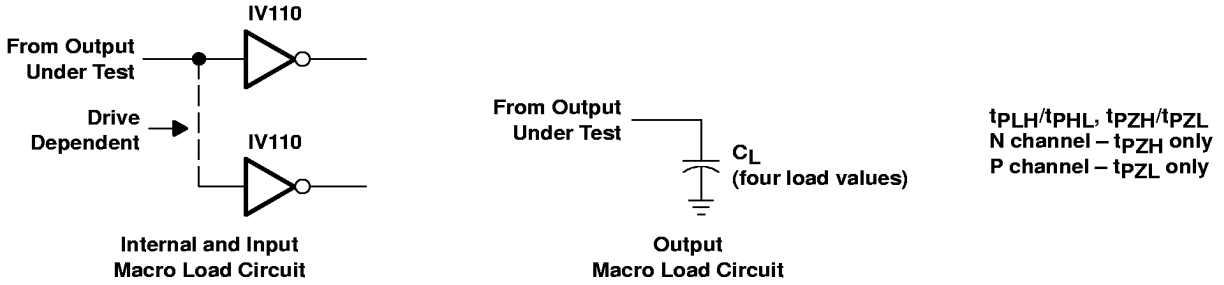

Figure 7. Loading for Active Transitions

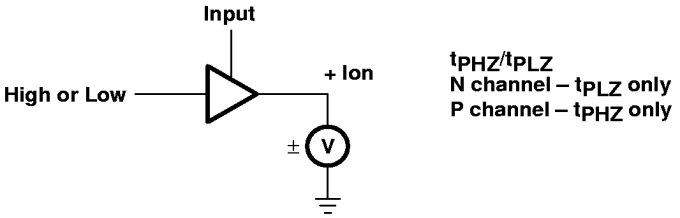

Figure 8. Loading for High-Impedance Transitions

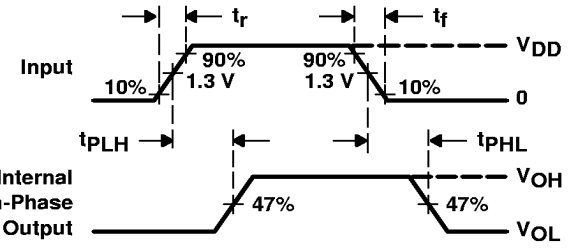

Figure 9. TTL Input Macro Propagation-Delay-Time Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

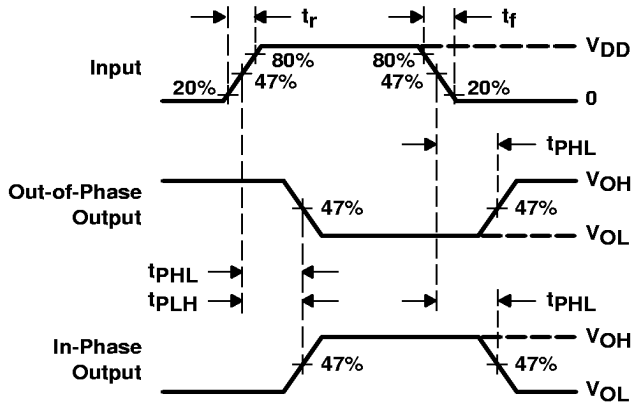


Figure 10. Internal Push/Pull Output Propagation-Delay-Time Voltage Waveforms

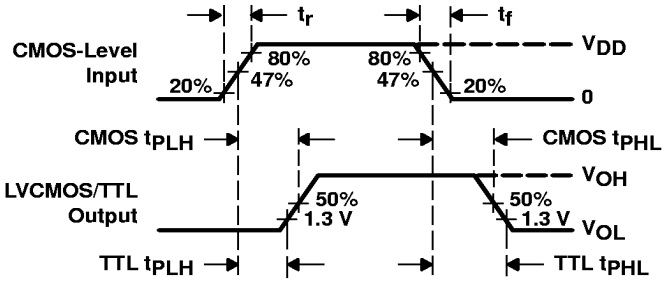


Figure 11. TTL Output Macro Propagation-Delay-Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

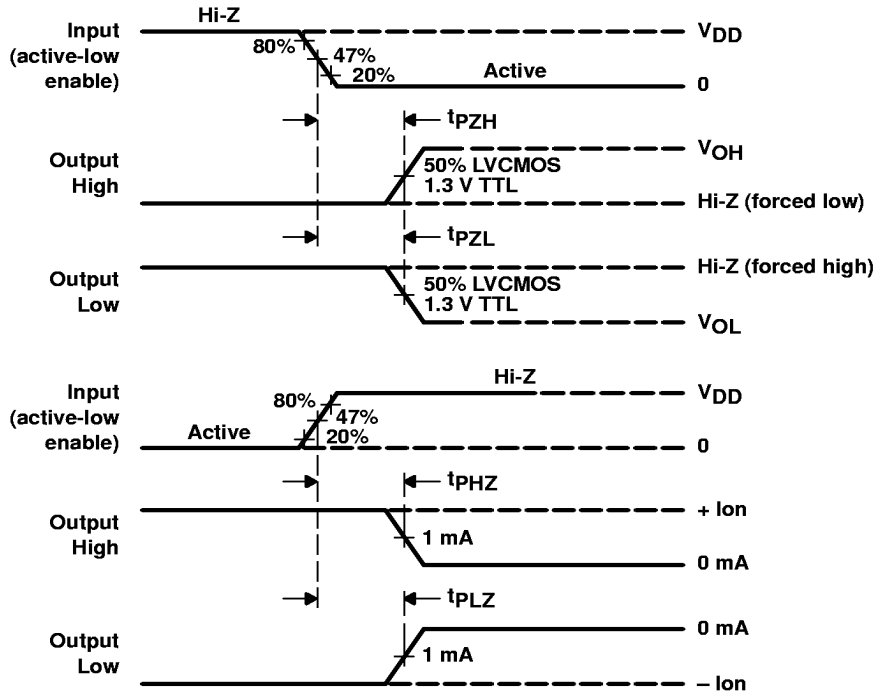


Figure 12. TTL 3-State Output Disable and Enable Voltage Waveforms

APPLICATION INFORMATION

Figure 13 illustrates a 0/24/2 design. This design has 24 10/100 Mbit/s ports and two 1 Gbit/s ports. All of these are interconnected via the TNETX5105. The crossbar switch provides a non-blocking architecture.

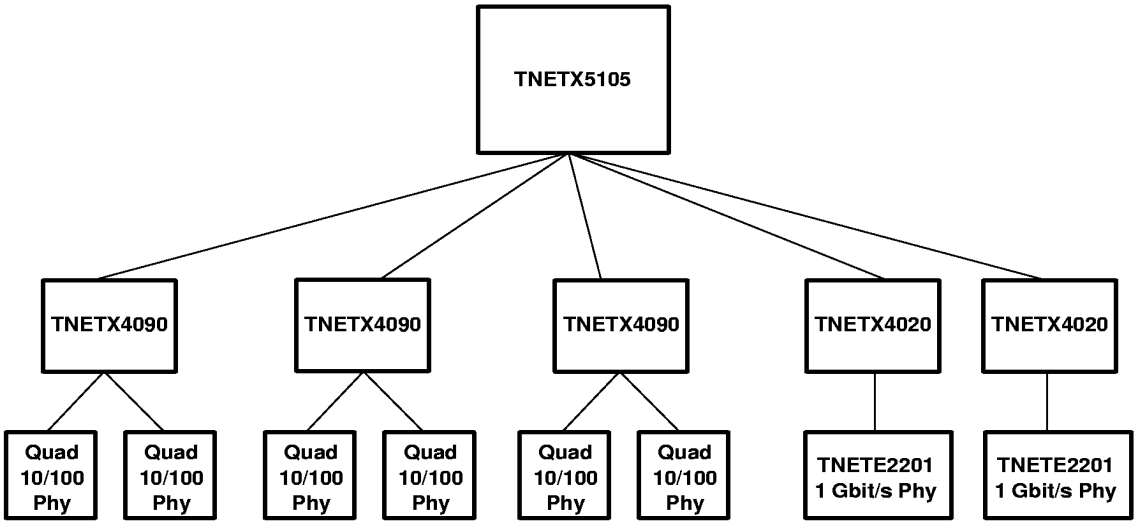


Figure 13. TNETX5105 Non-Blocking System

Figure 14 illustrates a 0/0/5 design. This design has five 1-Gbit/s ports. All of these are interconnected via the TNETX5105. The crossbar switch provides a non-blocking architecture.

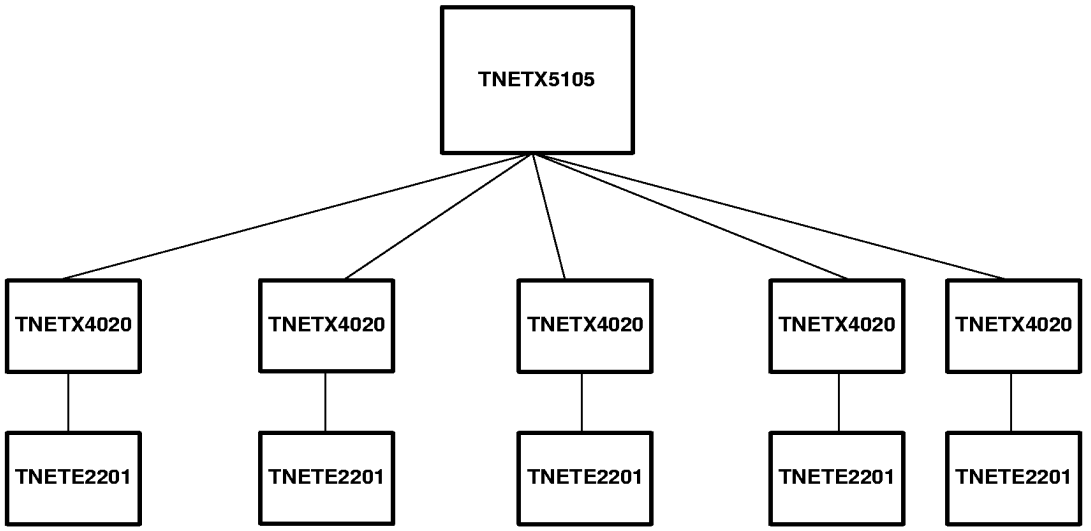
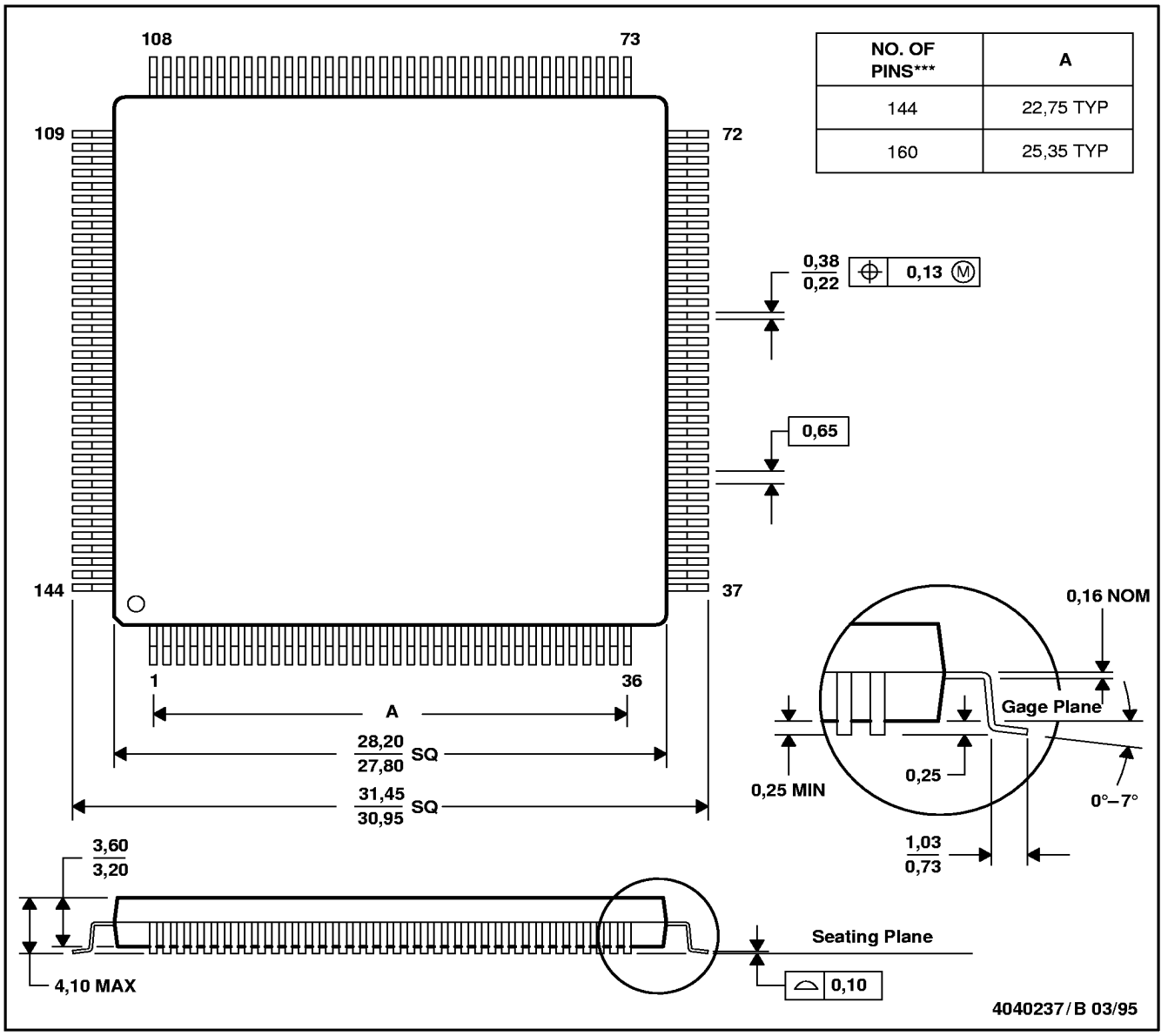


Figure 14. Five 1-Gbit/s Ports Via the Non-Blocking TNETX5105

MECHANICAL DATA

PCE (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

144 PIN SHOWN



NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat spreader (HSP)
D. Falls within JEDEC MS-022
E. The 144 PCE is identical to the 160 PCE except that four leads per corner are removed.

TEXAS INSTRUMENTS
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