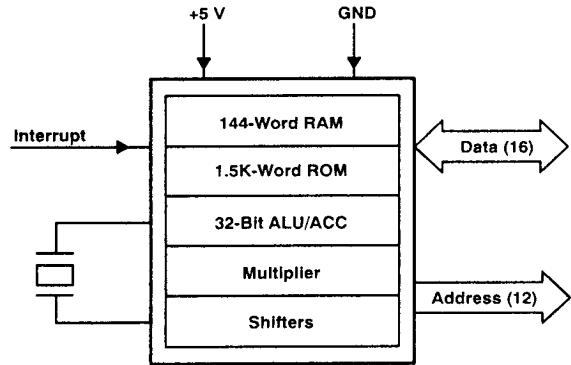


TMS320C10, TMS320C10-14, TMS320C10-25 DIGITAL SIGNAL PROCESSORS

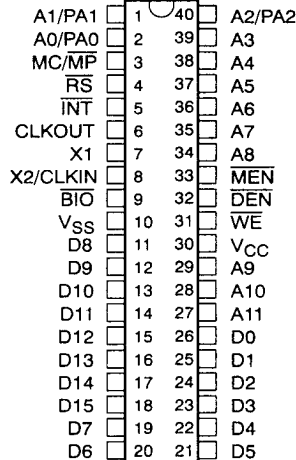
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Key Features: TMS320C10

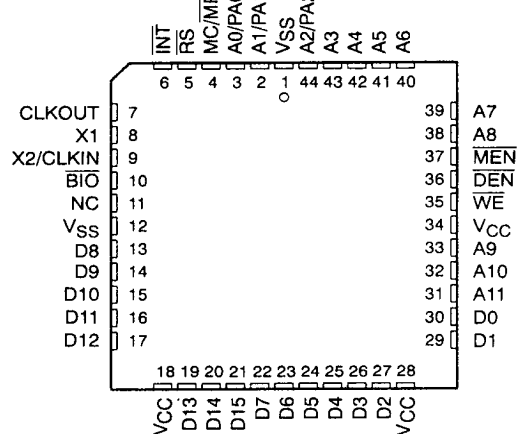
- Instruction Cycle Timing
 - 160-ns (TMS320C10-25)
 - 200-ns (TMS320C10)
 - 280-ns (TMS320C10-14)
- 144 Words of On-Chip Data RAM
- 1.5K Words On-Chip Program ROM
- External Memory Expansion up to 4K Words at Full Speed
- 16 × 16-Bit Multiplier With 32-Bit Product
- 0 to 16-Bit Barrel Shifter
- On-Chip Clock Oscillator
- Device Packaging:
 - 40-Pin DIP
 - 44-Lead PLCC
- Single 5-V Supply
- Operating Free-Air Temperature Range
 - ... 0°C to 70°C



TMS320C10
N/JD Package
(Top View)



TMS320C10
FN/FZ Package
(Top View)



TMS320C10, TMS320C10-14, TMS320C10-25 DIGITAL SIGNAL PROCESSORS

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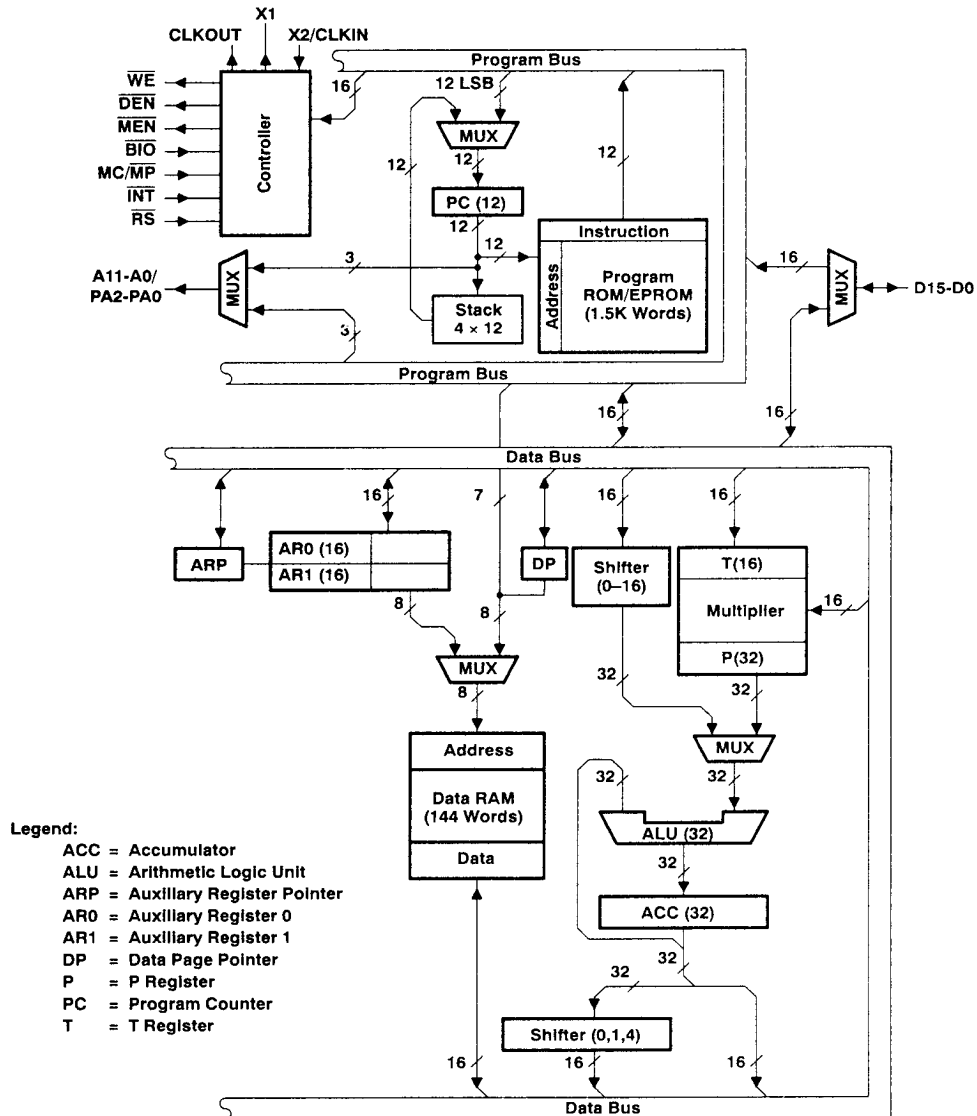
TERMINAL FUNCTIONS

NAME	I/O†	DEFINITION
A11-A0/PA2-PA0	O	External address bus. I/O port address multiplexed over PA2-PA0.
$\overline{\text{BIO}}$	I	External polling input
CLKOUT	O	System clock output, 1/4 crystal/CLKIN frequency
D15-D0	I/O	16-bit parallel data bus
$\overline{\text{DEN}}$	O	Data enable for device input data on D15-D0
$\overline{\text{INT}}$	I	External interrupt input
MC/MP	I	Memory mode select pin. High selects microcomputer mode. Low selects microprocessor mode.
$\overline{\text{MEN}}$	O	Memory enable indicates that D15-D0 will accept external memory instruction.
NC	O	No connection
$\overline{\text{RS}}$	I	Reset for initializing the device
VCC	I	+ 5 V supply
VSS	I	Ground
$\overline{\text{WE}}$	O	Write enable for device output data on D15-D0
X1	O	Crystal output for internal oscillator
X2/CLKIN	I	Crystal input internal oscillator or external system clock input

† Input/Output/High-impedance state.



functional block diagram



TMS320C10, TMS320C10-14, TMS320C10-25
DIGITAL SIGNAL PROCESSORS

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electrical specifications

This section contains the electrical specifications for all speed versions of the 'C10 Digital Signal Processors, including test parameter measurement information.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range V_{CC} (see Note 6)	— 0.3 V to 7 V
Input voltage range	— 0.3 V to 7 V
Output voltage range	— 0.3 V to 7 V
Continuous power dissipation	0.5 mW
Operating free-air temperature: L suffix	0°C to 70°C
A suffix	— 40°C to 85°C
Storage temperature	— 55°C to 150°C

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS} .

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN	3			V
		All remaining inputs	2			V
V_{IL}	Low-level input voltage	MC/MP			0.6	V
		All remaining inputs			0.8	V
I_{OH}	High-level output current, all outputs				—300	μ A
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature	L suffix	0		70	°C
		A suffix	— 40		85	°C



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TMS320C10, TMS320C10-14, TMS320C10-25 DIGITAL SIGNAL PROCESSORS

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electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VOH	High-level output voltage		IOH = MAX		2.4	3		V
			IOH = 20 µA (see Note 7)		VCC – 0.4‡			
VOL	Low-level output voltage		IOL = MAX			0.3	0.5	V
IOZ	Off-state output current		VCC = MAX	VO = 2.4 V		20		µA
				VO = 0.4 V		– 20		
II	Input current		VCC = VSS to VCC	All inputs except CLKIN		±20		µA
				CLKIN		±50		
Ci	Input capacitance	Data bus	f = 1 MHz, all other pins 0 V			25‡		pF
		All others				15‡		
Co	Output capacitance	Data bus				25‡		pF
		All others				10‡		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Values derived from characterization data and not tested.

NOTE 7: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

INTERNAL CLOCK OPTION

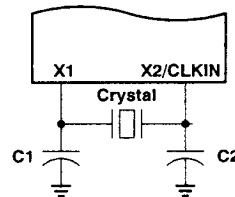


Figure 1. Internal Clock Option

PARAMETER MEASUREMENT INFORMATION

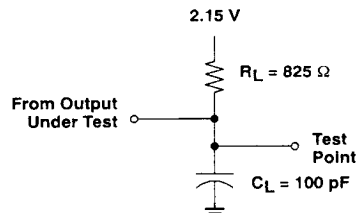


Figure 2. Test Load Circuit

TEXAS
INSTRUMENTS

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A-17