National Semiconductor Corporation

microCMOS

T-75-11-09

TP3052/TP3052-1/TP3053/TP3053-1 TP3054/TP3054-1/TP3057/TP3057-1 Serial Interface CODEC/FILTER COMBO™ Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

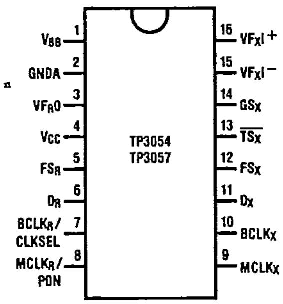
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
- μ-law with signaling, TP3020 or TP5116A timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Dual-In-Line on PCC surface mount packages

Connection Diagrams (Continued on Page 15)

Dual-In-Line Package

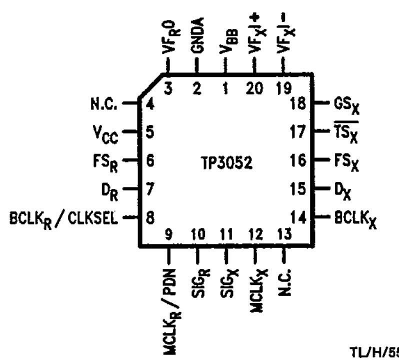


TL/H/5510-1

Top View

Order Number TP3054J, TP3054J-1, TP3057J or TP3057J-1
See NS Package Number J16A

Plastic Chip Carriers



TL/H/5510-10

Top View

Order Number TP3052V or TP3052V-1
See NS Package Number V20A

Block Diagram

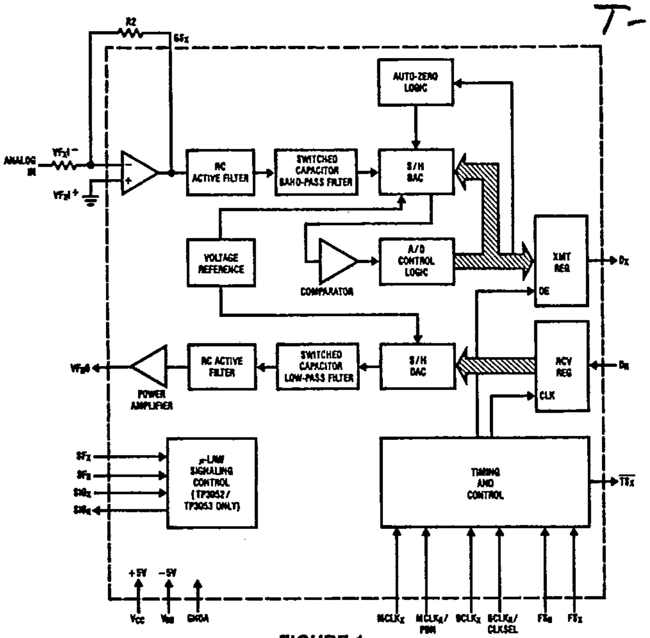


FIGURE 1

TL/H/5510-2

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
SF_R	When high during FS_R, this input indicates a receive signal frame.
SIG_R	The eighth bit of the PCM data appears at this output after each receive signalling frame.
SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
SF_X	When high during FS_X, this input indicates a transmit signaling frame.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3053 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 53, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the TP5116A/56A long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 and TP3053 μ-law COMBOs contain circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications, and the TP3053 for long frame sync applications, although the TP3053 may also be used in short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Functional Description (Continued)

Signaling for the TP3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2.* With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "½" to minimize noise and distortion. This short frame signaling may also be implemented using the TP3053, providing SF_R and SF_X are left open circuit or tied low. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the TP3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the TP3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R, which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the "½" step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4.* The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3052, TP3053, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3052, TP3053, TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifer capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC}+0.3V to V_{BB}−0.3V
Voltage at any Digital Input or Output	V_{CC}+0.3V to GNDA−0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ESD rating is to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L=3.2 mA $\overline{SIG_R}$, I_L=1.0 mA $\overline{TS_X}$, I_L=3.2 mA, Open Drain			**0.4** **0.4** **0.4**	V V V
V_{OH}	Output High Voltage	D_X, I_H= −3.2 mA SIG_R, I_H= −1.0 mA	**2.4** **2.4**			V V
I_{IL}	Input Low Current	GNDA≤V_{IN}≤V_{IL}, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	V_{IH}≤V_{IN}≤V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA≤V_O≤V_{CC}	**−10**		**10**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	−2.5V≤V≤+2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V≤V≤+2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, R_L≥10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO= ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	No Load		0.5	**1.5**	mA
$I_{BB}0$	Power-Down Current	No Load		0.05	**0.3**	mA
$I_{CC}1$	Power-Up Active Current	No Load		6.0	**9.0**	mA
$I_{BB}1$	Power-Up Active Current	No Load		6.0	**9.0**	mA

Timing Specifications Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V. See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	**100**			ns
t_{WBH}	Width of Bit Clock High	V_{IH} = 2.2V	**160**			ns
t_{WBL}	Width of Bit Clock Low	V_{IL} = 0.6V	**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	**80**			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			**140**	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	C_L = 0 pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	**20**		**165**	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	TP3053 Only	**60**			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	TP3053 Only	**60**			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	TP3052 and TP3053	**100**			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	TP3052 and TP3053	**50**			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		**50**			ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	TP3053 Only	**100**			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock		485	488	15725	ns

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Timing Diagrams

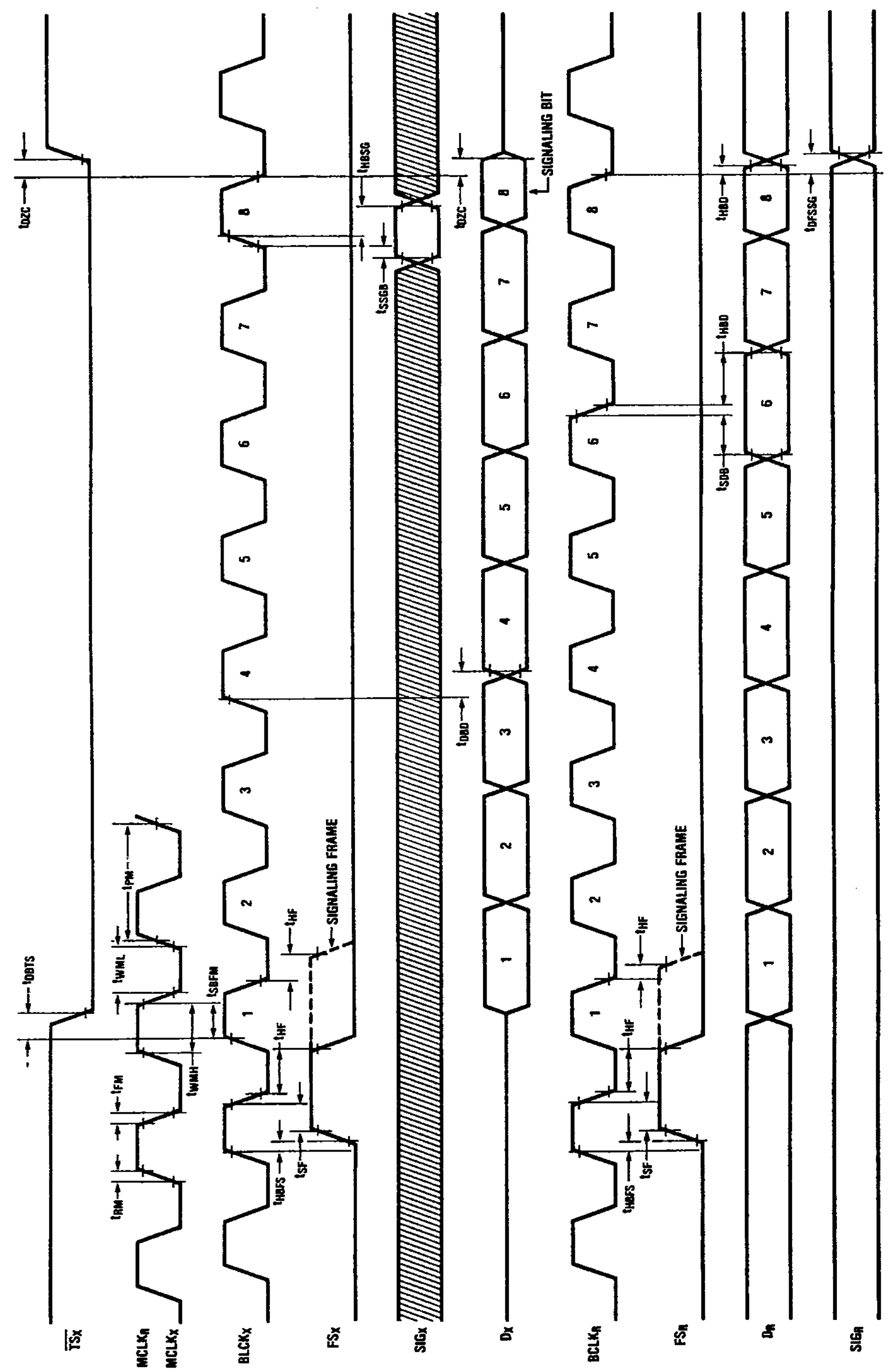

FIGURE 2. Short Frame Sync Timing

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Timing Diagrams (Continued)

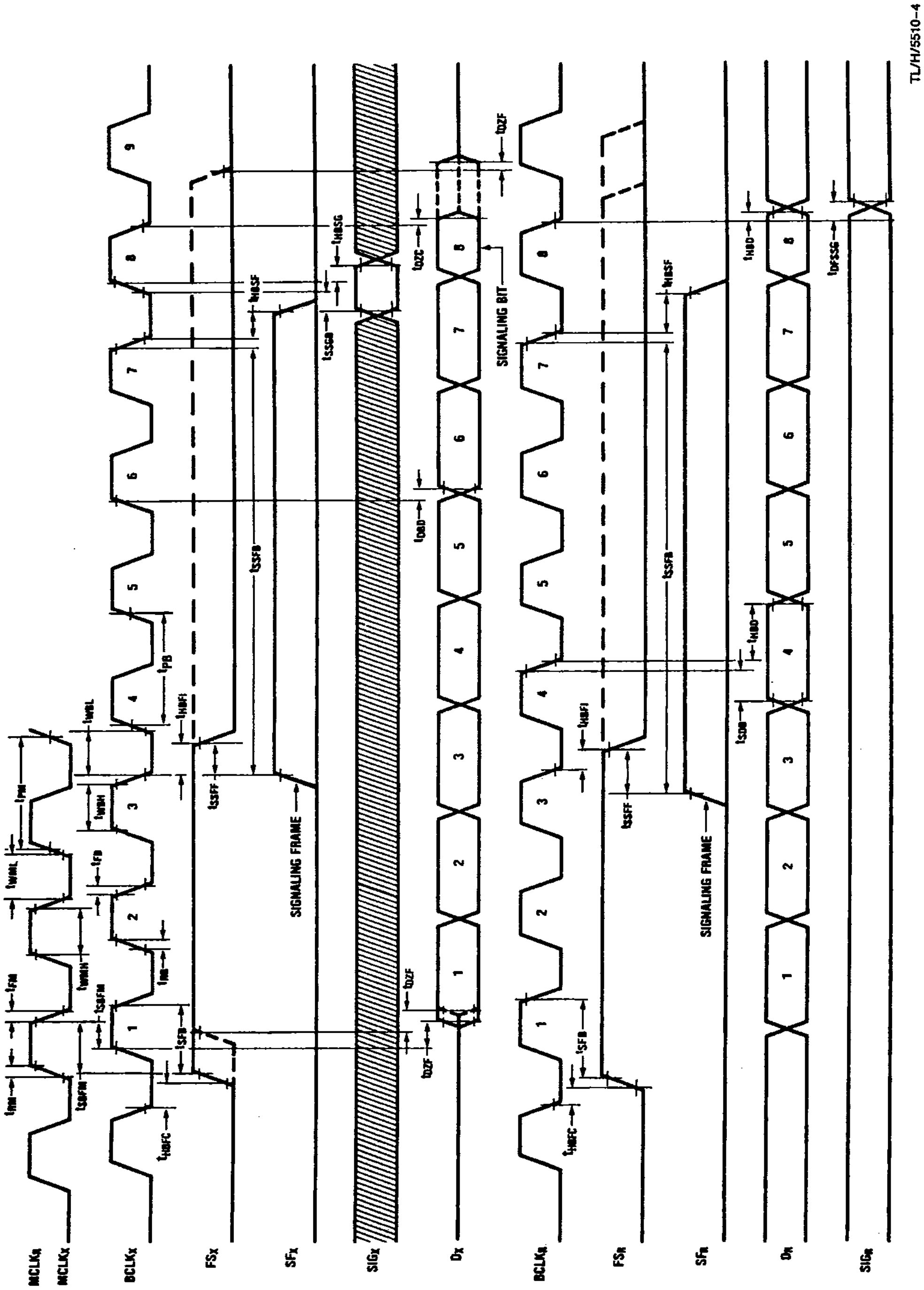

FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		1.2276		Vrms
t_{MAX}		Max Overload Level TP3052, TP3053, TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input at GS_X=0 dBm0 at 1020 Hz TP3052/53/54/57 TP3052/53/54/57-1	 **−0.15** **−0.20**		 **0.15** **0.20**	 dB dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz f=50 Hz f=60 Hz (TP3052/53/54/57-1) f=60 Hz (TP3052/53/54/57) f=200 Hz f=300 Hz–3000 Hz f=3300 Hz f=3400 Hz (TP3052/53/54/57) f=3400 Hz (TP3052/53/54/57-1) f=4000 Hz f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7** **−0.95**		**−40** **−30** **−22** **−26** **−0.1** **0.15** **0.05** **0** **0.05** **−14** **−32**	dB dB dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 VF_XI+ = −40 dBm0 to +3 dBm0 VF_XI+ = −50 dBm0 to −40 dBm0 VF_XI+ = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz TP3052/53/54/57 TP3052/53/54/57-1	 **−0.15** **−0.20**		 **0.15** **0.20**	 dB dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz	**−0.15** **−0.35** **−0.7**		**0.15** **0.05** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level = −40 dBm0 to +3 dBm0 = −40 dBm0 to +3 dBm0 (TP3052/53/54/57-1 only) = −50 dBm0 to −40 dBm0 = −55 dBm0 to −50 dBm0	 **−0.2** **−0.25** **−0.4** **−1.2**		 **0.2** **0.25** **0.4** **1.2**	 dB dB dB dB
V_{RO}	Receive Output Drive Level	R_L=600Ω	−2.5		2.5	V

Transmission Characteristics

(Continued) Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f=500 Hz–600 Hz f=600 Hz–800 Hz f=800 Hz–1000 Hz f=1000 Hz–1600 Hz f=1600 Hz–2600 Hz f=2600 Hz–2800 Hz f=2800 Hz–3000 Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
D_{RA}	Receive Delay, Absolute	f=1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f=500 Hz–1000 Hz f=1000 Hz–1600 Hz f=1600 Hz–2600 Hz f=2600 Hz–2800 Hz f=2800 Hz–3000 Hz	−40 −30	−25 −20 70 100 145	 90 125 175	μs μs μs μs μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3052, TP3053, TP3054 TP3052/53/54-1 (Note 1)		12	**15** **16**	dBrnC0 dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3057 TP3057-1 (Note 1)		−74	**−67** **−66**	dBm0p dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero — TP3052/53/54 TP3052/53/54-1		 8	 **11** **13**	 dBrnC0 dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero — TP3057-1		−82	**−79** **−77**	dBm0p dBm0p
N_{RS}	Noise, Single Frequency	f=0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+=0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = −50 dBm0 V_{CC}=5.0 V_{DC}+100 mVrms f=0 kHz–50 kHz (Note 2)	 **40**			 dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = −50 dBm0 V_{BB}=−5.0 V_{DC}+100 mVrms f=0 kHz–50 kHz (Note 2)	 **40**			 dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC}=5.0 V_{DC}+100 mVrms Measure VF_RO f=0 Hz–4000 Hz f=4 kHz–25 kHz f=25 kHz–50 kHz f=0–4 kHz (TP3052/53/54/57-1) f=4–50 kHz (TP3052/53/54/57-1)	 **40** **40** **36** **38** **35**			 dBC dB dB dBC dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB}=−5.0 V_{DC}+100 mVrms Measure VF_RO f=0 Hz–4000 Hz f=4 kHz–25 kHz f=25 kHz–50 kHz	 **40** **40** **36**			 dBC dB dB

Transmission Characteristics

(Continued) Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R.			−30	dB
		4600 Hz–7600 Hz			−30	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−30	dB
DISTORTION						
STD_X, STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		= −55 dBm0 XMT	**14**			dBC
		RCV	**15**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_X+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Quiet PCM Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz, VF_XI = Multitone (Note 2)		−90	**−70** (Note 2)	dB

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3053, TP3054 μ-Law								TP3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI+.

Note 3: All devices are measured using C message weighted filter.

Applications Information

POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

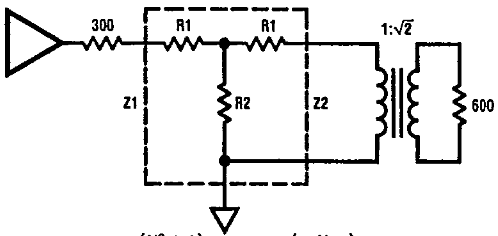
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

Where: $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

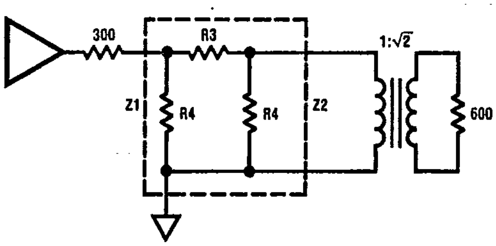
$$S = \sqrt{\frac{Z1}{Z2}}$$

Also: $Z = \sqrt{Z_{SC} \bullet Z_{OC}}$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



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$$R3 = \sqrt{\frac{Z1.Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

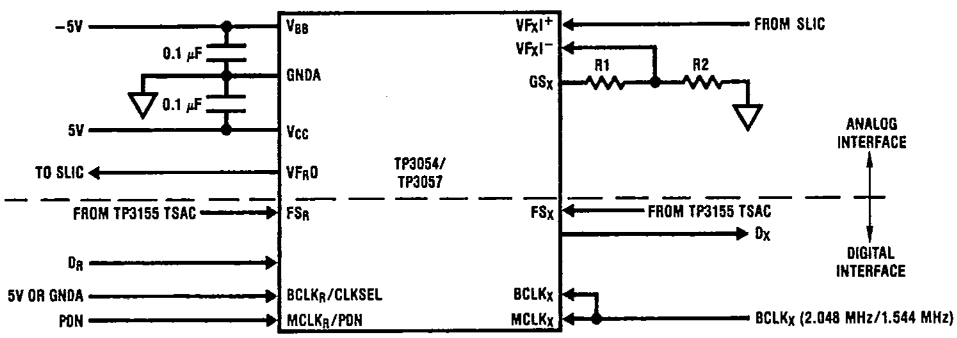
Note: See Application Note 370 for further details.

Applications Information (Continued)

TABLE II. Attentuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.61	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



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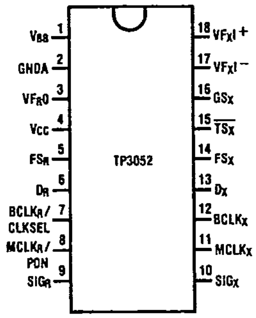
Note 1: XMIT gain $= 20 \times \log \left(\frac{R1+R2}{R2}\right)$ where $(R1+R2) > 10\ K\Omega$.

FIGURE 4

Connection Diagrams (Continued)

Dual-In-Line Package



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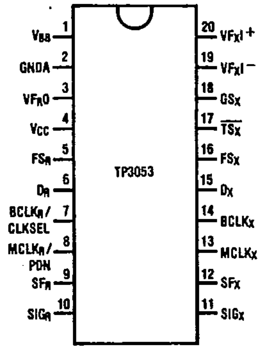
Top View

Order Number TP3052J or TP3052J-1

See NS Package Number J18A

Dual-In-Line Package



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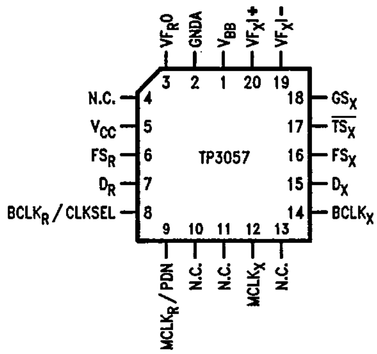
Top View

Order Number TP3053J or TP3053J-1

See NS Package Number J20A

Plastic Chip Carrier



TL/H/5510-7

Top View

Order Number TP3057V or TP3057V-1

See NS Package Number V20A