National Semiconductor

TP3072V-X COMBO® II Programmable PCM CODEC/Filter

General Description

The TP3072V-X is a second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber line and trunk cards. Using advanced switched capacitor techniques, COMBO II combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO II to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output.

Features

- Complete CODEC and FILTER system including:
  - — Transmit and receive PCM channel filters
  - — μ-law or A-law companding encoder and decoder
  - — Receive power amplifier drives 300Ω
  - — 4.096 MHz serial PCM data (max)
- Programmable Functions:
  - — Transmit gain: 19.0 dB range, 0.1 dB steps
  - — Receive gain: 19.0 dB range, 0.1 dB steps
  - — Hybrid balance cancellation filter
  - — 6 interface latches
  - — A or μ-law
  - — Analog loopback
  - — Digital loopback
- Direct interface to solid-state SLICs
- Simplifies transformer SLIC; single winding secondary
- Standard serial control interface
- 80 mW operating power (typ)
- 1.5 mW standby power (typ)
- Designed for CCITT and LSSGR applications
- TTL and CMOS compatible digital interfaces
- Extended temperature −40°C to +85°C
- See also AN-614 COMBO II Application Guide

Block Diagram

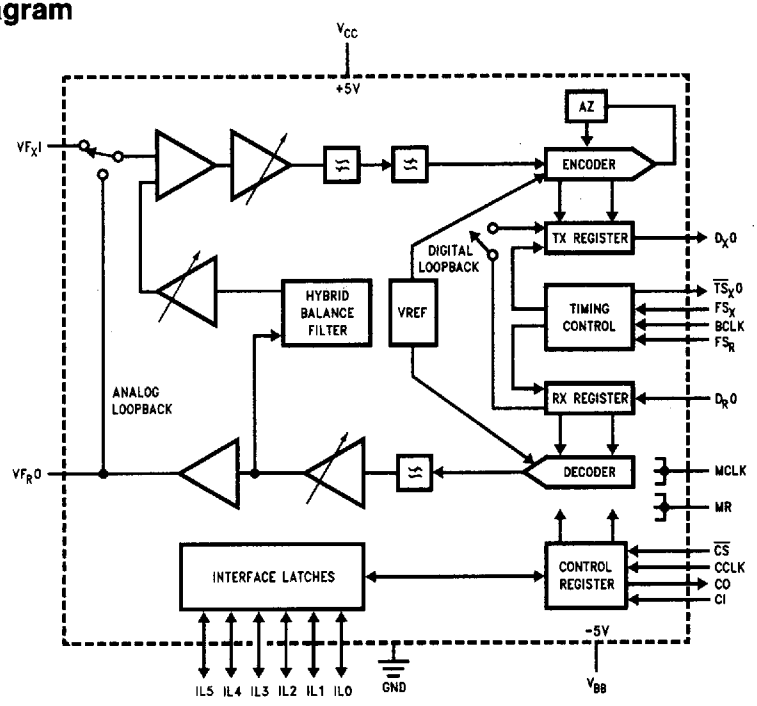

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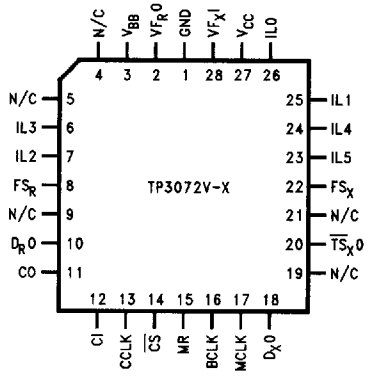
FIGURE 1

Connection Diagrams



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Order Number TP3072V-X
See NS Package Number V28A

Pin Descriptions

Pin	Description
V_{CC}	+5V ±5% power supply.
V_{BB}	−5V ±5% power supply.
GND	Ground. All analog and digital signals are referenced to this pin.
FS_X	Transmit Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the transmit timeslot.
FS_R	Receive Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the receive timeslot.
BCLK	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 128 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.
VF_XI	The Transmit analog high-impedance input. Voice frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and shifted out on the D_X0 pin.
VF_RO	The Receive analog power amplifier output, capable of driving load impedances as low as 300Ω (depending on the peak overload level required). PCM data received on the D_R0 pin is decoded and appears at this output as voice frequency signals.
D_X0	This Transmit Data TRI-STATE® output remains in the high impedance state except when the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS}_X0$	Normally this open-drain output is floating in a high impedance state except when the time-slot is active on the D_X0 output, when the $\overline{TS}_X0$ output pulls low to enable a backplane line-driver.
D_R0	This receive data input is inactive except during the time slot when the receive PCM data is shifted in on the falling edges of BCLK.
CCLK	Control Clock input. This clock shifts serial control information into or out from the CI or CO pin when the $\overline{CS}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI	Control Input pin. Serial control information is shifted to COMBO II on this pin when $\overline{CS}$ is low. It can be connected to CO if required.
CO	Control Output pin. Serial control information is read from COMBO II on this pin when $\overline{CS}$ is low. It can be connected to CI if required.
$\overline{CS}$	Chip Select input. When this pin is low, control information can be written to or read from COMBO II via the CI or CO pin.
IL5–IL0	IL5 through IL0 are available on the TP3072V-X. Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO II, while $\overline{CS}$ is low, and the information is shifted out on the CO pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
MR	This logic input must be pulled low for normal operation of COMBO II. When pulled momentarily high (at least 1 μsec.), all programmable registers in the device are reset to the states specified under "Power-On Initialization".
NC	No Connection. Do not connect to this pin. To prevent noise injection, do not route traces through this pin.

Functional Description

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO II and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed to OFF (00000000), the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI pin is ready for the first control byte of the initialization sequence. Other initial states in the Control Register are indicated in Section 2.0.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low. If not used, MR should be hard-wired to ground.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the "P" bit set to "1" as indicated in Table I. It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 output is in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are necessary to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see Tables I and II). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 during the first time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 pin during the first time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Power Amplifier capable of driving a 300Ω load to ±3.5V, a 600Ω load to ±3.8V or a 15 kΩ load to ±4.0V at peak overload.

A decode cycle begins immediately after the receive time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (½ frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table II). Non-delayed data mode is similar to long-frame timing on the TP3050/60 series of devices (COMBO®); time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode, which is similar to short-frame sync timing on COMBO, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles. During the Transmit time-slot, the D_X0 output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}_X0$ also pulls low for the first 7½ bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the D_R0 input during the Receive time-slot on the falling edges of BCLK.

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO II via the serial control port consisting of the control clock CCLK, the serial data input, CI, and output, CO, and the Chip Select input, $\overline{CS}$. All control instructions require 2 bytes, as listed in Table I, with the exception of a single byte power-up/down command. The byte 1 bits are used as follows: bit 7 specifies power up or power down;

Functional Description (Continued)

TABLE I. Programmable Register Instructions

Function	Byte 1 (Note 1) 7	6	5	4	3	2	1	0	Byte 2 (Note 1) 7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See Table II							
Read-Back Control Register	P	0	0	0	0	1	1	X	See Table II							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See Table V							
Read Interface Latch Register	P	0	0	0	1	1	1	X	See Table V							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table IV							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table IV							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table VII							
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table VII							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table VI							
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table VI							
White Hybrid Balance Register 1	P	0	1	1	0	0	1	X	Derive from Optimization Routine in TP3077SW Program							
Read Hybrid Balance Register 1	P	0	1	1	0	1	1	X								
White Hybrid Balance Register 2	P	0	1	1	1	0	1	X								
Read Hybrid Balance Register 2	P	0	1	1	1	1	1	X								
White Hybrid Balance Register 3	P	1	0	0	0	0	1	X								
Read Hybrid Balance Register 3	P	1	0	0	0	1	1	X								

Note 1: Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI or CO pin. X = don't care.

Note 2: "P" is the power-up/down control bit, see "Power-Up/Down Control" section. ("0" = Power Up, "1" = Power Down)

Note 3: Other register address codes are invalid and should not be used.

bits 6, 5, 4 and 3 specify the register address; bit 2 specifies whether the instruction is read or write; bit 1 specifies a one or two byte instruction; and bit 0 is not used.

To shift control data into COMBO II, CCLK must be pulsed 8 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first contiguously, i.e. it is not mandatory for $\overline{CS}$ to return high between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ should be set high when no data transfers are in progress.

To readback Interface Latch data or status information from COMBO II, the first byte of the appropriate instruction is strobed in while $\overline{CS}$ is low, as defined in Table I. $\overline{CS}$ must be kept low, or be taken low again for a further 8 CCLK cycles, during which the data is shifted onto the CO pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO pin is in the high-impedance TRI-STATE, enabling the CI and CO pins of many devices to be multiplexed together.

If $\overline{CS}$ returns high during either byte 1 or byte 2 before all eight CCLK pulses of that byte occur, both the bit count and byte count are reset and register contents are not affected. This prevents loss of synchronization in the control interface as well as corruption of register data due to processor interrupt or other problem. When $\overline{CS}$ returns low again, the device will be ready to accept bit 1 of byte 1 of a new instruction.

Programmable Functions

1.0 POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in Table I into COMBO II with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the "P" bit as indicated. When the power-up or down control is entered as a single byte instruction, bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output, D_X0, will remain in the high impedance state until the second FS_X pulse after power-up.

Programmable Functions (Continued)

2.0 CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in Table I. The second byte has the following bit functions:

TABLE II. Control Register Byte 2 Functions

Bit Number and Name								Function
7	6	5	4	3	2	1	0	
F_1	F_0	MA	IA	DN	DL	AL	PP	
0	0							MCLK = 512 kHz
0	1							MCLK = 1.536 or 1.544 MHz
1	0							MCLK = 2.048 MHz*
1	1							MCLK = 4.096 MHz
		0	X					Select μ-255 law*
		1	0					A-law, Including Even Bit Inversion
		1	1					A-law, No Even Bit Inversion
				0				Delayed Data Timing
				1				Non-Delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization. (Bit 4 = 0)

2.1 Master Clock Frequency Selection

A Master clock must be provided to COMBO II for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see Table II) must be set during initialization to select the correct internal divider.

2.2 Coding Law Selection

Bits "MA" and "IA" in Table II permit the selection of μ255 coding or A-law coding, with or without even bit inversion.

2.3 Analog Loopback

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop. Hybrid balance must be disabled for meaningful analog loopback function.

2.4 Digital Loopback

Digital Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register at D_X0. In digital loopback, the decoder will remain functional and output a signal at VF_RO. If this is undesirable, the receive output can be turned off by programming the receive gain register to all zeros.

3.0 INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Tables I and IV. For minimum power dissipation, unconnected latch pins should be programmed as outputs.

Bits L_5–L_0 must be set by writing the specified instruction to the LDR with the L bits in the second byte set as follows:

TABLE IV. Byte 2 Functions of Latch Direction Register

Byte 2 Bit Number							
7	6	5	4	3	2	1	0
L_0	L_1	L_2	L_3	L_4	L_5	X	X

L_n Bit	IL Direction
0	Input
1	Output

X = don't care

4.0 INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Tables I and V. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first, followed immediately by the Latch Direction Register.

TABLE V. Interface Latch Data Bit Order

Bit Number							
7	6	5	4	3	2	1	0
D_0	D_1	D_2	D_3	D_4	D_5	X	X

TABLE III. Coding Law Conventions

	μ255 law		True A-law with even bit inversion		A-law without even bit inversion	
	MSB	LSB	MSB	LSB	MSB	LSB
V_{IN} = +Full Scale	1	0000000	1	0101010	1	1111111
V_{IN} = 0V	1	1111111	1	1010101	1	0000000
	0	1111111	0	1010101	0	0000000
V_{IN} = −Full Scale	0	0000000	0	0101010	0	1111111

Note 1: The MSB is always the first PCM bit shifted in or out of COMBO II.

Programmable Functions (Continued)

5.0 PCM DIGITAL INTERFACE

COMBO II operates in fixed time-slot mode similar to the TP3050/60 series devices (COMBO). Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R; see *Figure 3*. Alternately, the device can be programmed to function in Delayed Timing mode in which the time-slot always begins with the leading (rising) edge of the second BCLK following leading edge of frame sync inputs FS_X and FS_R; see *Figure 4*. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

6.0 TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Tables I and VI. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.619 Vrms and 0.182 Vrms (equivalent to +6.4 dBm to −12.6 dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.08595)$$

and convert to the binary equivalent. Some examples are given in Table VI.

It should be noted that the Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB (Gain Register set to all ones). At high transmit gains there will be some degradation in noise performance for these parameters. See Application Note AN-614 for more information on this subject.

TABLE VI. Byte 2 of Transmit Gain Instruction

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_XI
0 0 0 0 0 0 0 0	No Output*
0 1 0 0 0 0 0 1	0.182
0 1 0 0 0 0 1 0	0.184
—	—
1 1 1 1 1 1 1 0	1.600
1 1 1 1 1 1 1 1	1.619

*Analog signal path is cut off, but D_X0 remains active and will output code representing idle noise.

7.0 RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Tables I and VII. Note the following restrictions on output drive capability:

a) 0 dBm0 levels ≤ 1.96 Vrms at VF_RO may be driven into a load of ≥ 15 kΩ to GND; receive gain set to 0 dB (Gain Register set to all ones)

b) 0 dBm0 levels ≤ 1.85 Vrms at VF_RO may be driven into a load of ≥ 600Ω to GND; receive gain set to −0.5 dB

c) 0 dBm0 levels ≤ 1.71 Vrms at VF_RO may be driven into a load of ≥ 300Ω to GND; receive gain set to −1.2 dB

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1043)$$

and convert to the binary equivalent. Some examples are given in Table VII.

TABLE VII. Byte 2 of Receive Gain Instruction

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_RO
0 0 0 0 0 0 0 0	No Output (Low Z to GND)
0 1 0 0 0 0 0 1	0.220
0 1 0 0 0 0 1 0	0.223
—	—
1 1 1 1 1 1 1 0	1.941
1 1 1 1 1 1 1 1	1.964

8.0 HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO II is a programmable filter consisting of a second-order section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The 2nd order section is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals.

As a 2nd order section, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring Hybal1, matching the phase of the hybrid at low to mid-band frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The 2nd order mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low-frequency pole and zero. In this mode, the pole/zero frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Figure 2 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_XI, are a function of the termination impedance Z_T, the line transformer and the impedance of the 2W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_RO to VF_XI is:

$$H(w) = Z_L'/(Z_T + Z_L') \quad (1)$$

8.1 PROGRAMMING THE FILTER

On initial power-up, the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in *Figure 2*. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input, D_RO, to the PCM digital output, D_XO, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO II to fully configure the Hybrid Balance Filter as follows:

Register 1: select/de-select Hybrid Balance Filter;
invert/non-invert cancellation signal;
select/de-select Hybal2 filter section;
attenuator setting.

Register 2: select/de-select Hybal1 filter;
set Hybal1 to 2nd order or 1st order;
pole and zero frequency selection.

Register 3: program pole frequency in Hybal2 filter;
program zero frequency in Hybal2 filter.

Standard filter design techniques may be used to model the echo path (see Equation 1) and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter designed to replicate it.

A Hybrid Balance filter design guide and software optimization program are available under license from National Semiconductor Corporation; order TP3077SW.

Applications Information

POWER SUPPLIES

While the pins of the TP3072V-X COMBO II devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, extra long pins on the connector should be used for ground and V_{BB}. In addition, a Schottky diode should be connected between V_{BB} and ground.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the device GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common device ground point to V_{CC} and V_{BB} as close to the device pins as possible. V_{CC} and V_{BB} should also be decoupled with Low Effective Series Resistance Capacitors of at least 10 μF located near the card edge connector.

Further guidelines on PCB layout techniques are provided in Application Note AN-614, "COMBO II™ Programmable PCM CODEC/Filter Family Application Guide".

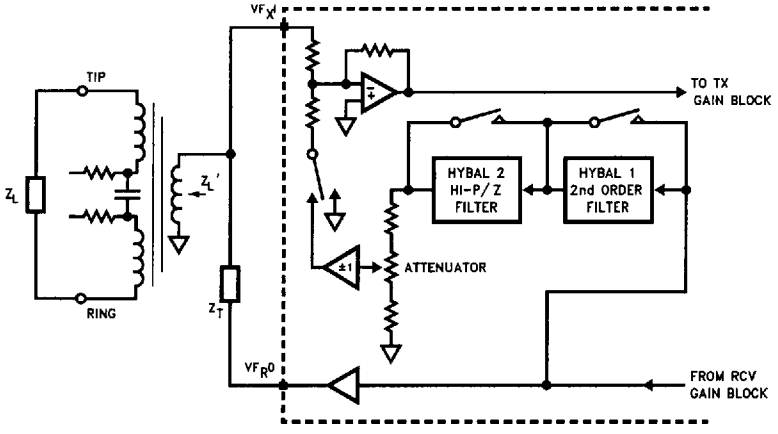

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FIGURE 2. Simplified Diagram of Hybrid Balance Circuit

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at VF_XI	V_{CC} + 0.5V to V_{BB} − 0.5V
Voltage at any Digital Input	V_{CC} + 0.5V to GND − 0.5V
Storage Temperature Range	−65°C to + 150°C
V_{BB} to GND	−7V
Current at VF_RO	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs (DC Meas.)*			**0.7**	V
V_{IH}	Input High Voltage	All Digital Inputs (DC Meas.)*	**2.0**			V
V_{OL}	Output Low Voltage	D_X0, $\overline{TS}_X0$, and CO, I_L = 3.2 mA, All Other Digital Outputs, I_L = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X0, and CO, I_L = −3.2 mA, All Other Digital Outputs (except $\overline{TS}_X$), I_L = −1 mA All Digital Outputs, I_L = −100 µA	**2.4** V_{CC} − 0.5			V V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	**−10**		**10**	µA
I_{IH}	Input High Current	Any Digital Input except MR, V_{IH} < V_{IN} < V_{CC}	**−10**		**10**	µA
		MR Only	**−10**		**100**	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X0, $\overline{TS}_X0$, CO IL5–IL0 When Selected as Inputs GND < V_{OUT} < V_{CC}	**−30**		**30**	µA
ANALOG INTERFACES						
I_{VFXI}	Input Current, VF_XI	−3.3V < VF_XI < 3.3V	**−10.0**		**10.0**	µA
R_{VFXI}	Input Resistance	−3.3V < VF_XI < 3.3V	**390**	620		kΩ
VOS_X	Input Offset Voltage Applied at VF_XI	Transmit Gain = 0 dB Transmit Gain = 25.4 dB			200 10	mV mV
RL_{VFRO}	Load Resistance	Receive Gain = 0 dB	15k			
CL_{VFRO}	Load Capacitance	CL_{VFRO} from VF_RO to GND			**200**	pF
RO_{VFRO}	Output Resistance	Steady Zero PCM Code Applied to D_R0		1.0	3.0	Ω
VOS_R	Output Offset Voltage at V_{FRO}	Alternating ± Zero PCM Code Applied to D_R0, Maximum Receive Gain	**−200**		**200**	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	CCLK, CI, CO, = 0.4V, $\overline{CS}$ = 2.4V Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled		0.1	**0.6**	mA
$I_{BB}0$	Power Down Current	As Above		−0.1	**−0.4**	mA
$I_{CC}1$	Power Up Current	CCLK, CI, CO = 0.4V, $\overline{CS}$ = 2.4V No Load on Power Amp Interface Latches Set as Outputs with No Load		8.0	**13.0**	mA
$I_{BB}1$	Power Up Current	As Above		−8.0	**−13.0**	mA
$I_{CC}2$	Power Down Current	Power Amp Enabled		2.0	**4.0**	mA
$I_{BB}2$	Power Down Current	Power Amp Enabled		−2.0	**−4.0**	mA

Note *: See definitions and timing conventions section.

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%; V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK TIMING						
f_{MCLK}	Frequency of MCLK	Selection of Frequency is Programmable (See Table III)		512 1536 1544 2048 **4096**		kHz kHz kHz kHz kHz
t_{WMH}	Period of MCLK High	Measured from V_{IH} to V_{IH} (See Note)	**80**			ns
t_{WML}	Period of MCLK Low	Measured from V_{IL} to V_{IL} (See Note)	**80**			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBM}	HOLD Time, BCLK LOW to MCLK HIGH		**50**			ns
t_{WFL}	Period of F_{SX} or F_{SR} Low	Measured from V_{IL} to V_{IL}	1			MCLK Period
PCM INTERFACE TIMING						
f_{BCLK}	Frequency of BCLK	May Vary from 128 kHz to 4096 kHz in 8 kHz Increments	**128**		**4096**	kHz
t_{WBH}	Period of BCLK High	Measured from V_{IH} to V_{IH}	**80**			ns
t_{WBL}	Period of BCLK Low	Measured from V_{IL} to V_{IL}	**80**			ns
t_{RB}	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FB}	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low		**30**			ns
t_{SFB}	Setup Time, $FS_{X/R}$ High to BCLK Low		**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads			**90**	ns
t_{DBZ}	Delay Time, BCLK Low to D_X0 Disabled if FS_X Low, FS_X Low to D_X0 disabled if 8th BCLK Low, or BCLK High to D_X0 Disabled if FS_X High		**15**		**100**	ns
t_{DBT}	Delay Time, BCLK High to $\overline{TS}_X$ Low if FS_X High, or FS_X High to $\overline{TS}_X$ Low if BCLK High	Load = 100 pF Plus 2 LSTTL Loads			60	ns
t_{ZBT}	TRI-STATE Time, BCLK Low to $\overline{TS}_X$ High if FS_X Low, FS_X Low to $\overline{TS}_X$ High if 8th BCLK Low, or BCLK High to $\overline{TS}_X$ High if FS_X High		15		60	ns
t_{DFD}	Delay Time, $FS_{X/R}$ High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only			**90**	ns
t_{SDB}	Setup Time, D_R0 Valid to BCLK Low		**30**			ns
t_{HBD}	Hold Time, BCLK Low to D_R0 Invalid		**15**			ns

Note: Applies only to MCLK Frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ±2% Duty Cycle must be used.

Timing Specifications (Continued)

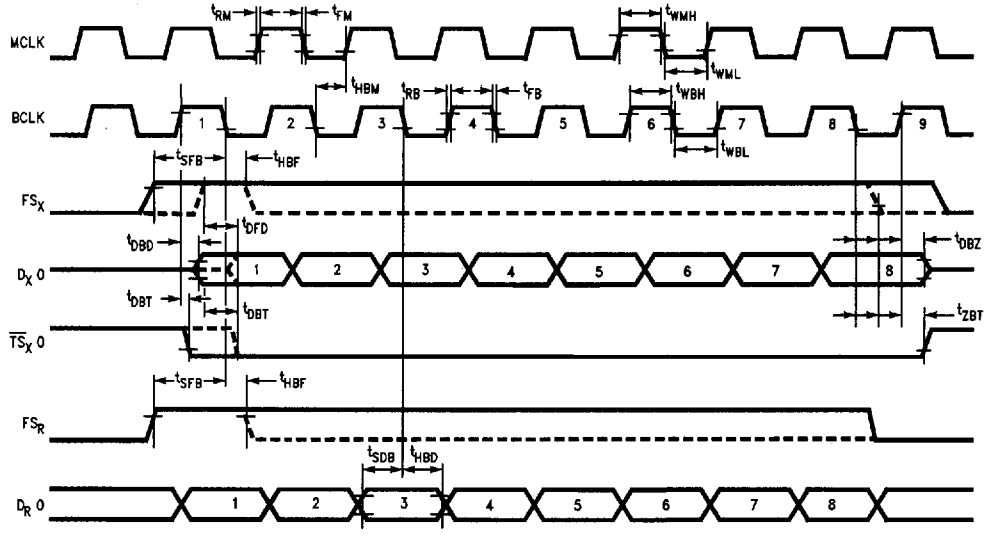
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL CONTROL PORT TIMING						
f_{CCLK}	Frequency of CCLK				**2048**	kHz
t_{WCH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	**160**			ns
t_{WCL}	Period of CCLK Low	Measured from V_{IL} to V_{IL}	**160**			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low	CCLK1	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High	CCLK 8	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low		**60**			ns
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High		50			ns
t_{SDC}	Setup Time, CI Data In to CCLK Low		**50**			ns
t_{HCD}	Hold Time, CCLK Low to CO Invalid		50			ns
t_{DCD}	Delay Time, CCLK High to CO Data Out Valid	Load = 100 pF plus 2 LSTTL Loads			**100**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO Valid	Applies Only if Separate $\overline{CS}$ used for Byte 2			**100**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or 9th CCLK High to CO High Impedance	Applies to Earlier of $\overline{CS}$ High or 9th CCLK High	15		80	ns
INTERFACE LATCH TIMING						
t_{SLC}	Setup Time, IL to CCLK 8 of Byte 1	Interface Latch Inputs Only	**100**			ns
t_{HCL}	Hold Time, IL Valid from 8th CCLK Low (Byte 1)		50			ns
t_{DCL}	Delay Time CCLK 8 of Byte 2 to IL	Interface Latch Outputs Only C_L = 50 pF			200	ns
MASTER RESET PIN						
t_{WMR}	Duration of Master Reset High		1			μs

Timing Diagrams



TL/H/11245–4

FIGURE 3. Non Delayed Data Timing Mode

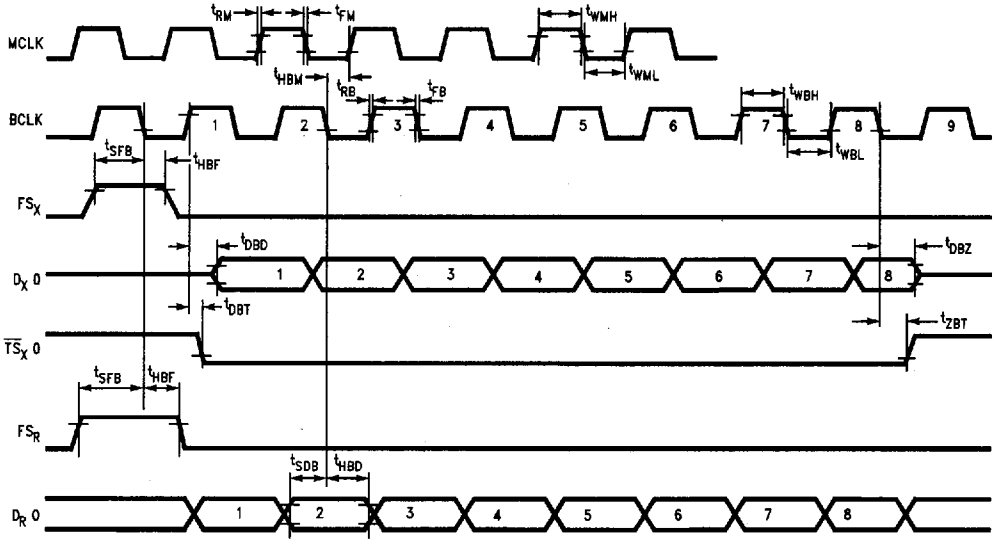


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FIGURE 4. Delayed Data Timing Mode (Time Slot Zero Only)

Timing Diagrams (Continued)

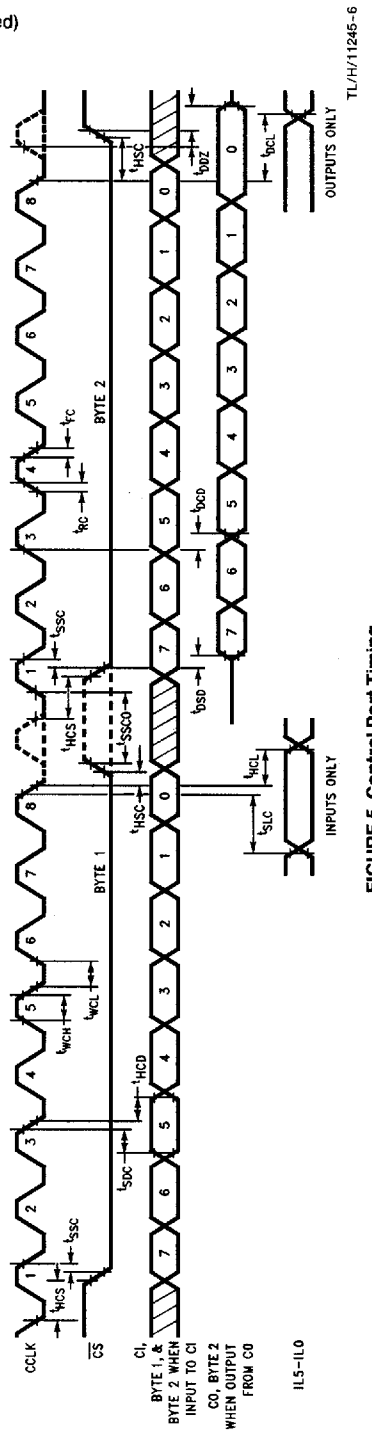

FIGURE 5. Control Port Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	The Maximum 0 dBm0 Levels are:				
		VF_XI		1.619		Vrms
		VF_RO (15 kΩ Load)		1.964		Vrms
		The Minimum 0 dBm0 Levels are:				
		VF_XI		0.182		mVrms
		VF_RO (Any Load ≥ 300Ω)		0.220		mVrms
		Overload Levels are 3.17 dBm0 (μLaw)				
		Gam = 19 dB and 3.14 dBm0 (A-Law)				
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for Maximum 0 dBm0 Test Level. (All 1's in gain register) Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at D_X0. T_A = 25°C	**−0.15**		**0.15**	**dB**
G_{XAG}	Transmit Gain Variation with Programmed Gain	T_A = 25°C, V_{CC} = 5V, V_{BB} = 5V				
		Programmed Gain from 0 dB to 12 dB				
		0 dBm0 Levels of 1.619 V_{rms} to 0.407 V_{rms}	**−0.12**		**0.12**	**dB**
		Programmed Gain from 12.1 dB to 19.0 dB				
		0 dBm0 Levels of 0.402 V_{rms} to 0.182 V_{rms}	**−0.14**		**0.14**	**dB**
G_{XAF}	Transmit Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4)				
		Minimum Gain < G_X < Maximum Gain				
		f = 60 Hz			−26	dB
		f = 200 Hz	−1.8		−0.1	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		f ≥ 4600 Hz. Measure Response at Alias Frequency from 0 kHz to 4 kHz.			−32	dB
		G_X = 0 dB, VF_XI = 1.619 Vrms				
		Relative to 1015.625 Hz				
		f = 62.5 Hz			**−24.9**	dB
		f = 203.125 Hz	**−1.7**		**−0.1**	dB
		f = 343.75 Hz	**−0.15**		**0.15**	dB
		f = 515.625 Hz	**−0.15**		**0.15**	dB
		f = 2140.625 Hz	**−0.15**		**0.15**	dB
		f = 3156.25 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
		Relative to 1062.5 Hz (Note 4)				
		f = 5250 Hz, Measure 2750 Hz			**−32**	dB
		f = 11750 Hz, Measure 3750 Hz			**−32**	dB
		f = 49750 Hz, Measure 1750 Hz			**−32**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE (Continued)						
G_{XAT}	Transmit Gain Variation with Temperature	Measured Relative to G_{XA}, V_{CC} = 5V, V_{BB} = −5V, Minimum gain < G_X < Maximum Gain	−0.15		0.15	dB
G_{XAL}	Transmit Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0.				
		VF_XI = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		VF_XI = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		VF_XI = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
G_{RA}	Receive Gain Absolute Accuracy	Receive Gain Programmed for Maximum 0 dBm0 Test Level (All 1's in Gain Register). Apply 0 dBm0 PCM Code to D_R0. Measure VF_RO. T_A = 25°C	**−0.15**		**0.15**	dB
G_{RAG}	Receive Gain Variation with Programmed Gain	T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V Programmed Gain from 0 dB to 12 dB 0 dBm0 Levels of 1.964 V_{rms} to 0.493 V_{rms}	**−0.12**		**0.12**	dB
		Programmed Gain from 12.1 dB to 19.0 dB 0 dBm0 Levels of 0.488 V_{rms} to 0.220 V_{rms}	**−0.14**		**0.14**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE (Continued)						
G_{RAT}	Receive Gain Variation with Temperature	Measured Relative to G_{RA}. V_{CC} = 5V, V_{BB} = −5V. Minimum Gain < G_R < Maximum Gain	−0.15		0.15	dB
G_{RAF}	Receive Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) D_R0 = 0 dBm0 code. Minimum Gain < G_R < Maximum Gain				
		f = 200 Hz	−0.25		0.15	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		G_R = 0 dB, D_R0 = 0 dBm0 Code, G_X = 0 dB (Note 4)				
		f = 296.875 Hz	**−0.15**		**0.15**	dB
		f = 1875.00 Hz	**−0.15**		**0.15**	dB
		f = 2906.25 Hz	**−0.15**		**0.15**	dB
		f = 2984.375 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
G_{RAL}	Receive Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0.				
		D_R0 = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		D_R0 = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		D_R0 = −55 dBm0 to − 50 dBm0	**−1.2**		**1.2**	dB
		D_R0 = 3.1 dBm0				
		R_L = 600Ω, G_R = −0.5 dB	−0.2		0.2	dB
		R_L = 300Ω, G_R = −1.2 dB	**−0.2**		**0.2**	dB
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Tx Delay, Absolute	f = 1600 Hz			315	μs
D_{XR}	Tx Delay, Relative to D_{XA}	f = 500–600 Hz			220	μs
		f = 600–800 Hz			145	μs
		f = 800–1000 Hz			75	μs
		f = 1000–1600 Hz			40	μs
		f = 1600–2600 Hz			75	μs
		f = 2600–2800 Hz			105	μs
		f = 2800–3000 Hz			155	μs
D_{RA}	Rx Delay, Absolute	f = 1600 Hz			200	μs
D_{RR}	Rx Delay, Relative to D_{RA}	f = 500–1000 Hz	−40			μs
		f = 1000–1600 Hz	−30			μs
		f = 1600–2600 Hz			90	μs
		f = 2600–2800 Hz			125	μs
		f = 2800–3000 Hz			175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted, μ-law Selected	(Note 1) All '1's in Gain Register		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted, A-law Selected	(Note 1) All '1's in Gain Register		−74	**−67**	dBm0p

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
NOISE (Continued)						
N_{RC}	Receive Noise, C Message Weighted, μ-law Selected	PCM Code is Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted, A-law Selected	PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–4 kHz (Note 2) f = 4 kHz–50 kHz	**36** 30			dBC dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz–4 kHz (Note 2) f = 4 kHz–50 kHz	**36** 30			dBC dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz–4000 Hz f = 4 kHz–25 kHz f = 25 kHz–50 kHz	 **36** 40 36			 dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz–4000 Hz f = 4 kHz–25kHz f = 25 kHz–50 kHz	 **36** 40 36			 dBC dB dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R0 4600 Hz–7600 Hz 7600 Hz–8400 Hz 8400 Hz–50,000 Hz			 **−30** **−40** **−30**	 dB dB dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel, μ-law Selected	Sinusoidal Test Method Level = 3.0 dBm0 = 0 dBm0 to − 30 dBm0 = −40 dBm0 = −45 dBm0	 **33** **36** **30** **25**			 dBC dBC dBC dBC
STD_{RL}	Signal to Total Distortion Receive with Resistive Load	Sinusoidal Test Method Level = +3.1 dBm0 R_L = 600Ω, G_R = −0.5 dB R_L = 300Ω, G_R = −1.2 dB	 33 **33**			 dBC dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Transmit or Receive Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Idle Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz (Note 2)		−90	**−70**	dB

Note 1: Measured by grounded input at VF_XI.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI.

Note 3: A signal is Valid if it is above V_{IH} or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply:

a) All input signals are defined as: V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10 ns, t_F < 10 ns.

b) t_R is measured from V_{IL} to V_{IH}. t_F is measured from V_{IH} to V_{IL}.

c) Delay Times are measured from the input signal Valid to the output signal Valid.

d) Setup Times are measured from the data input Valid to the clock input Invalid.

e) Hold Times are measured from the clock signal Valid to the data input Invalid.

f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}.

Note 4: A multi-tone test technique is used.