National Semiconductor

PRELIMINARY

T-75-11-09

TP3212 SLIM™ Subscriber Line Interface Module

General Description

The TP3212 is a complete electronic SLIC and PCM COMBO® CODEC/Filter module intended to interface the analog subscriber line to a PCM highway. It is designed to meet the requirements for POTS (Plain Old Telephone Service) lines in U.S. Digital Loop Carrier applications as specified in TR-TSY-000057. It has the capability to perform in-band on-hook transmission. When used in conjuction with a simple, non-critical, external protection network, two resistors and a ring relay, the TP3212 forms a complete line circuit, handling all the BORSCHT functions.

The TP3212 module consists of a line driver, a line receiver, a line impedance control circuit, a hybrid balance circuit, a loop supervision circuit, a ring supervision circuit, three positive relay drivers, a TP3054 COMBO CODEC/Filter and a serial control interface. Any changes in the status of the subscriber loop generate an interrupt, allowing the device to be used in either polled or interrupt driven applications.

Features

- Complete COMBO CODEC/Filter and SLIC functions
- Exceeds TR-TSY-000057 DLC specifications for POTS lines
- On-hook transmission capability
- Resistive loop feed with current limit
- Power denial mode
- Compatible with loop start and ground start signalling
- Automatic ring trip
- Four selectable balance networks
- Three positive relay drivers
- Thermal overload protection
- Compatible with inexpensive protection networks
- Withstands 500V RTN to GND surge
- Compatible with standard PCM highway
- Small physical size and minimal external components

Simplified Block Diagram

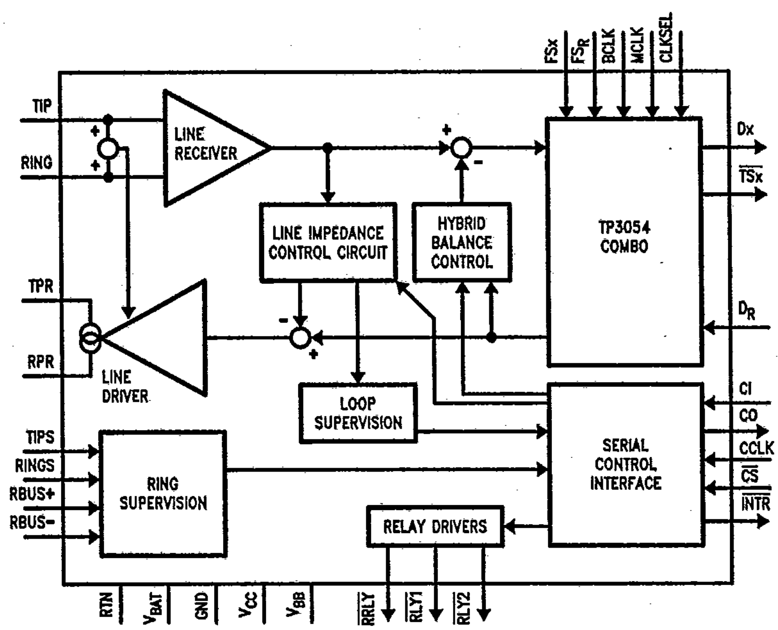

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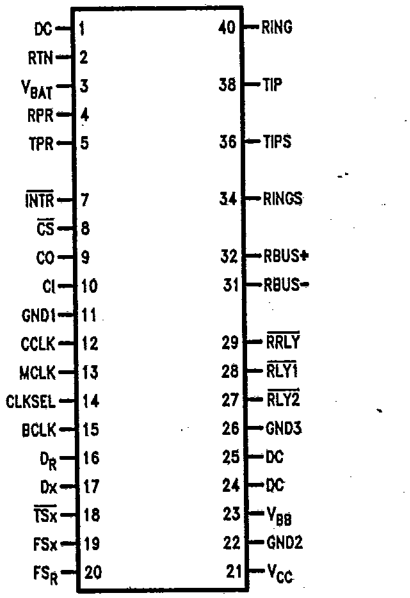
FIGURE 1. Simplified Block Diagram

Connection Diagram



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Order Number TP3212J
Refer To NSC Package Type HY40C

Pin Descriptions

Pin	Pin Descriptions
TIP	Normally positive side of the subscriber line.
RING	Normally negative side of the subscriber line.
TPR	High voltage line driver output. Connects to TIP via an external protection network.
RPR	High voltage line driver output. Connects to RING via an external protection network.
TIPS	Positive ring sensing input. Connected to the positive side of the subscriber loop during ringing.
RINGS	Negative ring sensing input. Connected to the negative side of the subscriber loop during ringing.
RBUS+	Positive ring bus sensing input. Connected to the positive side of the ring bus.
RBUS−	Negative ring bus sensing input. Connected to the negative side of the ring bus.
BCLK	Bit Clock used to shift PCM information into D_R and out of Dx. May vary from 64 kHz to 2.048 MHz in 8 kHz increments.
MCLK	Master clock. Must be 1.536, 1.544 or 2.048 MHz.
CLKSEL	Master clock select input. Must be connected high for 1.536 or 1.544 MHz operation. Must be connected low for 2.048 MHz operation.
FSx	Transmit frame synchronization pulse input which enables BCLK to shift the PCM information out of Dx. FSx is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
Dx	The TRI-STATE® PCM data output which is enabled by FSx.
$\overline{TSx}$	Open drain output which pulses low during the period when the Dx output is enabled.
FS_R	Receive frame synchronization pulse input which enables BCLK to shift the PCM information into D_R. FS_R is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
D_R	Receive data input. PCM data is shifted into D_R during the receive timeslot determined by FS_R.
CCLK	Control clock used to shift control data into CI and out of CO during $\overline{CS}$ low.
$\overline{CS}$	Chip select input. Must be low to enable the shifting of control data into CI and out of CO.
CI	The serial control data input used to set the operating state of the module.
CO	The serial status output used to monitor the operating state of the module. CO is TRI-STATE when $\overline{CS}$ is high. See *Figure 3* for timing diagram.
$\overline{INTR}$	Open drain interrupt output. A logic low indicates a change in the status of the subscriber loop, or a change in thermal shutdown.
V_{BB}	Negative power supply. $V_{BB} = -5V \pm 5\%$. Decoupled by internal 0.047 μF to ground.
V_{CC}	Positive power supply. $V_{CC} = 5V \pm 5\%$. Decoupled by 0.047 μF to ground.
$\overline{RRLY}$	Ring Relay Driver. Controlled by State Control Data Word bit D4 (see Table I). It is automatically turned off when ring trip is detected.
$\overline{RLY1}$	General purpose relay driver controlled by State Control Data Word bit D5.
$\overline{RLY2}$	General purpose relay driver controlled by State Control Data Word bit D6.
GND1 GND2 GND3	Low voltage ground. V_{BB}, V_{CC} and all digital signals are referenced to these pins. These pins must be externally connected together close to the module. Collectively referenced as GND in electrical specifications.
V_{BAT}	Negative high voltage supply. $V_{BAT} = -42.5V$ to $-56V$.
RTN	High voltage ground return. V_{BAT} and all analog signals are referenced to this pin.
DC	Don't connect. Do not make external connections to these pins.

Functional Block Description

Functional Block	Description
Line Driver	The Line Driver is a differential output transconductance amplifier which provides the d.c. power and balanced a.c. signals to the subscriber line. The d.c. power is determined by the DC Loop Impedance Control circuit. The a.c. signal applied to the line is controlled by the AC Loop Impedance Control and the analog signal generated by the TP3054 COMBO CODEC/Filter from the received PCM information. Feedback from the Tip and Ring lines produces an effective longitudinal input impedance of about 150Ω from TIP and RING to RTN (75Ω total). In the presence of large longitudinal current, each output of the Line Driver is capable of sourcing or sinking current to limit the longitudinal voltage.
Line Receiver	The Line Receiver monitors the metallic (differential) voltage on the line in the presence of large longitudinal (common mode) voltages.
Loop Impedance Control	The Loop Impedance Control feeds back the line voltage to produce a resistive/inductive d.c. feed impedance for longer loops and a constant current d.c. feed for shorter loops while maintaining an a.c. 2-wire input impedance of 900Ω + 2.16 μF over the voice band, easily meeting the 2-wire return loss requirements.
Hybrid Balance Control	The Hybrid Balance Control circuit consists of four software selectable networks, assuring that the 4-wire return loss requirements are met for a variety of conditions.
Loop Supervision	The Loop Supervision circuit monitors the d.c. current flow in the subscriber loop under non-ringing state and detects on-hook, off-hook and replicates dial pulses.
Ring Supervision	The Ring Supervision circuit monitors the d.c. current flow in the subscriber loop during the ringing state. This circuit is capable of detecting an off-hook condition in less than 200 ms in the presence of large a.c. ringing signals. It operates on loops with ringing superimposed on TIP or RING, or with balanced ringing. This supports bridged ringers, ringers to ground on either TIP or RING and with superimposed ringers.
Relay Drivers	The three relay drivers are capable of driving +5V or +12V relays directly. $\overline{\text{RRLY}}$ is dedicated to the ring relay and is automatically turned off when ring trip is detected by the Ring Supervision circuit. $\overline{\text{RLY1}}$ and $\overline{\text{RLY2}}$ are general purpose. Relay current is returned to GND3 at pin 26.
COMBO	The COMBO CODEC/Filter provides the PCM filtering, encoding and decoding functions necessary to interface the PCM highway to the analog signals on the subscriber loop. This function is identical to the industry standard TP3054 COMBO CODEC/Filter (see the TP3054 datasheet for full details).
Control Interface	The Control Interface circuit provides easy control and monitoring of the state of the TP3212 via a simple serial interface. Through this circuit the user can program the operating mode of the module, and monitor the line status (see Table I for details).

Functional Description

POWER-ON

When power is first applied, the power-on reset circuitry initializes the TP3212 and places it in a standby mode. The State Control Data Word is cleared to "0". All unnecessary circuitry is powered down. The serial control interface and the loop supervision circuitry remain fully functional. The device is now ready for activation, either by the user programming it into the ring mode by writing into the State Control Data Word or by the subscriber going off-hook, powering-up the device automatically.

THE STATE CONTROL DATA WORD

The State Control Data word is a single eight-bit word as shown in Table I. Bits D0–D7 of the control word program the operating state of the device. The module can initialize the power denial mode by itself in order to protect itself from damage under a thermal overload condition.

STATUS WORD

The eight-bit Status Word indicates the status of the TP3212 at the instant a read operation is performed. Table IV shows the definitions of the status word. A logic high indicates that the state or function is enabled, a low indicates that it is disabled.

THE CONTROL INTERFACE

The Control Interface consists of a single eight-bit shift register and a buffer register. The shift register is written via the serial input CI, under the control of $\overline{\text{CS}}$ and CCLK, to program the device's operating state. Several bits of the shift register may be altered by the device itself in response to changes in the subscriber loop status. These changes in

Functional Description (Continued)

state may be read via the serial output CO. The S2 and S3 status bits are over-written by the occurrence of a thermal overload, forcing the device into the Power-Denial mode. S7 is the hook-switch status bit. A logic "0" for S7 indicates an Off-Hook at normal mode or Ring-Trip at ring mode at the instant of accessing the control interface and a logic "1" indicates on-hook. Any changes in line status, or thermal shutdown condition will generate an interrupt at $\overline{INTR}$ output.

TABLE I. State Control Data Word

Control Bit	Description
D7	Selects loop detector's thresholds. Must be programmed to "0" for loop start and "1" for ground start. This bit is overwritten by the line supervision circuitry.
D6	Logical "1" enables $\overline{RLY2}$.
D5	Logical "1" enables $\overline{RLY1}$.
D4	Logical "1" enables Ring mode, turns on $\overline{RRLY}$ and Ring Supervision circuit. Status Bit S7 indicates ring-trip. Logical "0" enables the normal mode.
D3	Used with D2 to select Power denial, Battery Reversal or On-Hook Transmission modes. See Table II. Under Power Denial mode, the Line Drivers are disabled, denying power to the subscriber loop. It can be set or cleared by a write operation. Under a thermal overload condition, D3 is forced to "1" and D2 is forced to "0" in order to protect the device from damage. As long as the thermal overload condition exists, the Power Denial mode cannot be cleared by a write operation.
D2	Used with D3 to select Power denial, Battery Reversal or On-Hook Transmission modes. See Table II.
D1	Used with D0 to select hybrid balance network. See Table III.
D0	Used with D1 to select hybrid balance network. See Table III.

TABLE II. Operating Modes of TP3212

D4	D3	D2	Mode
0	0	0	Normal
0	0	1	Reverse Battery
0	1	0	Power Denial
0	1	1	On-Hook Transmission
1	x	x	Ring

TABLE III. Hybrid Balance Test Networks

D1	D0	Reference Test Network
0	0	900Ω
0	1	1650Ω//(100Ω + 0.005 μF)
1	0	800Ω//(100Ω + 0.05 μF)
1	1	900Ω + 2.16 μF

There are several ways of accessing the serial control interface. They are:

a) Write/Read
b) Read/Write
c) Quick Status Read

In the Write/Read operation, the objective is to change the state of the device. While shifting the new state control data into CI, the previous status information is shifted out of CO. This data should be compared with the previous status information to determine if a change had occurred since the last access.

In the Read/Write operation, the objective is to monitor the state of the module. While the current status is shifted out at CO, the last known state of the device is shifted into CI externally. If a thermal overload condition has occurred since the last access, the device will automatically set itself to the power denial mode (S3 bit will be forced to "1" and S2 will be forced to "0") prior to the access and will be reset by writing the previous state. This has no detrimental effect, however, since the power-denial mode will immediately be set again and the device will remain in the Power-Denial mode as long as the thermal overload continues to exist. If ring trip has occurred or the hook switch status has changed since the last access, the S7 bit will also be altered by the device. The timing for the Write/Read or Read/Write modes is shown in *Figure 2*.

The Quick Status Read operation allows a fast read of the S7 status bit, which indicates if a Ring-Trip or Off-Hook condition exists. It does not cause the shift register to shift, thus no control data is required. *Figure 3* is the timing diagram for the Quick Status Read Mode.

Functional Description (Continued)

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TABLE IV. Status Information Word

Status Bit	Description
S7	Indicates switch hook status. S7 is a "1" if the subscriber is on-hook. If D4 is programmed to be "0" for normal mode, a logic "0" at S7 indicates off-hook. If the device is in the Ring mode (D4 = "1"), a logic "0" at S7 indicates ring-trip.
S6	A logic "1" indicates that $\overline{RLY2}$ is on.
S5	A logic "1" indicates that $\overline{RLY1}$ is on.
S4	A logic "1" indicates Ring mode is on. $\overline{RRLY}$ is turned on, and the Ring Supervision circuit is activated. A logic "0" at S7 indicates that a ring trip has occurred, forcing $\overline{RRLY}$ to be de-activated. D4 should be cleared to "0" by a write/read operation in order to program the device into the non-ringing mode.
S3	S2 and S3 indicate Power Denial, Battery Reversal, or On-Hook Transmission mode (see Table II). When an overload condition exists which raises the junction temperature to exceed about 170°C, the TP3212 will automatically initiate a power denial mode (S3 forced to "1" and S2 forced to "0") to protect itself from damage. The device will not go back to the normal mode even if the thermal overload ceases to exist. The system can determine if the thermal overload condition has cleared itself by programming the TP3212 into the desired operating mode and read back status bits S2 and S3. If the overload still exists, the power denial mode will be activated again as long as the device's junction temperature exceeds approximately 170°C.
S2	S2 and S3 indicate Power Denial, Battery Reversal, or On-Hook Transmission mode (see Table II).
S1	Indicates the selected hybrid balance test network as shown in Table III.
S0	Indicates the selected hybrid balance test network as shown in Table III.

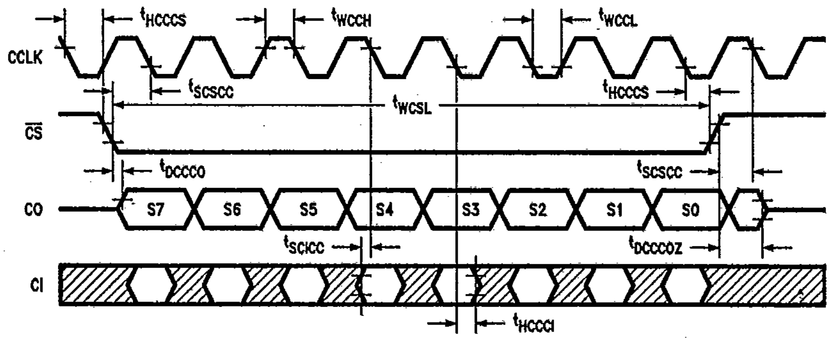

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FIGURE 2. Control Interface Timing—Write/Read or Read/Write Modes

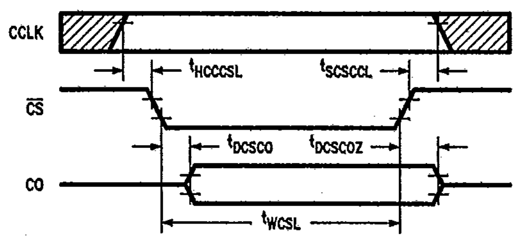

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FIGURE 3. Control Interface Timing—Quick Status Read Mode

Functional Description (Continued)

BATTERY FEED

With $V_{BAT} = -52V$, the TP3212 provides a nominal apparent battery voltage of −44.9V across TIP and RING. The module provides a resistive/inductive feed at longer loops. The d.c. current feed has been designed to guarantee 20 mA into an 1800Ω loop at nominal battery, and 18 mA into a 1600Ω loop at minimum battery of −42.5V. At shorter loops, the d.c. feed is current-limited to nominally 43 mA in order to conserve power. At normal battery polarity (D3 = 0 and D2 = 0), TIP is more positive than RING. The current feed characterisitc is shown in *Figure 4.*

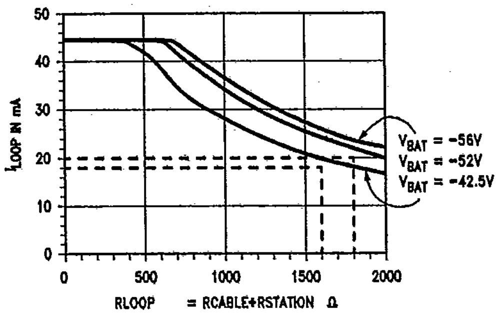

FIGURE 4. d.c. Feed Characteristics

2-WIRE IMPEDANCE

The nominal 2-wire input impedance is 900Ω + 2.16 μF. This is shunted by the feeding inductance which is nominally 26 Henries on long loops, and approaches infinity on short loops.

TRANSMISSION LEVEL

The 0 TLP is referenced at the PCM interface of the four wire ports. The TP3212 module has 2 dB loss for both transmit and receive signals. On the 2-wire analog interface, the transmit is +2 TLP and the receive is −2 TLP. TLP is defined as 0 dBm into 900Ω.

HYBRID BALANCE

The Hybrid Balance Control circuit contains four selectable balance networks which are selected by programming State Control Word bits D0 and D1. The balance networks are intended to be used with the corresponding reference test networks for hybrid balance as shown in Table III.

LONGITUDINAL BALANCE AND LONGITUDINAL CURRENT CAPABILITY

The 2-wire input of the device exhibits a longitudinal impedance of 150Ω from TIP to ground and from RING to ground. These impedances are extremely well matched and are not strongly dependent on impedance matching in the external protection network. The longitudinal voltage is sensed on the loop side of the protection network and fed back to the Line Driver, thus any component variations external to the device can be corrected by the feedback loop. The Line Driver is capable of handling 21 mA_{rms} of longitudinal current in each of the TIP and RING leads.

LOOP SUPERVISION

The Loop Supervision circuit operates in the normal (non-ringing) state. When control bit D7 is programmed to logic 0, it enables loop start signalling and a dynamic threshold comparator in order to maintain the dial pulse break interval within 46% to 74% regardless of the distortion introduced by the loop characteristics. The output of the Loop Impedance Control is monitored and off-hook indicated when the loop current exceeds nominally 13 mA and on-hook indicated when the current falls below nominally 11 mA, providing a 2 mA hysteresis. A logic "1" at status bit S7 indicates on-hook, while a logic "0" indicates off-hook. When control bit D7 is programmed to logic "1", it adjusts the loop comparator's thresholds for ground start signalling. Off-hook is indicated when the current from RING to Ground (with TIP open) exceeds nominally 17 mA and on-hook when the current falls below nominally 13 mA.

A typical example of hook switch timing is illustrated in *Figure 5.* While in the standby mode, all unnecessary circuitry is powered down. When Loop Supervision detects off-hook, the module is powered up, $\overline{INTR}$ goes low and status bit S7 is cleared (A). The $\overline{INTR}$ remains active until $\overline{CS}$ goes low and status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). When the Loop Supervision detects on-hook, all unnecessary circuitry is again powered down, status bit S7 is set and $\overline{INTR}$ is again set low (C). When the status information is read, the present switch hook status is latched, clearing the interrupt, and $\overline{INTR}$ goes high (D). In the case of either on-hook or off-hook, if the system fails to read the status before the switch hook reverts to its previous state, the interrupt will clear itself (E). If the device's control interface is being accessed when off-hook occurs, i.e., $\overline{CS}$ is low, $\overline{INTR}$ is set low immediately (F) but S7 is cleared only after $\overline{CS}$ returns high (G). On the next Read/Write access, S7 is latched.

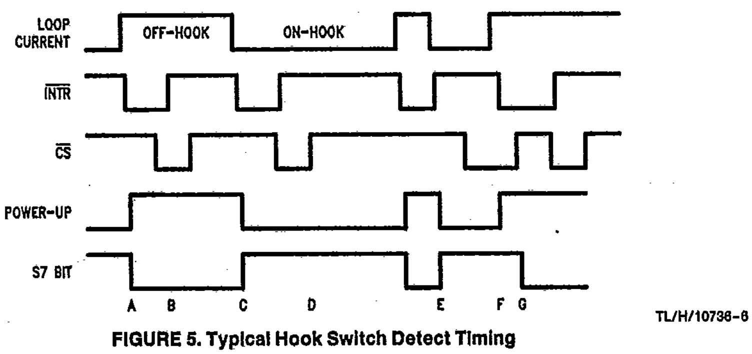

FIGURE 5. Typical Hook Switch Detect Timing

Functional Description (Continued)

RING SUPERVISION

The Ring Supervision circuit measures the loop current across two 360Ω ring sensing resistors with a 1 MΩ internal resistive bridge (see *Figure 10*). The voltage at the output of the bridge is filtered, then algebraically added and subtracted from a voltage corresponding to a loop current of about 11 mAdc. Each of the resulting voltages are integrated over one period of the ring frequency and compared to zero. If either of the resulting voltages is less than zero for two consecutive cycles, ring-trip is detected. $\overline{RRLY}$ is de-activated, status bit S7 is cleared to "0" indicating ring trip, and an interrupt is also generated. Control bit D4 (RING) is not automatically reset to "0", it has to be cleared to "0" by a write/read operation after a ring trip is detected. If the MCLK is interrupted and stays continuously high or low for more than 200 μs, the ring relay driver will be turned off.

The ring supervision circuit works with zero to five bridged ringers (1 ringer = 7 kΩ at 20 Hz), with ring frequencies from 16 to 67 Hz, with ring voltages from 90 to 155 Vrms applied to either TIP or RING, superimposed on positive or negative battery voltages of from 42 to 56 volts on loops up to 1700Ω. Furthermore, it operates with up to five ringers connected from TIP or RING to ground or with up to three superimposed ringers connected from TIP to ground and three from RING to ground with a battery voltage of ±38 ±2V. The ring sensing inputs at TIPS, RINGS, RBUS+ and RBUS− when connected as shown in *Figure 10,* will present an effective load of about 500 kΩ across the ring bus.

A typical example of ring trip timing is illustrated in *Figure 6.* When the Ring Supervision circuit detects a ring trip, the device immediately turns off $\overline{RRLY}$, clears S7 and sets $\overline{INTR}$ low (A). The interrupt remains active until $\overline{CS}$ goes low and the status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). Status bit S7 will remain a zero until the D4 bit is written to a zero, removing the device from the RING mode (C). At this time, the S7 bit will indicate the switch hook status. Even though the station equipment is normally off-hook at this time, S7 will generally return to a "1" (C) for several milliseconds after D4 is cleared. This is because the Loop Supervision circuit was disconnected from the loop during ringing mode (D4 = 1), and it takes several milliseconds to detect the off hook at which time S7 will be cleared and $\overline{INTR}$ will be set low (D). At this point the device is in the normal (non-ringing) mode, all necessary circuitry is powered up.

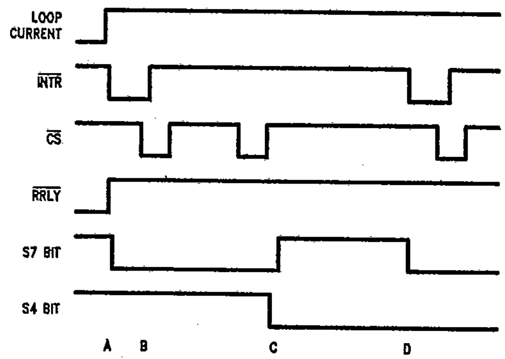

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FIGURE 6. Typical Ring Trip Detect Timing

THERMAL OVERLOAD

The Line Driver incorporates a built-in thermal overload detection circuitry. In the event of a fault on the subscriber line which causes the Line Driver to reach an internal junction temperature of approximately 170°C, the Line Driver will protect itself by forcing the device into the power-denial mode, S3 is forced to "1" and S2 is forced to "0". The device will remain at the power denial mode even though the thermal overload ceases to exist. After the line fault has been corrected, the device can be put back into service under system control (see Table IV).

A typical example of thermal overload detection timing is illustrated in *Figure 7.* When a thermal overload is detected, S3 is set high and S2 is set low (A), forcing the device into the Power-Denial mode, and $\overline{INTR}$ is set low. The interrupt remains active until $\overline{CS}$ goes low, clearing $\overline{INTR}$ (B). As long as the thermal overload condition exists, the power denial mode cannot be reset by a write operation (B). When the thermal overload condition clears, the $\overline{INTR}$ will again be set low, but the device continued to remain at power denial mode (C). Thus the device does not automatically re-apply power to the line since the fault that originally caused the failure may still exist and would simply cause the overload to re-occur. In this example, the power denial mode is cleared by a control write to normal mode, clearing S2 and S3 to "0" (D). If the device is being accessed at the instant the thermal shutdown indication occurs, $\overline{INTR}$ is set low immediately, but S3 will be set high and S2 will be set low only after $\overline{CS}$ returns high (E).

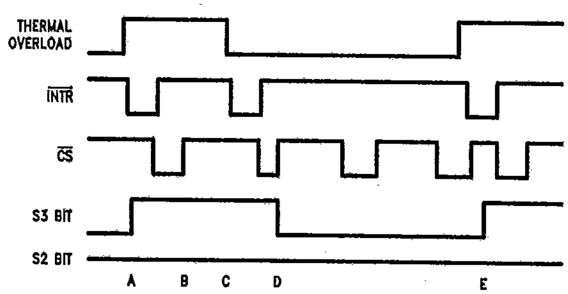

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FIGURE 7. Typical Thermal Overload Detection Timing

Functional Description (Continued)

ON-HOOK TRANSMISSION MODE

The device is in the on-hook transmission mode when bit D3 and D2 of the State Control Data Word is set to the logic "1" and the loop is under "on-hook". In this mode, the line drivers operate in a reduced power state but all circuitry is active. This enables the system to communicate with a subscriber terminal or the subscriber to communicate through the network or to a terminal in the central office to provide alarm and telemetry services. When the loop goes off-hook, the loop supervision circuitry behaves normally and causes the line drivers to power up. Bit S7 of the Status Information Word is cleared and an interrupt is initiated. This enables the system to terminate any transmissions and handle the call initiation in the normal manner.

PCM INTERFACE

The PCM interface consists of inputs MCLK, BCLK, FSx, FS_R and D_R, and outputs Dx and $\overline{TSx}$. MCLK controls the internal operation of the COMBO CODEC/Filter's encoder and decoder, and must be 1.536 or 1.544 MHz if CLKSEL is connected high and 2.048 MHz if CLKSEL is connected low. BCLK shifts the PCM data out of Dx on its rising edge and latches the PCM data into D_R on its falling edge. It must be synchronous with MCLK and may be any integer multiple of 8 kHz from 64 kHz to 2.048 MHz. FSx and FS_R are 8 kHz pulse waveforms which determine the beginning of the PCM data transfer out of Dx and into D_R respectively. Both must be synchronous with MCLK but may have any phase relationship with each other. $\overline{TSx}$ is an open drain output which pulses low for the duration of the data transfer out of Dx. It is intended to be wire-ORed with the $\overline{TSx}$ outputs of other subscriber line interface modules to provide an enable signal for external TRI-STATE drivers buffering the PCM transmit data from a line card onto the backplane.

Short Frame Sync Operation

The TP3212 Subscriber Line Interface Module can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, the frame sync pulses applied to both FSx and FS_R must be one BCLK period long and with timing relationships as specified in *Figure 8*. With FSx high during a falling edge of BCLK, the next rising edge of BCLK enables the Dx TRI-STATE output buffer, which will output the PCM sign bit. The following seven rising edges of the bit clock shifts out the remaining seven bits of PCM data, MSB first. The next falling edge disables the Dx output. With FS_R high during a falling edge of BCLK, the next falling edge latches the PCM sign bit into D_R. The next seven falling edges latch the remaining seven bits, MSB first.

Long Frame Sync Operation

To use the long frame sync mode, the frame sync pulses applied to both FSx and FS_R must be three or more bit periods long, with timing relationships as specified in *Figure 9*. Based on the transmit frame sync pulse, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The Dx TRI-STATE output buffer is enabled with the rising edge of FSx or the rising edge of BCLK, whichever comes later, and the first bit clocked out is the PCM sign bit. The following seven rising edges of BCLK shift out the remaining seven bits, MSB first. The Dx output is disabled by the falling edge of BCLK following the eighth rising edge or by FSx going low, whichever comes later. A rising edge of the receive frame sync will cause PCM data at D_R to be latched in on the next eight falling edges of BCLK.

Functional Description (Continued)

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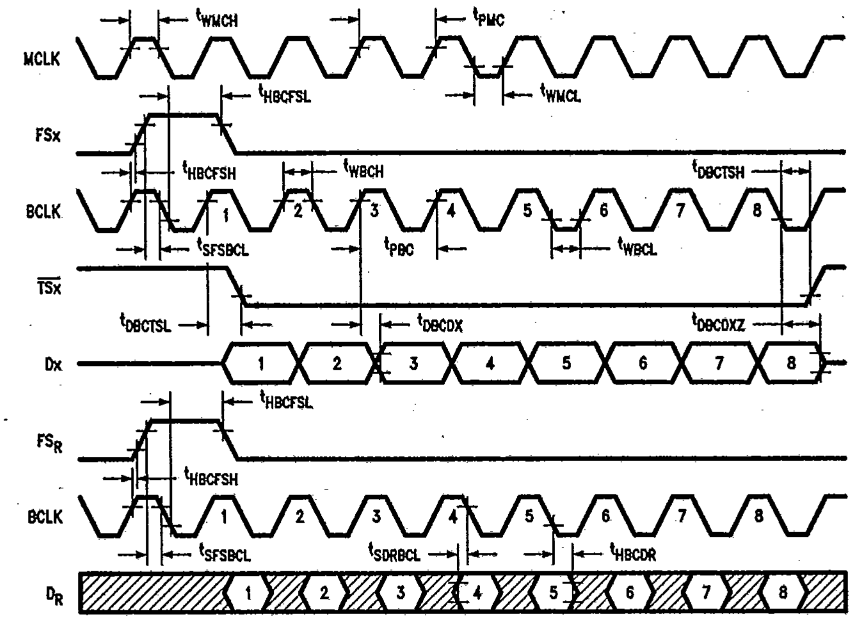

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FIGURE 8. Timing Diagram for Short Frame Mode

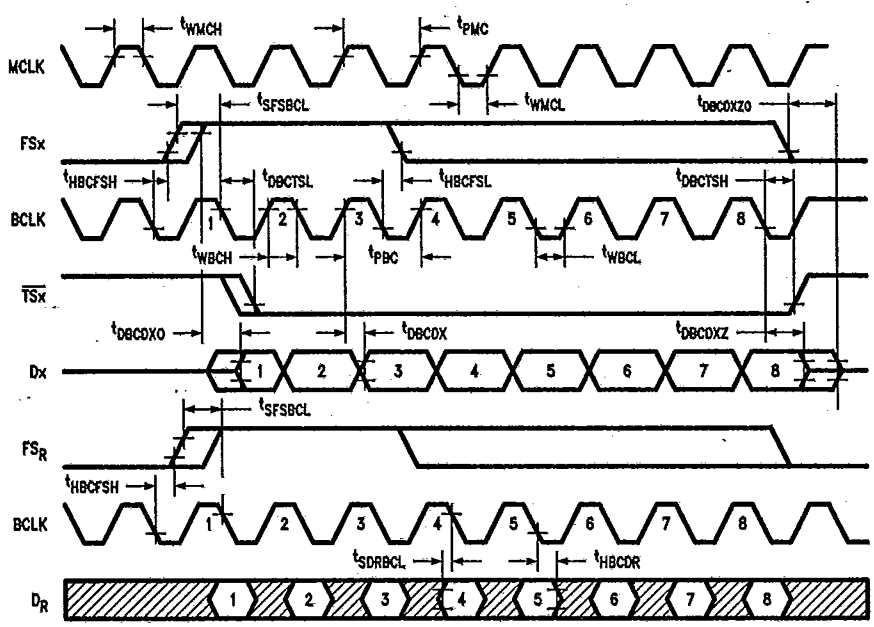

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FIGURE 9. Timing Diagram for Long Frame Mode

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	−0.5V to 7V
V_{BB} to GND	0.5V to −7V
V_{BAT} to RTN	0.5V to −70V
RTN to GND	±500V, 10 μs/50 μs Pulse
Voltage at any digital input or output	V_{CC} + 0.3V to GND − 0.3V
TPR, RPR to RTN	2V to −85V (50 ms)
TIP, RING, TIPS, RINGS, RBUS+, RBUS− to RTN	±1000V, 10 μs/1000 μs Pulse
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature	150°C

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (Normal Mode: D2 = 0, D3 = 0)						
$I_{BAT}0$	V_{BAT} Idle Current	I_{LOOP} = 0 mA, V_{BAT} = −52V		2.1	**4.0**	mA
$I_{BB}0$	V_{BB} Idle Current	I_{LOOP} = 0 mA		1.9	**3.6**	mA
$I_{CC}0$	V_{CC} Idle Current	I_{LOOP} = 0 mA		2.9	**5**	mA
$I_{BAT}1$	V_{BAT} Active Current	I_{LOOP} = 20 mA, V_{BAT} = −52V		23	**25**	mA
$I_{BB}1$	V_{BB} Active Current	I_{LOOP} = 20 mA		8.9	**17.2**	mA
$I_{CC}1$	V_{CC} Active Current	I_{LOOP} = 20 mA		11.8	**17.2**	mA
POWER DISSIPATION (On-Hook Transmission Mode: D2 = 1, D3 = 1)						
$I_{BAT}OH$	V_{BAT} Idle Current	I_{LOOP} = 0 mA, V_{BAT} = −52V		2.1	**4.0**	mA
$I_{BB}OH$	V_{BB} Idle Current	I_{LOOP} = 0 mA		8.9	**17.2**	mA
$I_{CC}OH$	V_{CC} Idle Current	I_{LOOP} = 0 mA		11.8	**17.2**	mA
DIGITAL INTERFACE (Note 1)						
V_{IL}	Input Low Level	All Digital Inputs			**0.7**	V
V_{IH}	Input High Level	All Digital Inputs except CLKSEL CLKSEL	**2** **4**			V V
V_{OL}	Output Low Level	Dx, $\overline{TSx}$, CO, I_L = 3.2 mA $\overline{INTR}$, I_L = 2.0 mA			**0.4** **0.4**	V V
V_{OH}	Output High Level	Dx, CO, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GND < V_{IN} < V_{IL}, All Digital Inputs	**−100**		**100**	μA
I_{IH}	Input High Current	V_{IH} < V_{IN} < V_{CC}, All Digital Inputs	**−100**		**100**	μA
I_{OH}	Output High Current	$\overline{TSx}$ and $\overline{INTR}$, V_{OH} < V_{OUT} < V_{CC}	**−100**		**100**	μA
I_{OZ}	Output Current in the High Impedance State	CO, Dx	**−100**		**100**	μA

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Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
BATTERY FEED						
I_{LOOP+}	Loop Current Normal Battery	R_{LOOP} = 1800Ω, V_{BAT} = −52V R_{LOOP} = 1600Ω, V_{BAT} = −42.5V R_{LOOP} = 100Ω, V_{BB} = −4.75V (Note 2)	**20** **18** 40	21.3 19.2 43	**24** **22** 46	mA mA mA
I_{LOOP-}	Loop Current Reverse Battery	R_{LOOP} = 1800Ω, V_{BAT} = −52V R_{LOOP} = 1600Ω, V_{BAT} = −42.5V R_{LOOP} = 100Ω, V_{BB} = −4.75V (Note 2)	**20** **18** 40	21.3 19.2 43	**24** **22** 46	mA mA mA
I_{PD}	Power Denial Loop Current	R_{LOOP} = 100Ω		0.1	**2**	mA
V_{LOOP}	Loop Voltage	R_{LOOP} = 10 kΩ, V_{BAT} = −52V		−43.4		V
LOOP SUPERVISION						
$R_{OFFHK}0$	Loop Resistance to Produce an Off-Hook Indication at Loop Start	$R_{OFFHK}0$ Connected from TIP to RING V_{BAT} = −42.5V D7 = 0			**2000**	Ω
$R_{ONHK}0$	Loop Resistance to Produce an On-Hook Indication at Loop Start	$R_{ONHK}0$ Connected from TIP to RING V_{BAT} = −56V D7 = 0	**9**			kΩ
$R_{OFFHK}1$	Loop Resistance to Produce an Off-Hook Indication at Ground Start	$R_{OFFHK}1$ Connected from RING to RTN, TIP Open V_{BAT} = −42.5V D7 = 1			**1330**	Ω
$R_{ONHK}1$	Loop Resistance to Produce an On-Hook Indication at Ground Start	$R_{ONHK}1$ Connected from RING to RTN, TIP Open V_{BAT} = −56V D7 = 1	**9**			kΩ
DPD	Dial Pulse Distortion	D7 = 0, R_{LEAK} = 15 kΩ R_{LOOP} = 100Ω, 12 pps, Break = 58% R_{LOOP} = 1800Ω, 12 pps, Break = 64%, $\overline{CS}$ High, Measure Width of Break Period at $\overline{INTR}$	38.4 **38.4**		61.5 **61.5**	ms ms
RING SUPERVISION						
RNGTRP1	Ring Trip Detect, Normal Ringing	RBUS+ = 0V, RBUS− = −48V, TIPS = −5V, RINGS = −43V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms
RNGTRP2	Ring Trip Detect, Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −43V, RINGS = −5V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms
RNGTRP3	Ring Trip Non-Detect, Normal Ringing	RBUS+ = 0V, RBUS− = −48V, TIPS = −3V, RINGS = −45V, Must Not Detect Ring Trip within the Specified Time (Note 3)	**0**		**180**	ms

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Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
RING SUPERVISION (Continued)						
RNGTRP4	Ring Trip Non-Detect, Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −45V, RINGS = −3V, Must Not Detect Ring-Trip within the Specified Time (Note 3)	**0**		**180**	ms
RNGTRP5	Ring Trip Detect, Normal Ringing	TIPS, RBUS− = −5V, RINGS, RBUS+ = 26 Vrms, f = 20 Hz Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP6	Ring Trip Detect, Reverse Ringing	TIPS, RBUS− = 26 Vrms, RINGS, RBUS+ = −5V, f = 20 Hz Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP7	Ring Trip Non-Detect, Normal Ringing	TIPS, RBUS− = −3V, RINGS, RBUS+ = 26 Vrms, f = 20 Hz Must Not Detect Ring-Trip within the Specified Time (Note 3)	**0**		**190**	ms
RNGTRP8	Ring Trip Non-Detect, Reverse Ringing	TIPS, RBUS− = 26 Vrms, RINGS, RBUS+ = −3V, f = 20 Hz Must Not Detect Ring-Trip within the Specified Time (Note 3)	**0**		**190**	ms
HYBRID BALANCE Unless otherwise specified, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
ECHO1	4-Wire Return Loss	Z_{REF} = 900Ω across Tip-Ring D1 = 0, D0 = 0				
		f = 203.125 Hz	**21**			dB
		f = 484.375 Hz	**26**			dB
		f = 1015.625 Hz	**26**	40		dB
		f = 2500 Hz	**26**			dB
		f = 3406.25 Hz	**21**			dB
ECHO2	4-Wire Return Loss	Z_{REF} = 1650Ω//(100Ω + 0.005 μF) D1 = 0, D0 = 1				
		f = 203.125 Hz	**21**			dB
		f = 484.375 Hz	**26**			dB
		f = 1015.625 Hz	**26**	40		dB
		f = 2500 Hz	**26**			dB
		f = 3406.25 Hz	**21**			dB

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Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
HYBRID BALANCE Unless otherwise specified, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
ECHO3	4-Wire Return Loss	Z_{REF} = 800Ω//(100Ω + 0.05 μF) D1 = 1, D0 = 0 f = 203.125 Hz f = 484.375 Hz f = 1015.625 Hz f = 2500 Hz f = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40		 dB dB dB dB dB
ECHO4	4-Wire Return Loss	Z_{REF} = 900Ω + 2.16 μF D1 = 1, D0 = 1 f = 203.125 Hz f = 484.375 Hz f = 1015.625 Hz f = 2500 Hz f = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40		 dB dB dB dB dB
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
RTNLOSS	2-Wire Return Loss	f = 203.125 Hz f = 484.375 Hz f = 1015.625 Hz f = 2500 Hz f = 3406.25 Hz	**21** **27** **27** **27** **27**	 40		dB dB dB dB dB
0 dBm0	The Absolute 2-Wire Reference Level	The Absolute Reference Level at the Two Wire Interface is +2 dBm/900Ω for Transmit, and −2 dBm/900Ω for Receive. Transmit (2-Wire to Dx) Receive (D_R to 2-Wire)		 1.194 0.754		 Vrms Vrms
G_{RA}	Absolute Receive Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V T_A = 25°C, D_R to 2-Wire Port, Input = Digital Code for 0 dBm0 at D_R, Measure Voltage across TIP-RING	**−0.25**		**0.25**	dB
G_{XA}	Absolute Transmit Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V T_A = 25°C, 2-Wire Port to Dx, Input = 0 dBm0 at 2-Wire Port, Measure Digital Code at Dx	**−0.25**		**0.25**	dB
G_{RAOH}	Absolute Receive Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V Z_{REF} = 900Ω + 2.16 μF D3 = 1, D2 = 1, I_{LOOP} = 0 mA D_R to 2-Wire	**−1**		**1**	dB
G_{XAOH}	Absolute Transmit Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V from 2-Wire Analog Interface to Dx D3 = 1, D2 = 1, I_{LOOP} = 0 mA	**−1**		**1**	dB
G_{RAV}	Absolute Receive Gain Over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%, V_{BAT} = −42.5V to −56V	**−0.3**		**0.3**	dB
G_{XAV}	Absolute Transmit Gain Over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%, V_{BAT} = −42.5V to −56V	**−0.3**		**0.3**	dB

Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
G_{RT}	Receive Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V Reference to G_{RA}	−0.15		0.15	dB
G_{XT}	Transmit Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V Reference to G_{XA}	−0.15		0.15	dB
G_{RF}	Receive Frequency Response	Measure Relative to G_{RA}				
		f = 203.125 Hz	**−1.9**		**0**	dB
		f = 296.875 Hz	**−0.4**		**0.25**	dB
		f = 484.375 Hz	**−0.25**		**0.25**	dB
		f = 2015.625 Hz	**−0.25**		**0.25**	dB
		f = 2703.125 Hz	**−0.25**		**0.25**	dB
		f = 3015.625 Hz	**−0.25**		**0.25**	dB
		f = 3203.125 Hz	**−0.25**		**0.25**	dB
		f = 3390.625 Hz	**−1.2**		**0**	dB
		f = 3984.375 Hz			**−14**	dB
SOS	Spurious Out of Band Signals (Alias Tones)	Measure Relative to G_{RA}				
		f = 4796.875 Hz			**−30**	dB
		f = 6703.125 Hz			**−30**	dB
		f = 11390.625 Hz			**−30**	dB
G_{XF}	Transmit Frequency Response	Measure Relative to G_{XA}				
		f = 62.500 Hz			**−21**	dB
		f = 203.125 Hz	**−2.5**		**0**	dB
		f = 296.875 Hz	**−0.4**		**0.25**	dB
		f = 484.375 Hz	**−0.25**		**0.25**	dB
		f = 2015.625 Hz	**−0.25**		**0.25**	dB
		f = 2703.125 Hz	**−0.25**		**0.25**	dB
		f = 3015.625 Hz	**−0.25**		**0.25**	dB
		f = 3202.125 Hz	**−0.25**		**0.25**	dB
		f = 3390.625 Hz	**−1.2**		**0**	dB
		f = 3984.375 Hz			**−14**	dB
		f = 5046.875 Hz			**−32**	dB
		f = 11890.625 Hz			**−32**	dB
G_{RL}	Receive Gain Variation with Signal Level	Measure Relative to G_{RA} PCM Level				
		= 3.1 dBm0	**−0.25**		**0.25**	dB
		= −2.3 dBm0	**−0.25**		**0.25**	dB
		= −11.4 dBm0	**−0.25**		**0.25**	dB
		= −17.6 dBm0	**−0.25**		**0.25**	dB
		= −23.9 dBm0	**−0.25**		**0.25**	dB
		= −29.9 dBm0	**−0.25**		**0.25**	dB
		= −37.8 dBm0	**−0.25**		**0.25**	dB
		= −47.1 dBm0	**−0.45**		**0.45**	dB
		= −55.7 dBm0	**−1.3**		**1.3**	dB

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Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
G_{XL}	Transmit Gain Variation with Signal Level	Measure Relative to G_{XA} PCM Level				
		= 3.1 dBm0	**−0.25**		**0.25**	dB
		= −2.3 dBm0	**−0.25**		**0.25**	dB
		= −11.4 dBm0	**−0.25**		**0.25**	dB
		= −17.6 dBm0	**−0.25**		**0.25**	dB
		= −23.9 dBm0	**−0.25**		**0.25**	dB
		= −29.9 dBm0	**−0.25**		**0.25**	dB
		= −37.8 dBm0	**−0.25**		**0.25**	dB
		= −47.1 dBm0	**−0.45**		**0.45**	dB
		= −55.7 dBm0	**−1.3**		**1.3**	dB
STD_R	Receive Signal to Total Distortion	Measure through C Message Filter PCM Level				
		= 3.1 dBm0	**33**			dBC
		= 0.0 dBm0	**36**			dBC
		= −2.3 dBm0	**36**			dBC
		= −11.4 dBm0	**36**			dBC
		= −17.6 dBm0	**36**			dBC
		= −23.9 dBm0	**36**			dBC
		= −29.9 dBm0	**35**			dBC
		= −37.8 dBm0	**30**			dBC
		= −40.0 dBm0	**28**			dBC
		= −45.0 dBm0	**24**			dBC
		= −47.1 dBm0	**22**			dBC
		= −55.7 dBm0	**13**			dBC
STD_X	Transmit Signal to Total Distortion	Measure through C Message Filter PCM Level				
		= 3.1 dBm0	**33**			dBC
		= 0.0 dBm0	**36**			dBC
		= −2.3 dBm0	**36**			dBC
		= −11.4 dBm0	**36**			dBC
		= −17.6 dBm0	**36**			dBC
		= −23.9 dBm0	**36**			dBC
		= −29.9 dBm0	**35**			dBC
		= −37.8 dBm0	**30**			dBC
		= −40.0 dBm0	**28**			dBC
		= −45.0 dBm0	**24**			dBC
		= −47.1 dBm0	**21**			dBC
		= −55.7 dBm0	**12**			dBC
D_{RA}	Absolute Receive Delay	f = 1600 Hz		190		μs

Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
D_{RR}	Receive Delay Distortion	Measure Relative to D_{RA} f = 500 Hz f = 1000 Hz f = 2600 Hz f = 2800 Hz f = 3000 Hz		 −2 −10 70 100 150		 μs μs μs μs μs
D_{XA}	Absolute Transmit Delay	f = 1600 Hz		300		μs
D_{XR}	Transmit Delay Distortion	Measure Relative to D_{XA} f = 500 Hz f = 600 Hz f = 800 Hz f = 1000 Hz f = 2600 Hz f = 2800 Hz f = 3000 Hz		 250 150 65 30 60 80 140		 μs μs μs μs μs μs μs
NOISE Z_{REF} = 900Ω + 2.16 μF, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
N_{RC}	Receive C Message Weighted Idle Channel Noise	PCM Code is Alternating Positive and Negative Zeroes		9	**13**	dBrnC
N_{XC}	Transmit C Message Weighted Idle Channel Noise	Measured by Extrapolation from Signal to Distortion Measurements about −50 dBm0		13	**17**	dBrnC
LONGITUDINAL BALANCE AND CAPABILITY						
$I_{LLS}1$	Longitudinal Current Capability, Loop Start	I_{LOOP} = 5 mA, D7 = 0, f = 60 Hz, Inject $I_{LLS}1$ into TIP and RING. Device Must Not Detect Off-Hook. Triangular Waveform	**21**			mArms
$I_{LLS}2$	Longitudinal Current Capability, Loop Start	I_{LOOP} = 21 mA, D7 = 0, f = 60 Hz, Inject $I_{LLS}2$ into TIP and RING. Device Must Not Detect On-Hook. Triangular Waveform	**21**			mArms
$I_{LGS}1$	Longitudinal Current Capability, Ground Start	f = 60 Hz, I_{GROUND} = 0 mA, D7 = 1 Triangular Waveform. Inject $I_{LGS}1$ into RING, TIP Open. Device Must Not Detect Off-Hook	**8.5**			mArms
$I_{LGS}2$	Longitudinal Current Capability, Ground Start	I_{GROUND} = 50 mA, f = 60 Hz. Inject $I_{LGS}2$ into RING, TIP Open. Device Must Not Detect On-Hook. Triangular Waveform, D7 = 1	50			mArms

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Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
LONGITUDINAL BALANCE AND CAPABILITY (Continued)						
BAL2W	2-Wire Longitudinal Balance	IEEE Method 455-1976, I_{LOOP} = 20 mA $I_{LONGITUDINAL}$ = 20 mArms/leg, Measure $V_{METALLIC}$ across TIP-RING				
		f = 62.5 Hz	**61**			dB
		f = 203.125 Hz	**61**	64		dB
		f = 1015.625 Hz	**61**	64		dB
		f = 2015.625 Hz	**61**			dB
		f = 2703.125 Hz	**56**			dB
		f = 3000 Hz	**54**	59		dB
		f = 3406.25 Hz	**51**			dB
POWER SUPPLY REJECTION RATIO Unless otherwise specified, Z_{REF} = 900 +2.16 μF, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
$PPSR_R$	V_{CC} Power Supply Rejection, Receive	V_{CC} = 5.0 V_{DC} +164 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**30**			dB
		f = 3328.125 Hz	**30**			dB
$VPSR_R$	V_{BAT} Power Supply Rejection, Receive	V_{BAT} = −52.0 V_{DC} +424 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**40**			dB
		f = 3328.125 Hz	**40**			dB
$PPSR_X$	V_{CC} Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} +164 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**30**			dB
		f = 3328.125 Hz	**30**			dB
$VPSR_X$	V_{BAT} Power Supply Rejection, Transmit	V_{BAT} = −52.0 V_{DC} +424 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**40**			dB
		f = 3328.125 Hz	**40**			dB
RELAY DRIVERS						
VR_{ON}	Driver On Voltage	I_L = 80 mA			**1**	V
IR_{OFF}	Leakage Current	V_{RELAY} = 40V, Relay Off			**100**	μA
DIGITAL TIMING, PCM INTERFACE (See *Figures 8* and *9*, Notes 4 and 5)						
$1/t_{PMC}$	MCLK Frequency	Clock Frequency Accuracy < ±100 ppm		1.536		MHz
				1.544		MHz
				2.048		MHz
t_{WMCH}	Width of MCLK High		**160**			ns
t_{WMCL}	Width of MCLK Low		**160**			ns
$1/t_{PBC}$	BCLK Frequency				**2.048**	MHz
t_{WBCH}	Width of BCLK High		**160**			ns
t_{WBCL}	Width of BCLK Low		**160**			ns

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Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SHORT FRAME SYNC MODE (*Figure 8*)						
t_{SFSBCL}	Setup Time from FS High to BCLK Low		**50**			ns
t_{HBCFSL}	Hold Time from BCLK Low to FS Low		**100**			ns
t_{HBCFSH}	Hold Time from BCLK Low to FS High		**0**			ns
t_{DBCDX1}	Delay Time from Bit Clock to Dx Data Valid	C_L = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
t_{DBCTSL}	Delay Time from BCLK to $\overline{TSx}$ Low	C_L = 150 pF plus 2 LSTTL Loads			**140**	ns
t_{SDRBCL}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
LONG FRAME SYNC MODE (*Figure 9*)						
t_{HBCFSH}	Hold Time from BCLK Low to FS		**0**			ns
t_{SFSBC0}	Setup Time from FS to BCLK Low		**95**			ns
t_{WFSL}	Width of FS Low		**160**			ns
t_{DBCDX0}	Delay Time from BCLK or FS, Whichever Comes Later, to Dx Valid	C_L = 150 pF plus 2 LSTTL Loads	**20**		**165**	ns
t_{DBCDX}	Delay Time from BCLK to Dx Valid	C_L = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
$t_{DBCDXz0}$	Delay Time from BCLK or FS, Whichever Comes Later, to Dx Disabled	C_L = 50 pF	**20**		**165**	ns
t_{SDRBC}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
DIGITAL TIMING, SERIAL CONTROL INTERFACE (See *Figures 2* and *3*, Notes 4 and 5)						
$1/t_{PCC}$	CCLK Frequency	Frequency Accuracy < ±100 ppm	0.08		**2.048**	MHz
t_{WCCH}	Width of CCLK High		**200**			ns
t_{WCCL}	Width of CCLK Low		**200**			ns
t_{WCSL}	Width of $\overline{CS}$ Low				**100**	μs

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
READ/WRITE, WRITE/READ MODES *(Figure 2)*						
t_{HCCCS}	Hold Time from CCLK to $\overline{CS}$		**100**			ns
t_{SCSCC}	Setup Time from $\overline{CS}$ to CCLK		**100**			ns
t_{DCCCO}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Valid	C_L = 150 pF plus 2 LSTTL Loads			**150**	ns
t_{DCCCOZ}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Disabled				**150**	ns
t_{SCCCI}	Setup Time from CI to CCLK		**100**			ns
t_{HCICC}	Hold Time from CCLK to CI		**100**			ns
t_{DCSIN}	Delay Time from $\overline{CS}$ Low to $\overline{INTR}$ High	R_L = 1 kΩ from $\overline{INTR}$ to V_{CC}			**200**	ns
QUICK STATUS READ MODE *(Figure 3)*						
t_{HCCCSL}	Hold Time from CCLK to $\overline{CS}$ Low		**100**			ns
t_{SCSCCL}	Setup Time from $\overline{CS}$ to CCLK Low		**100**			ns
t_{DCSCO}	Delay Time from $\overline{CS}$ to CO Valid	C_L = 150 pF plus 2 LSTTL Loads			**150**	ns
t_{DCSCOZ}	Delay Time from $\overline{CS}$ to CO Disabled				**150**	ns

Note 1: See Appendix I for the definition of digital interface parameters.

Note 2: Derate based on T_{JMAX} = 150°C, thermal resistance from junction of bipolar IC to heat spreader = 27°C/W, thermal resistance from heat spreader to ambient is 18°C/W at still air, and 11.5°C/W at 120 ft/min of air velocity.

Note 3: The intent of Ring Trip Non-Detect tests are to insure that ring trip does not occur under the specified conditions even after an essentially infinite period of time. For practical purposes of cost effectively testing the SLIM Subscriber Line Interface Module, the wait time to determine that a false ring trip has not occurred has necessarily been limited to a value which has been determined through characterization to insure that false ring trip never occurs.

Note 4: See Appendix I for the definition and naming conventions used for digital timing parameters.

Note 5: See Table V for the definition of the mneumonics used for the digital timing parameters.

TABLE V. Timing Parameter Mneumonics

Pin Name	Mneumonic
$\overline{INTR}$	IN
$\overline{CS}$	CS
CO	CO
CI	CI
CCLK	CC
MCLK	MC
BCLK	BC
D_R	DR
Dx	DX
$\overline{TSx}$	TS
FS_R	FS
FSx	FS

Applications Information

TYPICAL LINE CIRCUIT

Relatively few external components are required to implement a DLC POTS line circuit. As shown in *Figure 10*, a complete line circuit is implemented using TP3212 with an external protection network consisting of fuse resistors R_{TIP} and R_{RING}, and a voltage clamp device, two 360Ω ring sensing resistors, ring relay and two test relays. It should be noted that no supply decoupling capacitors are required for each line circuit from ±5V to ground, although the use of one larger electrolytic capacitor may be advisable for each power supply near the point at which it enters the line card.

Protection resistors R_{TIP} and R_{RING} should be nominally 100Ω with matching better than 1%. The selection of R_{TIP} and R_{RING} is important because they are fundamental to the ability of the line circuit to meet lightning and power cross requirements. R_{TIP} and R_{RING} should be designed such that they can withstand level one lightning and power cross requirement, while fusing open when overstressed by level two lightning and power cross. TPR and RPR are protected by the external voltage clamp device to limit the voltage at these two pins to within +2 to −85V. The ring sensing resistors, R_S, are 360Ω which sets the ring trip threshold to about 11 mAdc. The heavy relay current will be returned to GND3 at pin 26.

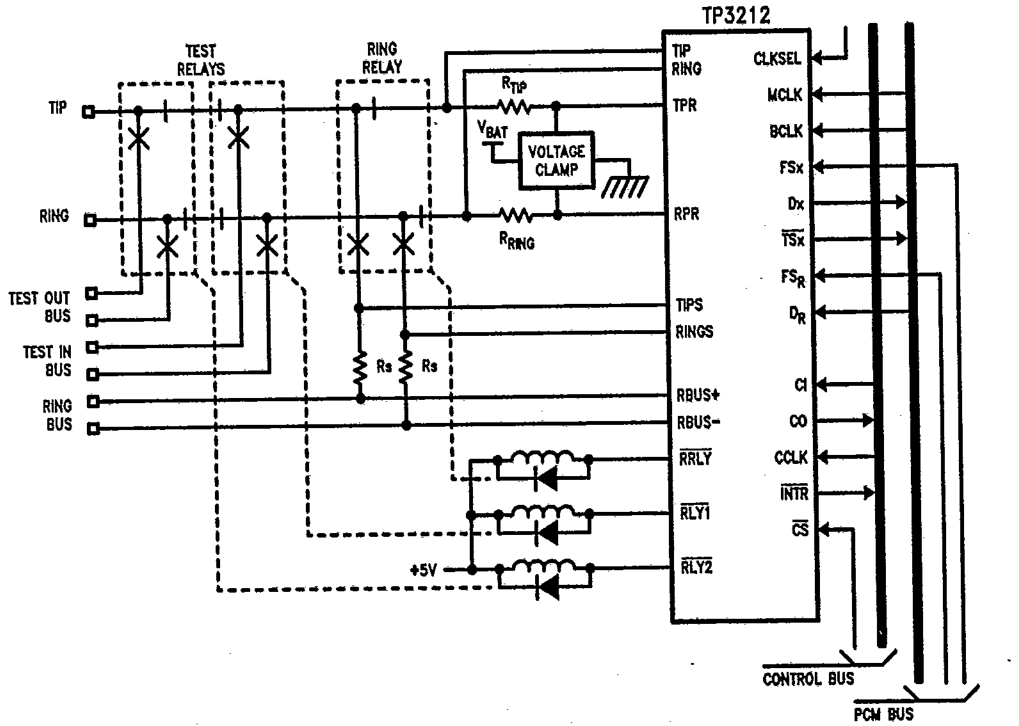
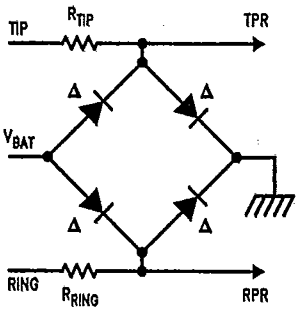


FIGURE 10. Complete DLC POTS Line Circuit Using TP3212

Applications Information (Continued)

SECONDARY PROTECTION

The high voltage protection network in *Figure 10* consists of resistors R_{TIP}, R_{RING} and a voltage limiting circuit which limits the voltage at TPR and RPR. A number of low cost possibilities for this voltage limit are shown in *Figure 11*. The lowest cost solution is a simple full wave rectifier diode bridge used to clamp the voltage to no more than one or two volts above RTN or below V_{BAT}, provided that the V_{BAT} supply is capable to absorb the power surges. The TIP and RING input terminals of the TP3212 is internally connected in series to two 300 kΩ thick film resistors, which are capable of withstanding power cross and surges.



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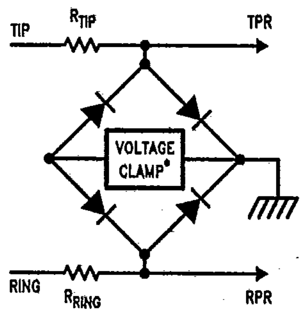
Δ20 Amp, 100V
20 Amp Surge



TL/H/10736-13

*SGS L5060
Thomson TPC68B

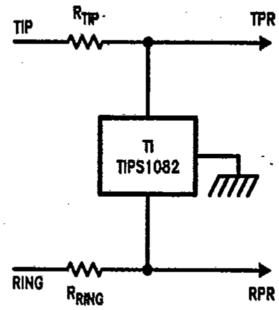


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FIGURE 11. Recommended Secondary Protection Networks

TYPICAL LINE CARD

A complete N-channel line card is illustrated in *Figure 12*. The backplane control interfaces vary greatly in different applications, and this example illustrates a possible arrangement.

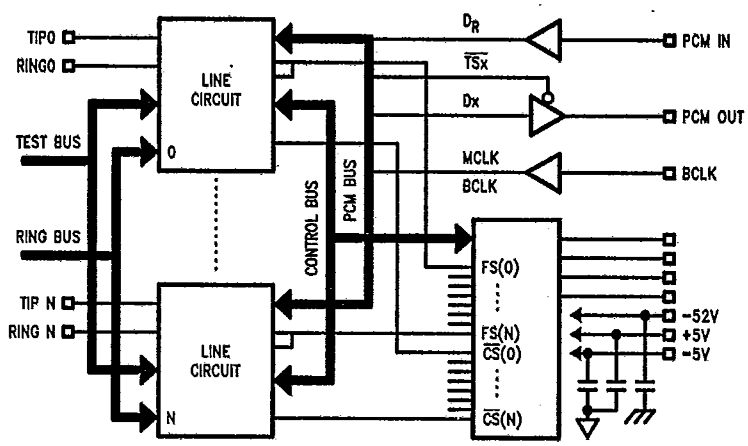

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FIGURE 12. Typical N-Channel Linecard