National Semiconductor

PRELIMINARY

TP5087/TP5092/TP5094/TP5380 DTMF (TOUCH-TONE®) Generators

General Description

These Tone Dialers are low threshold voltage, field-implanted, metal gate CMOS integrated circuits. The devices interface directly to a standard telephone keypad and generate all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A MUTE OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 2.5V-10V operation when generating tones (TP5380)
- 2V operation of keyscan and MUTE logic
- Powered directly from telephone line
- Interfaces with standard single-contact or 2-of-8 telephone keypad
- Static sensing of key closures
- On-chip 3.579545 MHz crystal-controlled oscillator
- On-chip regulation of tone amplitudes
- High group and low group tones generated and mixed internally
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$ pin

Block Diagram

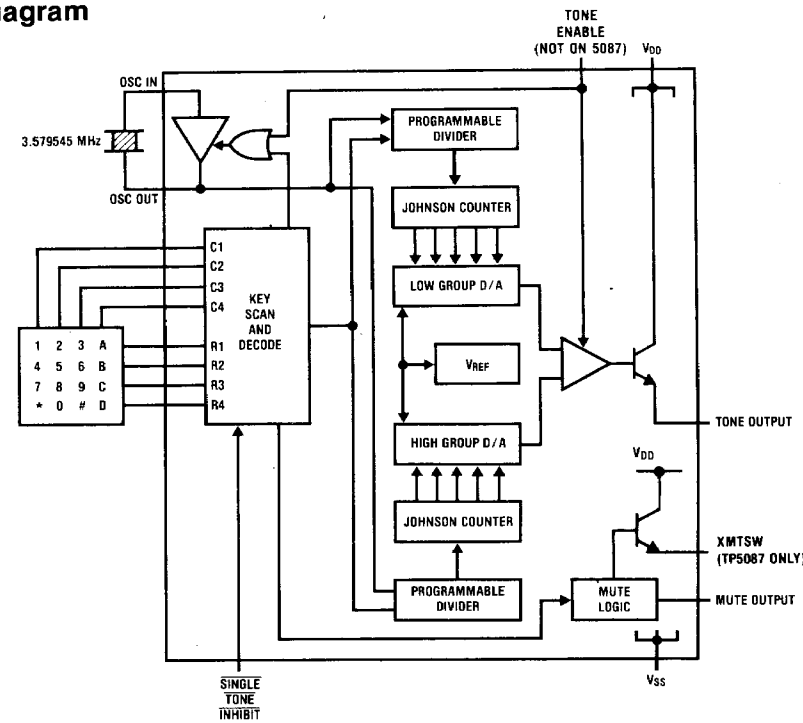

FIGURE 1. TP5087 Family

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Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	15V
Maximum Voltage at Any Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Operating Temperature	$-30°C$ to $+60°C$
Storage Temperature	$-55°C$ to $+150°C$
Maximum Power Dissipation	500 mW

Electrical Characteristics T_A within operating temperature range, $3.5V < V_{DD} < 10V$ unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
TP5087, TP5092, TP5094					
Minimum Supply Voltage Swing, $V_{DD\,(min)}$	Generating Tones			3.5	V
Output Amplitudes	$R_L = 240\Omega$				
Low Group TP5087, TP5094			400		mVrms
TP5092			450		mVrms
High Group TP5087, TP5094			540		mVrms
TP5092			620		mVrms
Mean Output DC Offset, V_{OS}	$V_D = 3.5V$		1.3		V
	$V_{DD} = 10V$		4.6		V
TP5380					
Minimum Supply Voltage Swing, $V_{DD\,(min)}$	Generating Tones			2.5	V
Output Amplitudes	$R_L = 100\Omega$				
Low Group			170		mVrms
High Group			230		mVrms
Mean Output DC Offset, V_{OS}	$V_{DD} = 2.5V$		0.7		V
	$V_{DD} = 10V$		2.5		V
ALL PARTS					
Minimum Supply Voltage for Keysense and MUTE Logic Functions				2	V
Operating Current					
Idle	R_L = open,		20		μA
Generating Tones	$V_{DD} = 3.5V$		2		mA
Input Pull-Up Resistors					
COLUMN and ROW (Pull-Down)			40		kΩ
SINGLE TONE INHIBIT			50		kΩ
TONE ENABLE			50		kΩ
MUTE OUT Sink Current (COLUMN and ROW Inactive)	$V_{DD} = 3V$, $V_o = 0.5V$	0.5			mA
MUTE OUT Source Current (COLUMN and ROW Active)	$V_{DD} = 3V$, $V_o = 2.5V$	0.5			mA
High Group Pre-Emphasis		2.4	2.7	3.0	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth	22			dB
Start-Up Time (to 90% Amplitude)	$V_{DD} \geq 4V$, $R_L \geq 150\Omega$		2	5	ms

Note 1: Crystal Specifications: Parallel Resonant, $R_S \leq 150\Omega$, $L = 100$ mH, $C_0 = 5$ pF, $C_1 = 0.02$ pF.

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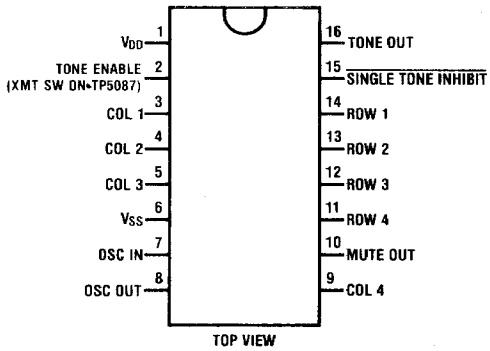
Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number TP5087N, TP5092N, TP5094N or TP5380N
See NS Package N16A

Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically to ensure no modulation of the line when tones are not being generated. A valid key closure activates the MUTE output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

Pin Descriptions

V_{DD} (Pin 1): The positive voltage supply to the device, referenced to V_{SS}. The collectors of the TONE OUT, and XMT SW transistors are also connected to this pin.

V_{SS} (Pin 6): This is the negative voltage supply.

OSCILLATOR (Pins 7 and 8): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when both COLUMN inputs and ROW inputs are sensed sequentially with no valid input having been detected. The oscillator is also stopped when the TONE ENABLE input is pulled to logic low.

ROW and COLUMN Inputs (Pins 3, 4, 5, 9, 11, 12, 13, 14): When no key is pushed, pull-up resistors are active on COLUMN inputs and pull-down resistors are active on ROW inputs. Column latches are ON and ready to store column key closures. After a key is pushed, the row pull-down resistors cause a negative-true on COLUMN inputs which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.

TONE ENABLE Input (Pin 2): The TONE ENABLE input h an internal pull-up resistor. When this input is open o logic high, the normal tone output mode will occur. Wh this input is at logic low, the device will be in the inact mode, tone output will be at an open circuit state.

XMT SW Output (Pin 2 of TP5087 only): With no key puts, this output is pulled high by the open emitter of NPN transistor. Any key entry turns off this transistor pulling its base to V_{SS}.

MUTE Output (Pin 10): The MUTE output is a conventio CMOS output that sinks current to V_{SS} with no valid in and sources current from V_{DD} when a valid key input sensed. The MUTE output will switch regardless of state of the SINGLE TONE INHIBIT input.

SINGLE TONE INHIBIT Input (Pin 15): The SINGLE TO INHIBIT input is used to inhibit the generation of oth than valid tone pairs due to multiple row-column closur It has a pull-up resistor to V_{DD}, and when left open or tied V_{DD}, single or dual tones may be generated in accordan with Table II. When forced to V_{SS}, any input situation th would normally result in a single tone will now result in tone, with all other chip functions operating normally.

TONE OUT (Pin 16): This output is the open emitter of NPN transistor, the collector of which is connected to V_{D} When an external load resistor is connected from TO OUT to V_{SS}, the output voltage on this pin is the sum of t high and low group sine-waves superimposed on a DC c set. When not generating tones, this output transistor turned OFF to minimize the device idle current.

Applications Information

Adjustment of the emitter load resistor results in variati of the mean DC current during tone generation, the si wave signal current through the output transistor, and t output distortion. Increasing values of load resistan decrease both the signal current and distortion, while creasing the source impedance of the device as seen fr its power supply terminals. Note that the DTMF generat is a current source which modulates its own supply t minals in a conventional telephone application.

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TABLE I. OUTPUT FREQUENCY ACCURACY

Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	−0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	−0.11
High Group f_H	C1	1209	1206.0	−0.24
	C2	1336	1331.7	−0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

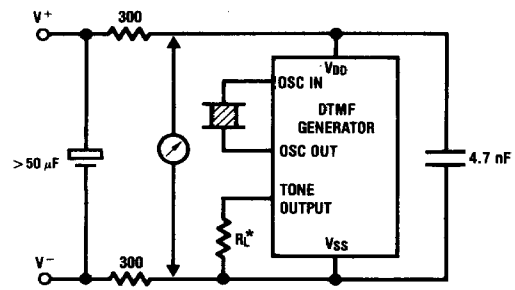
TABLE II. FUNCTIONAL TRUTH TABLE

SINGLE TONE INHIBIT	TONE ENABLE	ROW	COLUMN	Tones		MUTE
				Low	High	
X	O	X	X	0V	0V	0
X	X	O/C	O/C	0V	0V	0
X	1	One	One	f_L	f_H	1
1	1	2 or More	One	—	f_H	1
1	1	One	2 or More	f_L	—	1
1	1	2 or More	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	One	V_{OS}	V_{OS}	1
0	1	One	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	2 or More	V_{OS}	V_{OS}	1

Note 1: X is don't care state.

Note 2: V_{OS} is the output offset voltage.

Note 3: TONE ENABLE and $\overline{\text{SINGLE TONE INHIBIT}}$ have internal pull-up resistors.



* Adjust R_L for desired tone amplitudes.

FIGURE 2. Amplitude and Distortion Measurements for Conventional Telephone Applications

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