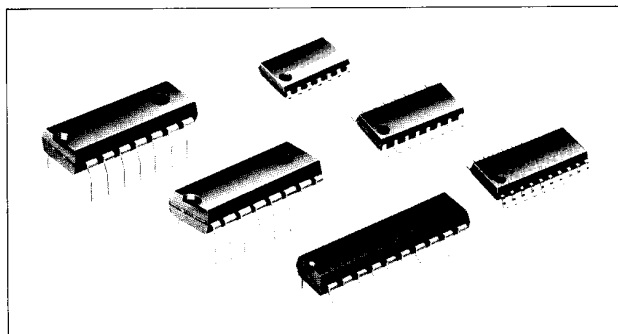




The BU74HC is a series of CMOS ICs characterized by low voltage and low power consumption. In addition to a wide supply voltage range, the BU74HC is compatible with the general-purpose 74HC series. Another feature of the series is that it can drive LS-TTL ICs directly. The BU74HC is available in standard DIP and MF (mini-flat) packages.

Features

1. Low power consumption.
2. Wide supply voltage range (2~6V).
3. High input impedance.
4. High fan-out.
5. Capable of directly driving LS-TTL10.
6. High speed.

BU74HC Series Product Summary

☆Under development

Category	Type	Function	Block diagram	Package	
				Configuration	No. of pins
Gates	BU74HC00	Quad 2-input NAND gate	Fig. 19	DIP/MF	14
	BU74HC02	Quad 2-input NOR gate	Fig. 20	DIP/MF	14
	BU74HC08	Quad 2-input AND gate	Fig. 21	DIP/MF	14
	☆BU74HC14	Hex Schmitt trigger	Fig. 22	DIP/MF	14
	BU74HC86	Quad 2-input exclusive OR Gate	Fig. 23	DIP/MF	14
	☆BU74HC132	Quad 2-input Schmitt trigger	Fig. 24	DIP/MF	14
	BU74HC266	Quad 2-input exclusive NOR gate	Fig. 25	DIP/MF	14
Latches	☆BU74HC373	Octal tristate noninverting D-type transparent latch	Fig. 26	DIP/MF	20
	☆BU74HC533	Octal tristate noninverting D-type transparent latch	Fig. 27	DIP/MF	20
Flip-flops	BU74HC73	Dual J-K flip-flop with reset	Fig. 28	DIP/MF	14
	BU74HC74	Dual D-type flip-flop with set & reset	Fig. 29	DIP/MF	14
	BU74HC76	Dual J-K flip-flop with set & reset	Fig. 30	DIP/MF	16
	☆BU74HC174	Hex D-type flip-flop with common clock & reset	Fig. 31	DIP/MF	16
	☆BU74HC374	Octal tristate noninverting D-type flip-flop	Fig. 32	DIP/MF	20
	☆BU74HC534	Octal tristate noninverting D-type flip-flop	Fig. 33	DIP/MF	20
Digital data selectors/multiplexers	☆BU74HC157	Quad 2-input data selector/multiplexer	Fig. 34	DIP/MF	16
	☆BU74HC158	Quad 2-input data selector/multiplexer with inverting output	Fig. 35	DIP/MF	16
Decoders	BU74HC138	1-OF-8 decoder/demultiplexer	Fig. 36	DIP/MF	16
	BU74HC139	Dual 1-OF-4 decoder/demultiplexer	Fig. 37	DIP/MF	16
Counters	BU74HC160	Presetable BCD counter	Fig. 38	DIP/MF	16
	BU74HC161	Presetable binary counter	Fig. 39	DIP/MF	16
	☆BU74HC162	Presetable BCD counter	Fig. 40	DIP/MF	16
	☆BU74HC163	Presetable binary counter	Fig. 41	DIP/MF	16
Buffers/inverters	BU74HC04	Hex unbuffered inverter	Fig. 42	DIP/MF	14
	☆BU74HC240	Octal tristate inverting buffer/line driver/line receiver	Fig. 43	DIP/MF	20
	☆BU74HC241	Octal tristate noninverting buffer/line driver/line receiver	Fig. 44	DIP/MF	20
	☆BU74HC244	Octal tristate noninverting buffer/line driver/line receiver	Fig. 45	DIP/MF	20
	☆BU74HC367	Hex noninverting buffer	Fig. 46	DIP/MF	16
	☆BU74HC368	Hex inverting buffer	Fig. 47	DIP/MF	16

CMOS Logic IC BU74HC Series

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V _{CC}	-0.5 ~ 7.0	V
Input voltage	V _{IN}	0.5 ~ V _{CC} + 0.5	V
Output voltage	V _{OUT}	-0.5 ~ V _{CC} + 0.5	V
Input current	I _{IN}	± 20	mA
Output current	I _{OUT}	± 25	mA
Circuit current	I _{CC}	± 50	mA
Power dissipation	P _d	500*	mW
Storage temperature	T _{stg}	-65 ~ 150	°C

*Derating is done at 5.0mW/°C for operation above Ta=25°C.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit	Conditions
Supply voltage	V _{CC}	2.0 ~ 6.0	V	—
Input, output voltage	V _{IN} , V _{OUT}	0 ~ V _{CC}	V	—
Operating temperature	T _{opr}	-40 ~ 85*	°C	—
Output rise time, fall time	t _r , t _f	~ 500	ns	—

*For an extended operating temperature range, consult your local ROHM representative.

Electrical Characteristics/DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
						V _{CC} (V)	V _{IN} (V)
Input high voltage	V _{IH}	1.5	1.2	—	V	2.0	—
		3.15	2.4	—		4.5	—
		4.2	3.2	—		6.0	—
Input low voltage	V _{IL}	—	0.6	0.3	V	2.0	—
		—	1.8	0.9		4.5	—
		—	2.4	1.2		6.0	—
Output high voltage	V _{OH}	1.9	1.998	—	V	2.0	V _{IH}
		4.4	4.499	—		4.5	or
		5.9	5.999	—		6.0	V _{IL}
Output low voltage	V _{OL}	—	0.002	0.1	V	2.0	V _{IH}
		—	0.001	0.1		4.5	or
		—	0.001	0.1		6.0	V _{IL}
Input current	I _{IN}	-0.1	0.00001	0.1	μA	6.0	V _{CC} or GND
Power consumption	I _{CC}	—	—	4	μA	6.0	V _{CC} or GND

Electrical Characteristics/Switching Characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{CC} (V)	Conditions
Max. clock frequency	f _{MAX}	5	11	—	MHz	2.0	50% DUTY CYCLE C _L = 50pF INPUT: tr = tf = 6ns
		27	54	—		4.5	
		32	64	—		6.0	
Low-to-high propagation delay time Clock → Q, $\bar{Q}$	t _{PLH}	—	88	175	ns	2.0	C _L = 50pF INPUT: tr = tf = 6ns
		—	18	35		4.5	
		—	15	30		6.0	
High-to-low propagation delay time Clock → Q, $\bar{Q}$	t _{PHL}	—	88	175	ns	2.0	C _L = 50pF INPUT: tr = tf = 6ns
		—	18	35		4.5	
		—	15	30		6.0	
Low-to-high propagation delay time SET, RESET → Q, $\bar{Q}$	t _{PLH}	—	115	230	ns	2.0	C _L = 50pF INPUT: tr = tf = 6ns
		—	23	46		4.5	
		—	20	39		6.0	
High-to-low propagation delay time SET, RESET → Q, $\bar{Q}$	t _{PHL}	—	115	230	ns	2.0	C _L = 50pF INPUT: tr = tf = 6ns
		—	23	46		4.5	
		—	20	39		6.0	
Output rise time Output fall time	t _{TLH} , t _{THL}	—	38	75	ns	2.0	OUTPUT: C _L = 50pF INPUT: tr = tf = 6ns
		—	8	15		4.5	
		—	6	13		6.0	
Maximum input capacitance	C _{IN}	—	5	10	pF	—	—

CMOS Logic IC BU74HC Series

Dimensions (Unit: mm)

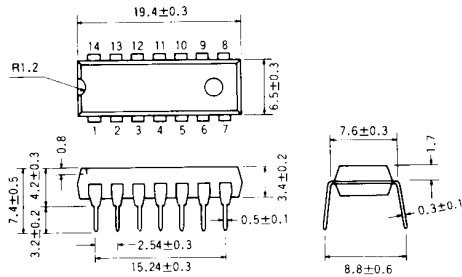


Fig. 1 14-pin DIP

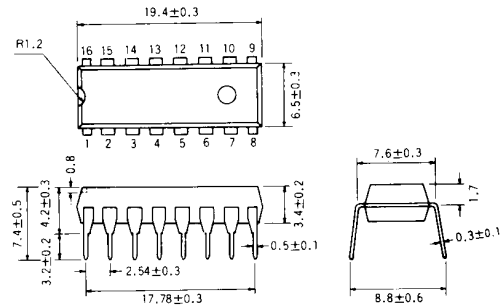


Fig. 2 16-pin DIP

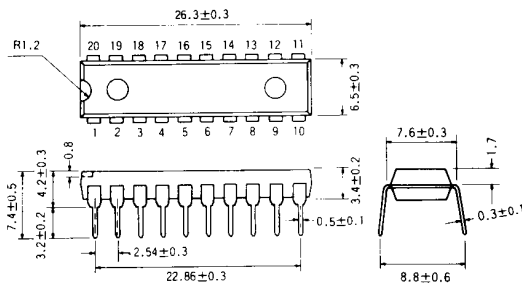


Fig. 3 20-pin DIP

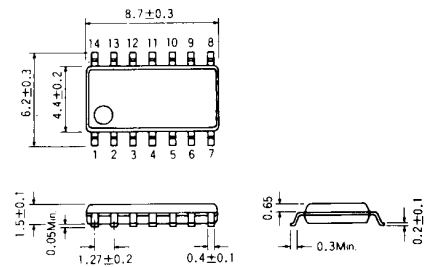


Fig. 4 14-pin MF

Dimensions (Unit: mm)

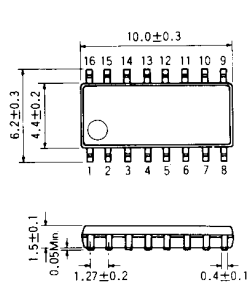


Fig. 5 16-pin MF

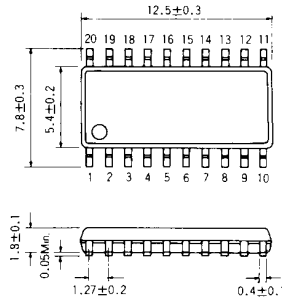


Fig. 6 20-pin MF

Electrical Characteristic Curves

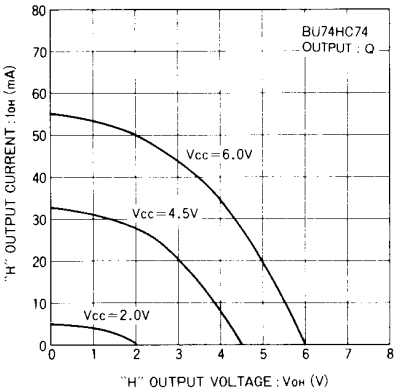


Fig. 7 Output high current vs. output high voltage

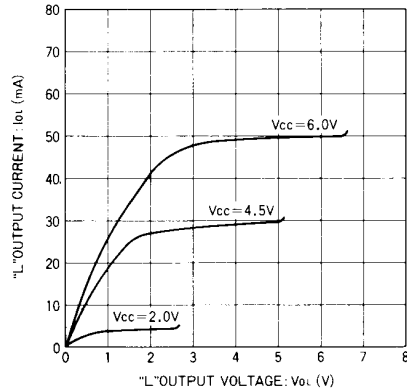


Fig. 8 Output low current vs. output low voltage

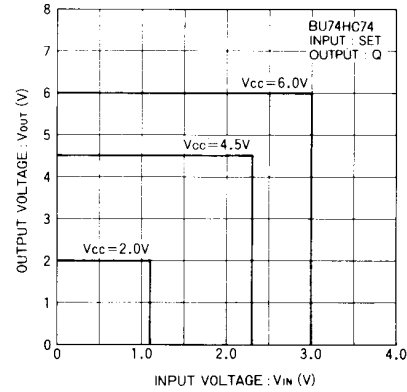


Fig. 9 Output voltage vs. input voltage

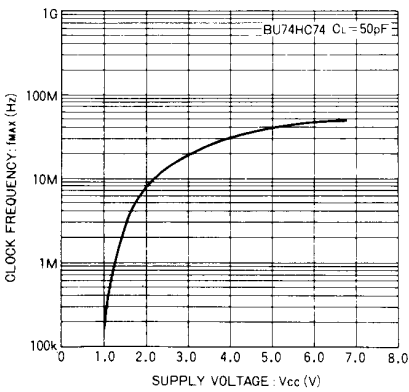


Fig. 10 Maximum clock frequency vs. supply voltage

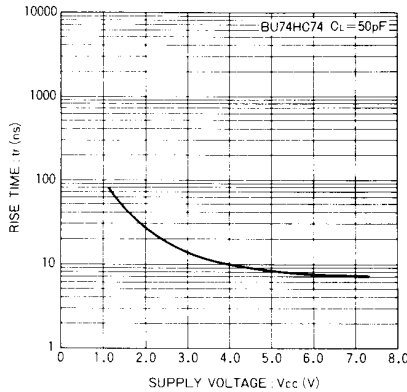


Fig. 11 Rise time vs. supply voltage

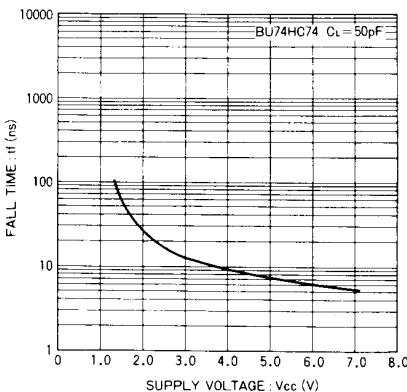


Fig. 12 Fall time vs. supply voltage

Electrical Characteristic Curves

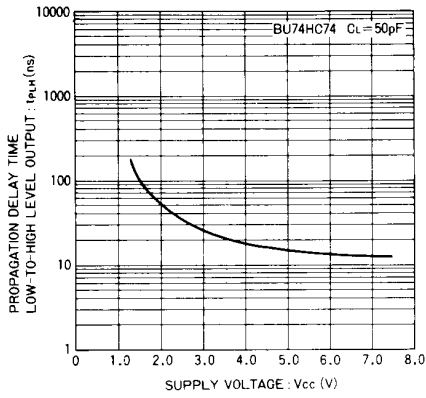


Fig. 13 Low-to-high propagation delay time vs. supply voltage

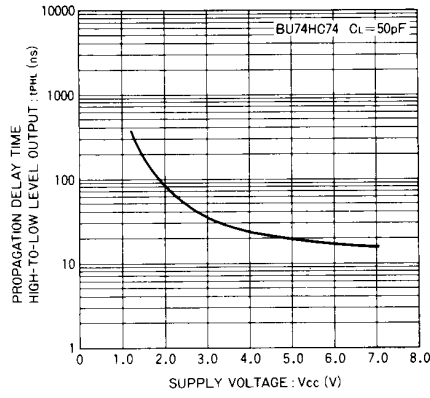


Fig. 14 High-to-low propagation delay time vs. supply voltage

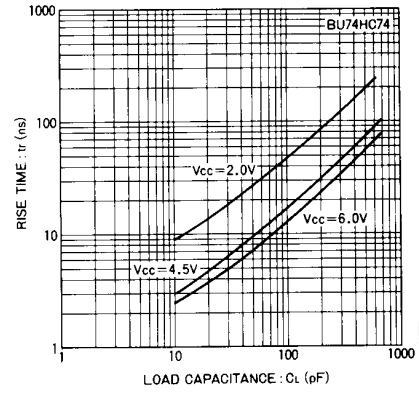


Fig. 15 Rise time vs. load capacitance

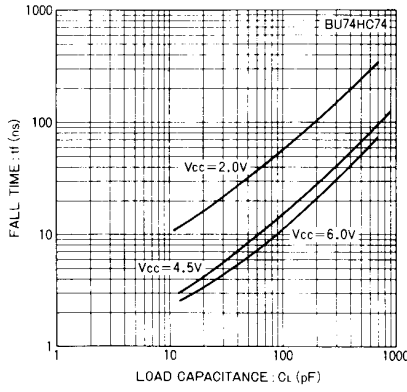


Fig. 16 Fall time vs. load capacitance

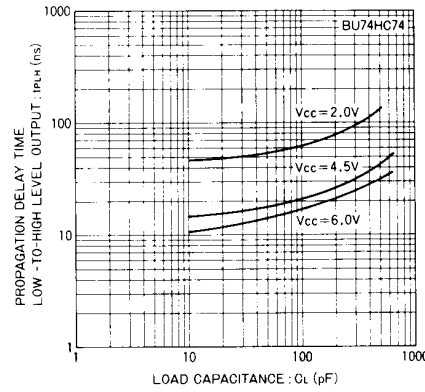


Fig. 17 Low-to-high propagation delay time vs. load capacitance

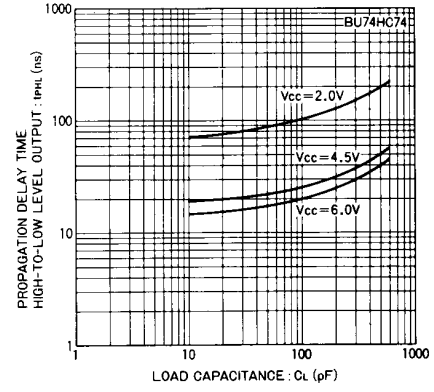


Fig. 18 High-to-low propagation delay time vs. load capacitance

CMOS Logic IC BU74HC Series

Block Diagrams

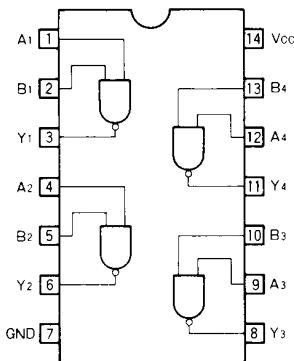


Fig. 19 BU74HC00

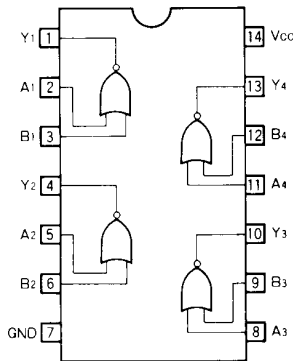


Fig. 20 BU74HC02

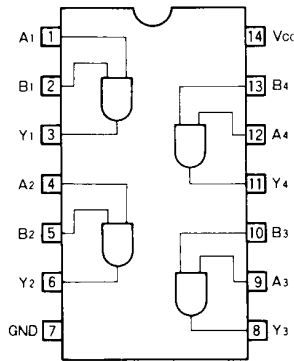


Fig. 21 BU74HC08

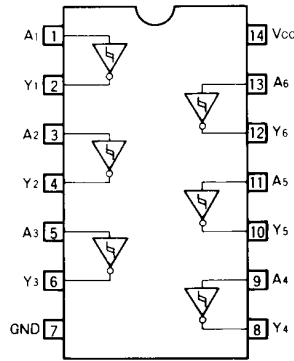


Fig. 22 BU74HC14

Block Diagrams

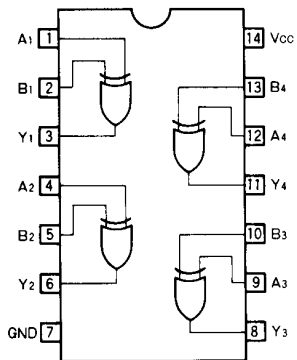


Fig. 23 BU74HC86

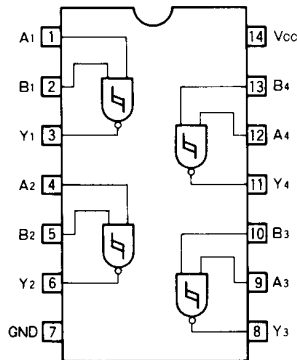


Fig. 24 BU74HC132

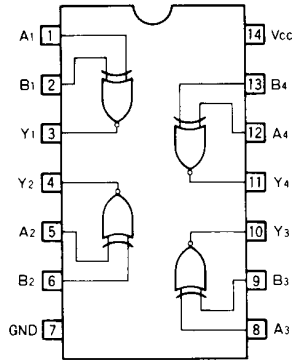


Fig. 25 BU74HC266

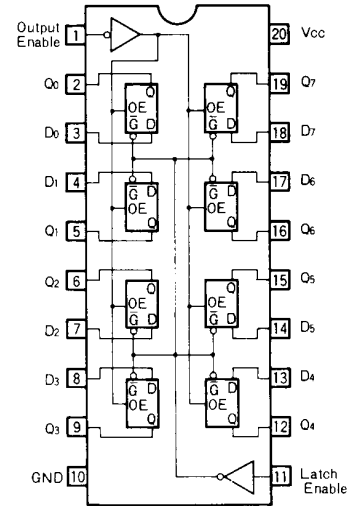


Fig. 26 BU74HC373

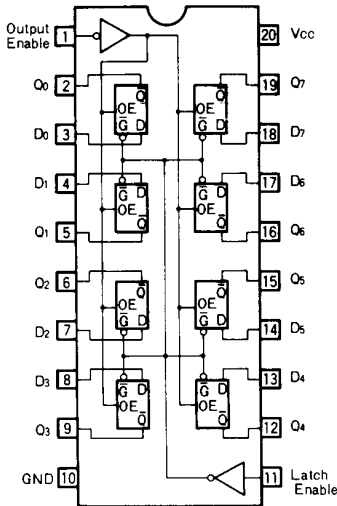


Fig. 27 BU74HC533

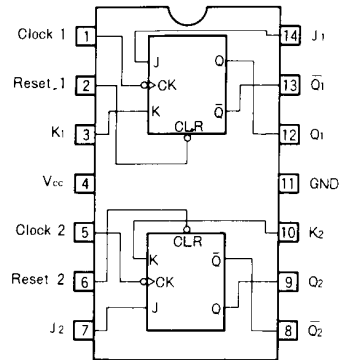


Fig. 28 BU74HC73

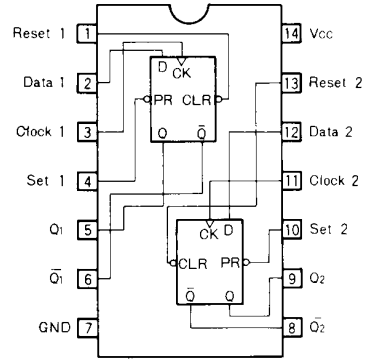


Fig. 29 BU74HC74

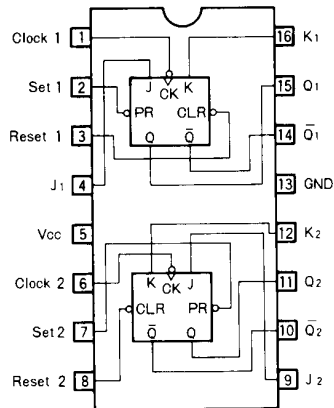


Fig. 30 BU74HC76

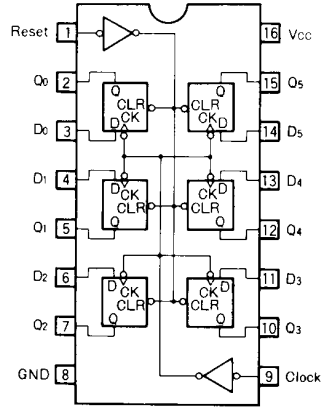


Fig. 31 BU74HC174

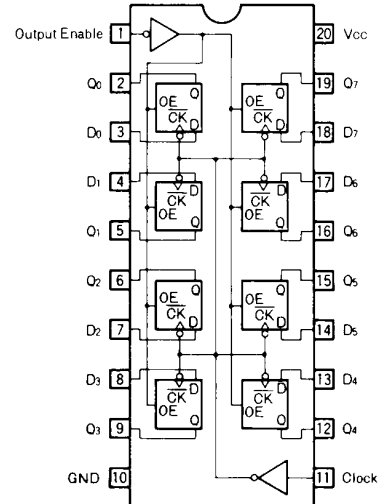


Fig. 32 BU74HC374

Block Diagrams

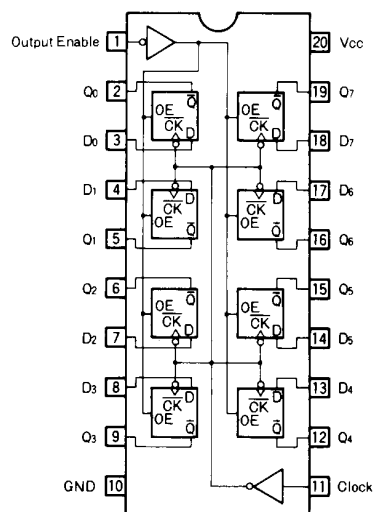


Fig. 33 BU74HC534

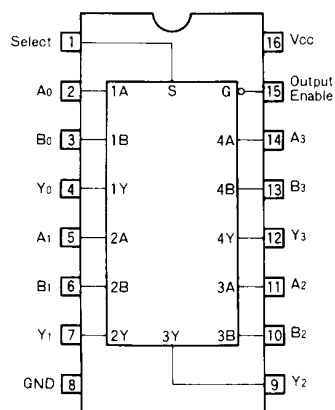


Fig. 34 BU74HC157

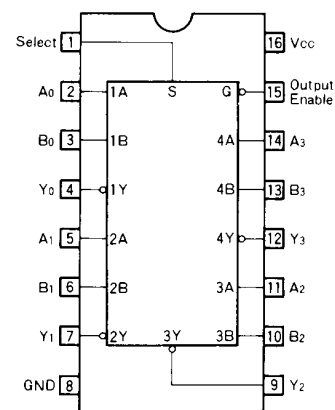


Fig. 35 BU74HC158

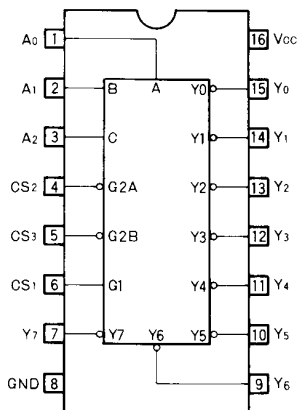


Fig. 36 BU74HC138

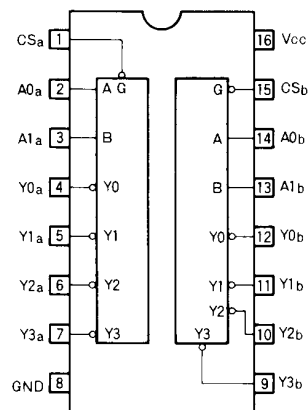


Fig. 37 BU74HC139

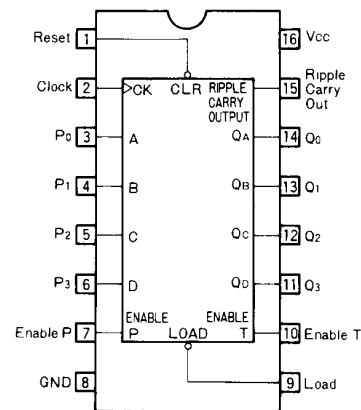


Fig. 38 BU74HC160

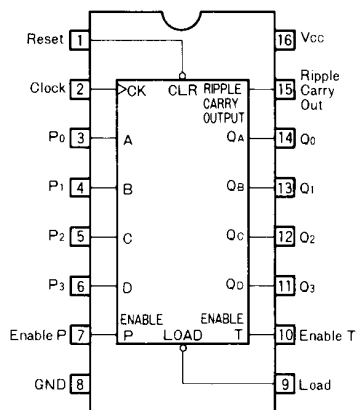


Fig. 39 BU74HC161

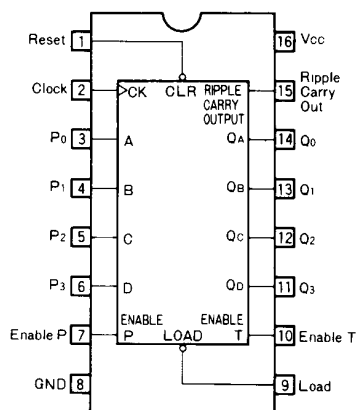


Fig. 40 BU74HC162

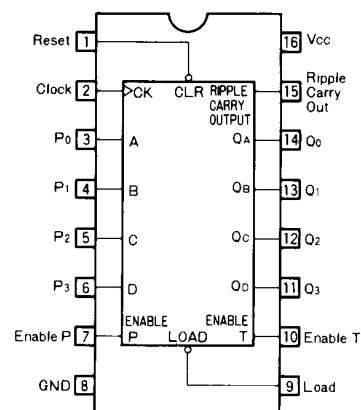


Fig. 41 BU74HC163

Block Diagrams

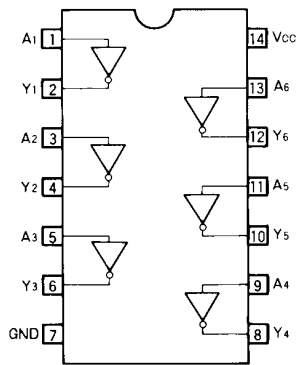


Fig. 42 BU74HCU04

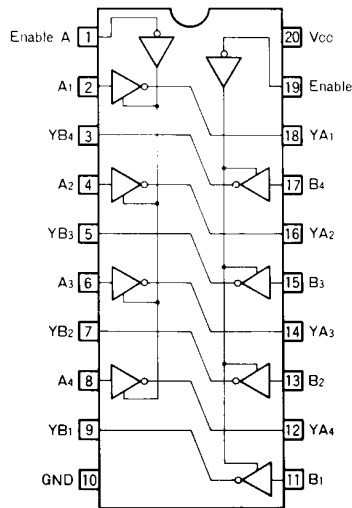


Fig. 43 BU74HC240

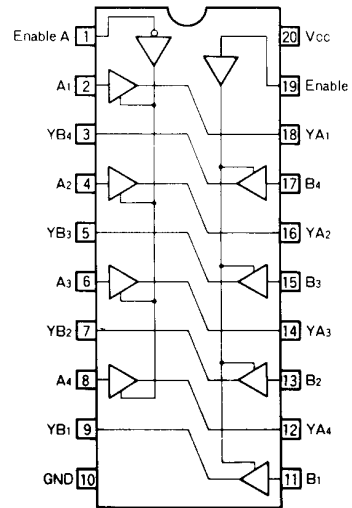


Fig. 44 BU74HC241

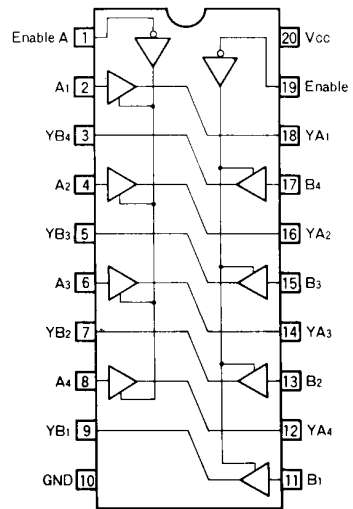


Fig. 45 BU74HC244

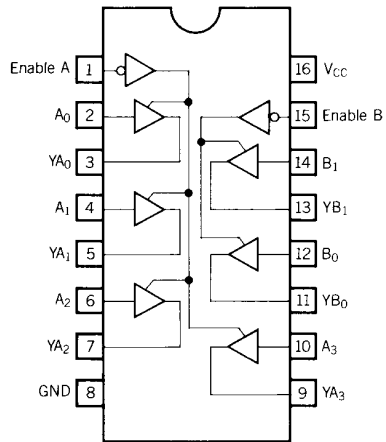


Fig. 46 BU74HC367

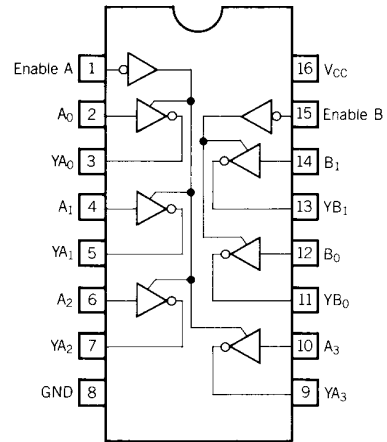


Fig. 47 BU74HC368

Waveforms

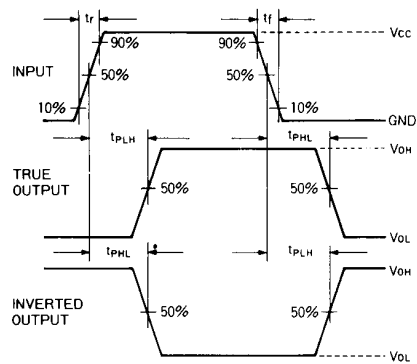


Fig. 48 Propagation delay time

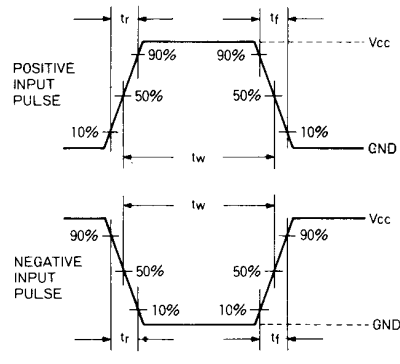


Fig. 49 Input pulse width

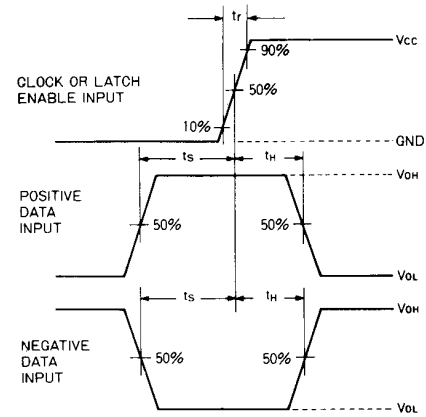


Fig. 50 Set-up time, hold time

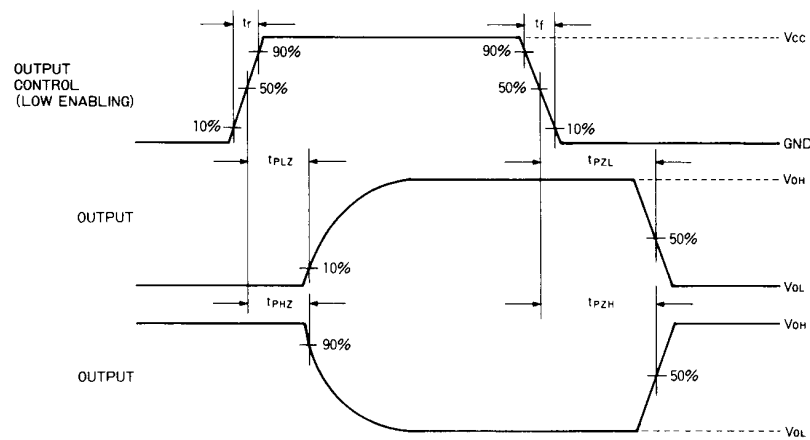


Fig. 51 Tristate output enable waveform, disable waveform

CMOS Logic IC BU74HC Series