# Servo signal processor for CD use
# BU9321BKS

The BU9321BKS is a servo signal processor for CD players that incorporates a double-speed, no-adjustment PLL, program servo, and signal processing block on one chip. It operates off a low power supply voltage, and has low power consumption.

●Applications

Portable CD players, radio cassette players, and mini-component systems.

●Features

1) PLL on chip. Bit clock extraction possible with just a few external components. EFM data modulation is possible.
2) Frame synchronizing signal detection and protection.
3) Servo filters for focus, tracking, and sled are on chip. Characteristics can be controlled using commands from the controller.
4) Sub-code serial output pin provided.
5) Output pins for both P-code and Q-code.
6) CLV sequencer automatically determines the CLV mode.
7) Track jump sequencer on chip. Possible to jump any number of tracks.
8) De-interleave function, and 2-level error detection, correction and flag processing for C1 and C2.
9) The signal to the DAC is output by the MSB first 2'SCOMP serial out, and offset circuit ON and OFF can be controlled for CD-ROM compatibility.
10) 16 kilobits of on-chip SRAM absorb ±4 frames of jitter.
11) Double-speed playback is possible.

●Absolute maximum ratings (Ta = 25°C)

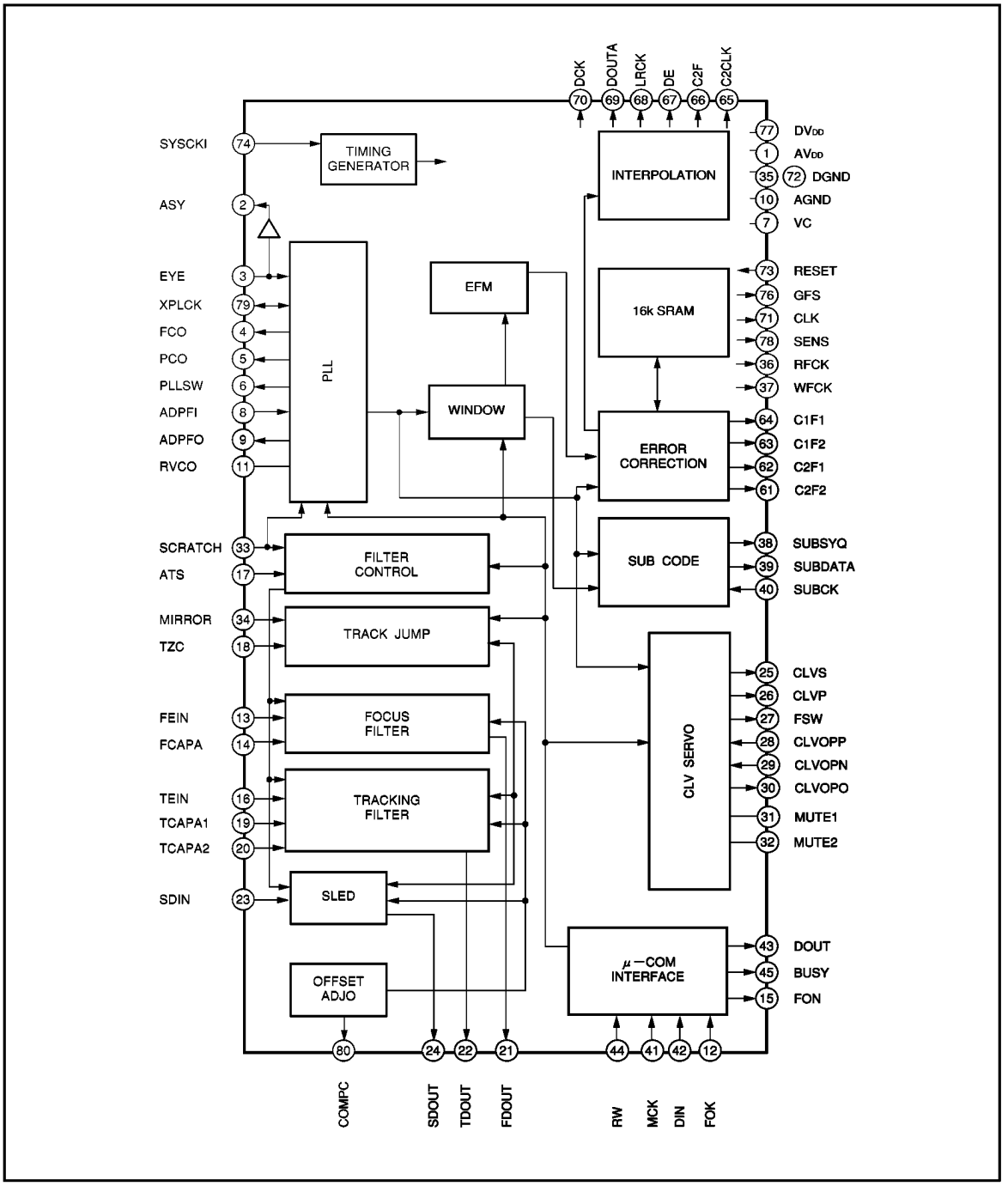
| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | 4.5 | V |
| Power dissipation | Pd | 400 * | mW |
| Operating temperature | Topr | −25~+75 | ℃ |
| Storage temperature | Tstg | −55~+125 | ℃ |

* Reduced by 4mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | 2.6 | — | 3.5 | V |

●Block diagram

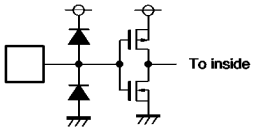
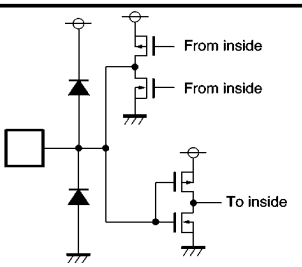
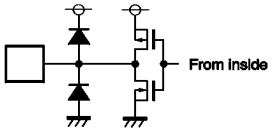
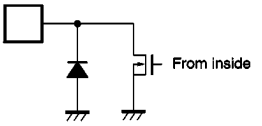
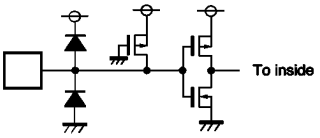
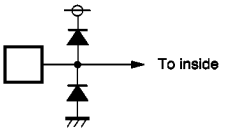
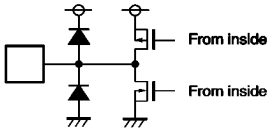
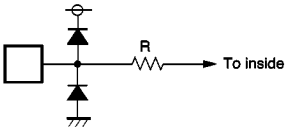


●Pin descriptions

| Pin No. | Pin name | Analog/digital | I / O | Function | I/O circuit |
|---|---|---|---|---|---|
| 1 | $AV_{DD}$ | — | — | Analog power supply | — |
| 2 | ASY | Digital | O | EFM signal slice level control output | 4 |
| 3 | EYE | Digital | I | EFM signal input pin from the RF amplifier | 1 |
| 4 | FCO | Analog | O | PLL frequency comparator output (R=15Ω) | 8 |
| 5 | PCO | Analog | O | PLL phase comparison error voltage output (R=5Ω) | 8 |
| 6 | PLLSW | Analog | O | PLL time constant switch pin | 6 |
| 7 | VC | Analog | I | Bias voltage input | 7 |
| 8 | ADPFI | Analog | I | PLL addition amplifier inversion signal | 7 |
| 9 | ADPFO | Analog | O | PLL addition amplifier output | 7 |
| 10 | AGND | — | I | Analog ground | — |
| 11 | RVCO | Analog | I | PLL VCO oscillator frequency adjustment | 7 |
| 12 | FOK | Digital | I | Focus OK signal input | 1 |
| 13 | FEIN | Analog | I | Focus error signal input | 7 |
| 14 | FCAPA | Analog | O | For connection of capacitor for focus servo filter | 7 |
| 15 | FON | Digital | O | Focus on signal output | 2 |
| 16 | TEIN | Analog | I | Tracking error signal input | 7 |
| 17 | ATS | Analog | I | Anti-shock detector window comparator input | 7 |
| 18 | TZC | Analog | I | Tracking/zero cross comparator input | 7 |
| 19 | TCAPA1 | Analog | O | For connection of switch 1 for tracking servo filter | 7 |
| 20 | TCAPA2 | Analog | O | For connection of switch 2 for tracking servo filter | 7 |
| 21 | FDOUT | Analog | O | Focus drive output | 7 |
| 22 | TDOUT | Analog | O | Tracking drive output | 7 |
| 23 | SDIN | Analog | I | Sled amplifier input | 7 |
| 24 | SDOUT | Analog | O | Sled drive output | 7 |
| 25 | CLVS | Analog | O | CLV speed control output | 7 |
| 26 | CLVP | Analog | O | CLV phase control output | 7 |
| 27 | FSW | Analog | O | CLV filter time constant switch | 6 |
| 28 | CLVOPP | Analog | I | CLV addition amplifier non-inverted input | 7 |
| 29 | CLVOPN | Analog | I | CLV addition amplifier inverted input | 7 |
| 30 | CLVOPO | Analog | O | CLV addition amplifier output | 7 |
| 31 | MUTE1 | Analog | I / O | CLV mute switch 1 | 7 |
| 32 | MUTE2 | Analog | I / O | CLV mute switch 2 | 7 |
| 33 | SCRATCH | Digital | I | Scratch signal input | 1 |
| 34 | MIRROR | Digital | I | Mirror signal input | 1 |
| 35 | DGND | — | — | Digital ground | — |
| 36 | RFCK | Digital | O | Read frame clock output | 2 |
| 37 | WFCK | Digital | O | Write frame clock output | 2 |
| 38 | SUBSYQ | Digital | O | Sub-code sync signal S1 output | 2 |
| 39 | SUBDATA | Digital | O | Sub-code serial output | 2 |
| 40 | SUBCK | Digital | I | Clock input for sub-code read | 1 |

| Pin No. | Pin name | Analog/digital | I / O | Function | I/O circuit |
|---|---|---|---|---|---|
| 41 | MCK | Digital | I | Clock input for command read and sub-code read | 1 |
| 42 | DIN | Digital | I | Command serial input from microprocessor | 1 |
| 43 | DOUT | Digital | O | Sub-Q code serial output | 4 |
| 44 | RW | Digital | O | Read/write switch input | 1 |
| 45 | BUSY | Digital | O | Busy output ("L" during track jump) | 2 |
| 46 | N.C. | — | — | — | — |
| 47 | N.C. | — | — | — | — |
| 48 | N.C. | — | — | — | — |
| 49 | N.C. | — | — | — | — |
| 50 | N.C. | — | — | — | — |
| 51 | N.C. | — | — | — | — |
| 52 | N.C. | — | — | — | — |
| 53 | N.C. | — | — | — | — |
| 54 | N.C. | — | — | — | — |
| 55 | N.C. | — | — | — | — |
| 56 | N.C. | — | — | — | — |
| 57 | N.C. | — | — | — | — |
| 58 | N.C. | — | — | — | — |
| 59 | N.C. | — | — | — | — |
| 60 | N.C. | — | — | — | — |
| 61 | C2F2 | Digital | O | C22 correction flag output | 2 |
| 62 | C2F1 | Digital | O | C21 correction flag output | 2 |
| 63 | C1F2 | Digital | O | C12 correction flag output | 2 |
| 64 | C1F1 | Digital | O | C11 correction flag output | 2 |
| 65 | C2CLK | Digital | O | Strobe signal (f=176.4kHz) | 2 |
| 66 | C2F | Digital | O | Correction status output | 2 |
| 67 | DE | Digital | O | Strobe signal (f=88.2kHz) | 2 |
| 68 | LRCK | Digital | O | Strobe signal (f=44.1kHz) | 2 |
| 69 | DOUTA | Digital | O | Audio data output (2'SCOMP) | 2 |
| 70 | DOCK | Digital | O | Bit clock for DOUT (f=2.1168MHz) | 2 |
| 71 | CLK | Digital | O | Clock output (select from four types using &hE4 command) | 2 |
| 72 | DGND2 | — | — | Digital ground | — |
| 73 | RESET | Digital | I | Internal circuit reset | 3 |
| 74 | SYSCKI | Digital | I | System clock input (f=16.93MHz) | 1 |
| 75 | N.C. | — | — | — | — |
| 76 | GFS | Digital | O | GFS monitor output (select from four types using &hE4 command) | 2 |
| 77 | $DV_{DD}$ | — | — | Digital power supply | — |
| 78 | SENS | Digital | O | Monitor output pin (&hE4 command setting or offset comparator output) | 2 |
| 79 | XPLCK | Digital | I / O | PLL playback clock output or external PLL playback clock input | 5 |
| 80 | COMPC | Analog | O | Offset adjustment smoothing (analog offset measurement is possible) | 7 |

●Input / output circuits

| | | | |
|---|---|---|---|
| 1 |  | 5 |  |
| 2 |  | 6 |  |
| 3 |  | 7 |  |
| 4 |  | 8 |  |

Pin types

* 1 CMOS inputs.
  EYE (3pin), FOK (12pin), **SCRATCH (33pin), MIRROR (34pin), SUBCK (40pin), MCK (41pin), DIN (42pin)**, RW (44pin), SYSCKI (74pin)
* 2 Inputs with pullups.
  RESET (73pin)
* 3 CMOS outputs.
  FON (15pin), RFCK (36pin**), WFCK (37pin), SUBSYQ (38pin), SUBDATA (39pin), BUSY (45pin),** C2F2 (61pin), C2F1 (62pin), C1F2 (63pin), C1F1 (64pin), C2CLK (65pin**), C2F (66pin), DE (67pin), LRCK (68pin), DOUTA (69pin), DOCK (70pin),** CLK (71pin), GFS (76pin), SENS (78pin), XPLCK (79pin)
* 4 Tri-state outputs.
  ASY (2pin), DOUT (43pin)
* 5 Open drain.
  PLLSW (6pin), FSW (27pin)

●Electrical characteristics (digital system)

DC characteristics (unless otherwise noted, Ta = 25°C and $V_{DD}$ = 2.6V)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Conditions | Applicable pin |
|---|---|---|---|---|---|---|---|---|
| Input voltage | High level voltage | $V_{IH}$ | 1.9 | — | — | V | $I_O$=1mA | ∗1, 2 |
| | Low level voltage | $V_{IL}$ | — | — | 0.5 | V | $I_O$=−1mA | ∗1, 2 |
| Reset pin input current | | $I_{IH}$ | 15 | 40 | 100 | μA | $V_{IN}$=0V | ∗2 |
| Input current | | $I_{LI}$ | — | — | ±5 | μA | $V_{IN}$=0~2.6V | ∗1 |
| Output voltage | High level voltage | $V_{OH}$ | 2.2 | — | — | V | — | ∗3, 4 |
| | Low level voltage | $V_{OL}$ | — | — | 0.5 | V | — | ∗3, 4, 5 |
| Tri-state output leak current | | $I_{OZH}$ | — | — | ±5 | μV | $V_O$=0~2.6V | ∗4, 5 |

●Electrical characteristics (analog system)
(unless otherwise noted, Ta = 25°C, $V_{DD}$ = 2.6V, $R_L$ = 10kΩ and $V_C$ reference)

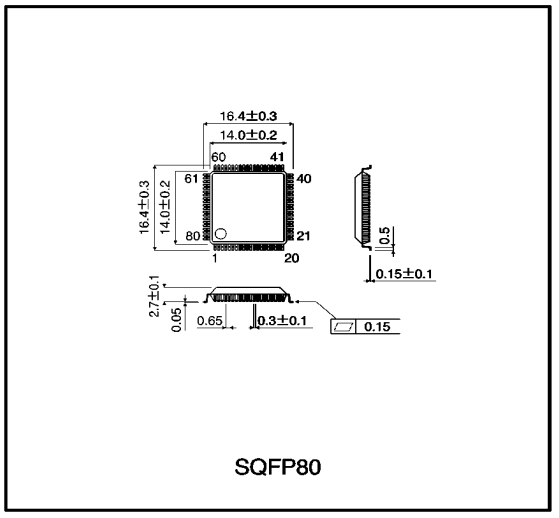
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions | Setting command |
|---|---|---|---|---|---|---|---|
| Quiescent current | $I_Q$ | 3.0 | 6.5 | 10 | mA | — | — |
| 〈Focus servo〉 | | | | | | | |
| DC voltage gain | $G_{FD1}$ | 23 | 26 | 29 | dB | IN=1Hz, 20m$V_{P-P}$ | 10×F, 1462 |
| AC voltage gain 1 | $G_{FDF1}$ | 3 | 6 | 9 | dB | IN=1kHz, 100m$V_{P-P}$ | 10×F, 1462 |
| AC voltage gain 2 | $G_{FDF2}$ | −4 | −1 | 2 | dB | IN=300Hz, 100m$V_{P-P}$ | 10×F, 1462 |
| Maximum output voltage | $V_{FD1}$ | 1.0 | — | — | V | — | — |
| Minimum output voltage | $V_{FD2}$ | — | — | −1.0 | V | — | — |
| Offset voltage | $V_{FOF}$ | −600 | — | 600 | mV | — | 10×F, 1462 |
| 〈Tracking servo〉 | | | | | | | |
| DC voltage gain | $G_{TD1}$ | 22 | 25 | 28 | dB | IN=1Hz, 20m$V_{P-P}$ | 10D×, 1159, 1207 |
| AC voltage gain 1 | $G_{TDF1}$ | 4 | 7 | 10 | dB | IN=1kHz, 100m$V_{P-P}$ | 10D×, 1159, 1207 |
| AC voltage gain 2 | $G_{TDF2}$ | −3 | 0 | 3 | dB | IN=300Hz, 100m$V_{P-P}$ | 10D×, 1159, 1207 |
| AC voltage gain 3 | $G_{TDF3}$ | 25 | 28 | 31 | dB | IN=1kHz, 20m$V_{P-P}$ *1 | 10D×, 1159, 1207 |
| AC voltage gain 4 | $G_{TDF4}$ | 20 | 23 | 26 | dB | IN=300Hz, 20m$V_{P-P}$ *1 | 10D×, 1159, 1207 |
| Maximum output voltage | $V_{TD1}$ | 1.0 | — | — | V | — | — |
| Minimum output voltage | $V_{TD2}$ | — | — | −1.0 | V | — | — |
| Offset voltage | $V_{TOF}$ | −530 | — | 530 | mV | — | 10D×, 1159, 1207 |
| Jump output voltage | $V_{JP1}$ | 1.0 | 1.2 | — | V | — | 13×F |
| Jump output voltage | $V_{JP2}$ | — | −1.2 | −1.0 | V | — | 13F× |
| ATS threshold voltage 1 | $V_{ATS1}$ | 10 | — | 50 | mV | — | — |
| ATS threshold voltage 2 | $V_{ATS2}$ | −50 | — | −10 | mV | — | — |
| TZC threshold voltage | $V_{TZC}$ | −50 | — | 50 | mV | — | — |
| ON resistance between TCAPA1 and TCAPA2 | $R_{TON}$ | — | 50 | 150 | Ω | I=0.1mA | 1E×1 |
| 〈Sled servo〉 | | | | | | | |
| DC voltage gain | $G_{SD1}$ | 23 | 26 | 29 | dB | IN=100Hz, 20m$V_{P-P}$ | 124× |
| Maximum output voltage | $V_{SD1}$ | 1.0 | — | — | V | — | — |
| Minimum output voltage | $V_{SD2}$ | — | — | −1.0 | V | — | — |
| Offset voltage | $V_{SOF}$ | −200 | 0 | 200 | mV | — | 124× |
| Kick output voltage 1 | $V_{KC1}$ | 1.0 | 1.2 | — | V | — | 18×F |
| Kick output voltage 2 | $V_{KC2}$ | — | −1.2 | −1.0 | V | — | 18F× |

*1 AC gain for gain amplifier (100kΩ between TCAPA1 and TCAPA2).
◎Not designed for radiation resistance.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions | Setting command |
|---|---|---|---|---|---|---|---|
| 〈CLV amplifier〉 | | | | | | | |
| Maximum output voltage | $V_{OPD1}$ | 1.0 | — | — | V | — | — |
| Minimum output voltage | $V_{OPD2}$ | — | — | 1.0 | V | — | — |
| Input offset voltage | $V_{OPOF}$ | −15 | 0 | 15 | mV | — | — |
| 〈CLV mute switch〉 | | | | | | | |
| ON resistance | $R_{ON}$ | — | 260 | 800 | Ω | I=1mA | E0 |
| 〈Offset adjustment block〉 | | | | | | | |
| Offset variable range 1 | $\Delta V_{OF1}$ | ±620 | ±710 | — | mV | Focus, tracking | |
| Offset variable range 2 | $\Delta V_{OF2}$ | ±300 | ±390 | — | mV | Sled | 124× |
| 〈PLL block〉 | | | | | | | |
| VCO oscillator frequency | $f_{VCO}$ | 13 | — | 21 | MHz | — | — |

*1 AC gain for gain amplifier (100kΩ between TCAPA1 and TCAPA2).
◎Not designed for radiation resistance.

●External dimensions (Units: mm)




SQFP80