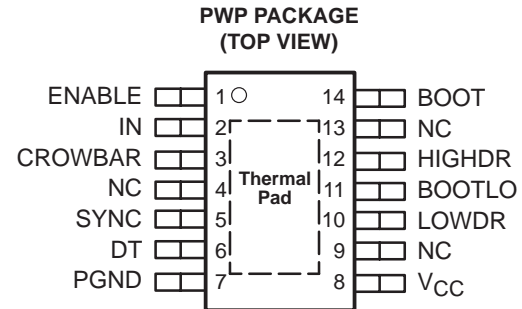
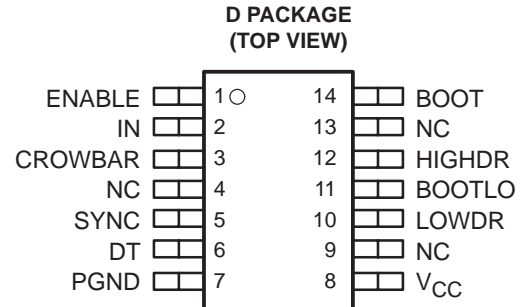


TPS2834, TPS2835 SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DEAD-TIME CONTROL

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- Floating Bootstrap or Ground-Reference High-Side Driver
- Adaptive Dead-Time Control
- 50-ns Max Rise/Fall Times With 3.3-nF Load
- 2.4-A Typical Output Current
- 4.5-V to 15-V Supply Voltage Range
- TTL-Compatible Inputs
- Internal Schottky Bootstrap Diode
- SYNC Control for Synchronous or Nonsynchronous Operation
- CROWBAR for OVP, Protects Against Faulted High-Side Power FETs
- Low Supply Current....3 mA Typical
- Ideal for High-Current Single or Multiphase Power Supplies
- –40°C to 125°C Operating Virtual Junction Temperature Range
- Available in SOIC and TSSOP PowerPAD Packages



NC – No internal connection

description

The TPS2834 and TPS2835 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using switching controllers that do not include on-chip MOSFET drivers. The drivers are designed to deliver minimum 2-A peak currents into large capacitive loads. The high-side driver can be configured as ground-reference or as floating-bootstrap. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions, and provides high efficiency for the buck regulator. The TPS2834 and TPS2835 have additional control functions: ENABLE, SYNC, and CROWBAR. Both high-side and low-side drivers are off when ENABLE is low. The driver is configured as a nonsynchronous-buck driver disabling the low-side driver when SYNC is low. The CROWBAR function turns on the low-side power FET, overriding the IN signal, for overvoltage protection against faulted high-side power FETs.

The TPS2834 has a noninverting input, while the TPS2835 has an inverting input. These drivers are available in 14-terminal SOIC and thermally enhanced TSSOP PowerPAD™ packages and operate over a junction temperature range of –40°C to 125°C.

Related Synchronous MOSFET Drivers

| DEVICE NAME | ADDITIONAL FEATURES | INPUTS | |
|-------------|-------------------------------|--------|-------------|
| TPS2830 | ENABLE, SYNC, and CROWBAR | CMOS | Noninverted |
| TPS2831 | | | Inverted |
| TPS2832 | W/O ENABLE, SYNC, and CROWBAR | CMOS | Noninverted |
| TPS2833 | | | Inverted |
| TPS2836 | W/O ENABLE, SYNC, and CROWBAR | TTL | Noninverted |
| TPS2837 | | | Inverted |



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PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TPS2834, TPS2835

SYNCHRONOUS-BUCK MOSFET DRIVERS

WITH DEAD-TIME CONTROL

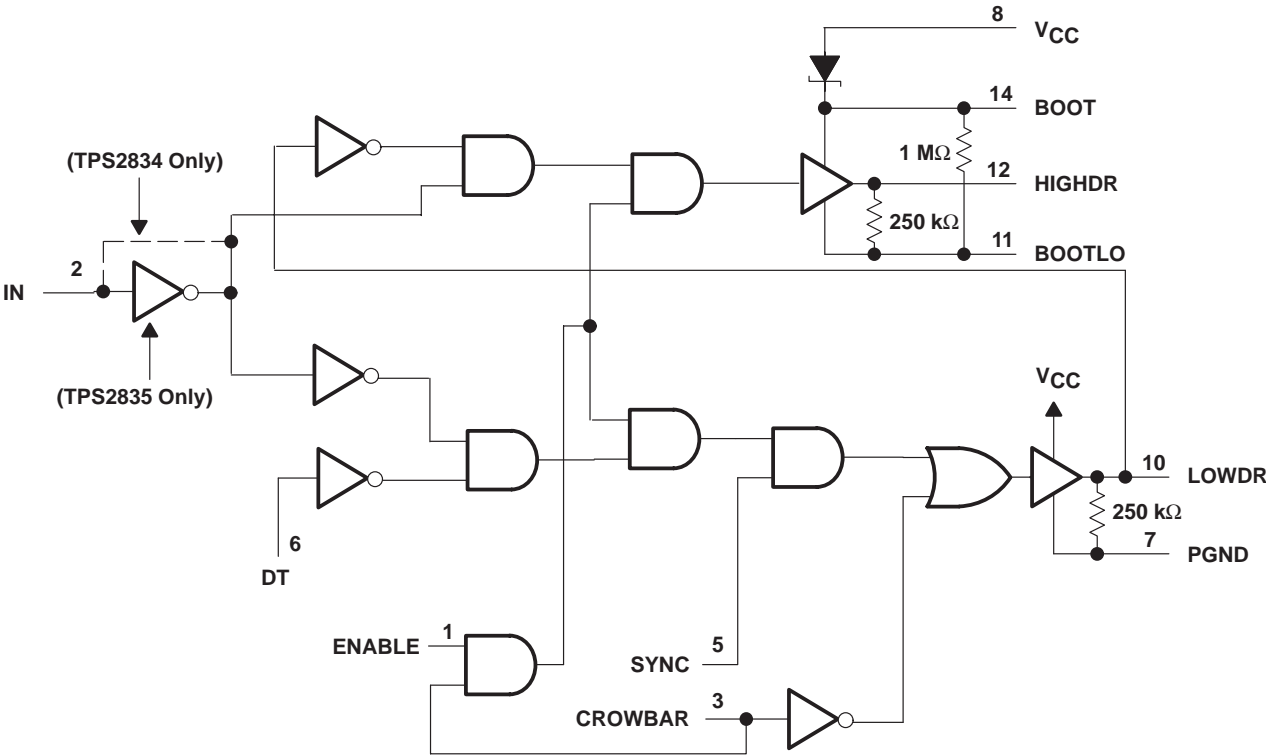
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AVAILABLE OPTIONS

| T _J | PACKAGED DEVICES | |
|-----------------|----------------------|--------------------------|
| | SOIC (D) | TSSOP (PWP) |
| – 40°C to 125°C | TPS2834D TPS2835D | TPS2834PWP TPS2835PWP |

The D and PWP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2834DR)

functional block diagram



TPS2834, TPS2835
SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL

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Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|------------------|----------|-----|--|
| BOOT | 14 | I | Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 μ F and 1 μ F. |
| BOOTLO | 11 | O | This terminal connects to the junction of the high-side and low-side MOSFETs. |
| CROWBAR | 3 | I | CROWBAR can to be driven by an external OVP circuit to protect against a short across the high-side MOSFET. If CROWBAR is driven low, the low-side driver will be turned on and the high-side driver will be turned off, independent of the status of all other control terminals. |
| DT | 6 | I | Dead-time control terminal. Connect DT to the junction of the high-side and low-side MOSFETs. |
| ENABLE | 1 | I | If ENABLE is low, both drivers are off. |
| HIGHDR | 12 | O | Output drive for the high-side power MOSFET |
| IN | 2 | I | Input signal to the MOSFET drivers (noninverting input for the TPS2834; inverting input for the TPS2835). |
| LOWDR | 10 | O | Output drive for the low-side power MOSFET |
| NC | 4, 9, 13 | | No internal connection |
| PGND | 7 | | Power ground. Connect to the FET power ground. |
| SYNC | 5 | I | Synchronous rectifier enable terminal. If SYNC is low, the low-side driver is always off; If SYNC is high, the low-side driver provides gate drive to the low-side MOSFET. |
| V _{CC} | 8 | I | Input supply. Recommended that a 1- μ F capacitor be connected from V _{CC} to PGND. |

detailed description

low-side driver

The low-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

high-side driver

The high-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

dead-time (DT) control

Dead-time control prevents shoot-through current from flowing through the main power FETs during switching transitions by controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (V_{drain}) is low; the TTL-compatible DT terminal connects to the junction of the power FETs.

ENABLE

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low. ENABLE is a TTL-compatible digital terminal.

IN

The IN terminal is a TTL-compatible digital terminal that is the input control signal for the drivers. The TPS2834 has a noninverting input; the TPS2835 has an inverting input.



TPS2834, TPS2835 SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DEAD-TIME CONTROL

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detailed description (continued)

SYNC

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off. SYNC is a TTL-compatible digital terminal.

CROWBAR

The CROWBAR terminal overrides the normal operation of the driver. When CROWBAR is low, the low-side FET turns on to act as a clamp, protecting the output voltage of the dc/dc converter against overvoltages due to a short across the high-side FET. V_{IN} should be fused to protect the low-side FET. CROWBAR is a TTL-compatible digital terminal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|------------------------------|
| Supply voltage range, V_{CC} (see Note 1) | –0.3 V to 16 V |
| Input voltage range: BOOT to PGND (high-side driver ON) | –0.3 V to 30 V |
| BOOTLO to PGND | –0.3 V to 16 V |
| BOOT to BOOTLO | –0.3 V to 16 V |
| ENABLE, SYNC, and CROWBAR | –0.3 V to 16 V |
| IN | –0.3 V to 16 V |
| DT | –0.3 V to 30 V |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating virtual junction temperature range, T_J | –40°C to 125°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to PGND.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ | DERATING FACTOR | $T_A = 70^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ |
|---------------------|-----------------------------|-----------------|--------------------------|--------------------------|
| PWP with solder‡ | 2668 | 26.68 mW/°C | 1467 | 1067 |
| PWP without solder‡ | 1024 | 10.24 mW/°C | 563 | 409 |
| D | 749 | 7.49 mW/°C | 412 | 300 |

JUNCTION-CASE THERMAL RESISTANCE TABLE

| | | |
|-----|----------------------------------|-----------|
| PWP | Junction-case thermal resistance | 2.07 °C/W |
|-----|----------------------------------|-----------|

‡ Test Board Conditions:

1. Thickness: 0.062"
 2. 3" × 3" (for packages <27 mm long)
 3. 4" × 4" (for packages >27 mm long)
 4. 2-oz copper traces located on the top of the board (0.071 mm thick)
 5. Copper areas located on the top and bottom of the PCB for soldering
 6. Power and ground planes, 1-oz copper (0.036 mm thick)
 7. Thermal vias, 0.33 mm diameter, 1.5 mm pitch
 8. Thermal isolation of power plane
- For more information, refer to TI technical brief literature number SLMA002.



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recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--------------------------|--------------|-----|-----|-----|------|
| Supply voltage, V_{CC} | | 4.5 | | 15 | V |
| Input voltage | BOOT to PGND | 4.5 | | 28 | V |

**electrical characteristics over recommended operating virtual junction temperature range,
 $V_{CC} = 6.5$ V, ENABLE = High, $C_L = 3.3$ nF (unless otherwise noted)**

supply current

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|----------------------|---|--|-----|-----|-----|---------------|
| V_{CC} | Supply voltage range | | | 4.5 | | 15 | V |
| V_{CC} | Quiescent current | $V_{(ENABLE)} = \text{LOW}, V_{CC} = 15$ V | | | | 100 | μA |
| | | $V_{(ENABLE)} = \text{HIGH}, V_{CC} = 15$ V | | | 300 | 400 | |
| | | $V_{(ENABLE)} = \text{HIGH}, V_{CC} = 12$ V, $f_{(SWX)} = 200$ kHz, $C_{(HIGHDR)} = 50$ pF, See Note 2 | | | 3 | | mA |

NOTE 2: Ensured by design, not production tested.

TPS2834, TPS2835

SYNCHRONOUS-BUCK MOSFET DRIVERS

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**electrical characteristics over recommended operating virtual junction temperature range,
V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)**

output drivers

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|--|---|-----|-----|-----|------|
| Peak output current | High-side sink (see Note 3) | Duty cycle < 2%, t _{pw} < 100 μs (see Note 2) | V(BOOT) – V(BOOTLO) = 4.5 V, V(HIGHDR) = 4 V | 0.7 | 1.1 | | A |
| | | | V(BOOT) – V(BOOTLO) = 6.5 V, V(HIGHDR) = 5 V | 1.1 | 1.5 | | |
| | | | V(BOOT) – V(BOOTLO) = 12 V, V(HIGHDR) = 10.5 V | 2 | 2.4 | | |
| | High-side source (see Note 3) | Duty cycle < 2%, t _{pw} < 100 μs (see Note 2) | V(BOOT) – V(BOOTLO) = 4.5 V, V(HIGHDR) = 0.5V | 1.2 | 1.4 | | A |
| | | | V(BOOT) – V(BOOTLO) = 6.5 V, V(HIGHDR) = 1.5 V | 1.3 | 1.6 | | |
| | | | V(BOOT) – V(BOOTLO) = 12 V, V(HIGHDR) = 1.5 V | 2.3 | 2.7 | | |
| | Low-side sink (see Note 3) | Duty cycle < 2%, t _{pw} < 100 μs (see Note 2) | V _{CC} = 4.5 V, V(LOWDR) = 4 V | 1.3 | 1.8 | | A |
| | | | V _{CC} = 6.5 V, V(LOWDR) = 5 V | 2 | 2.5 | | |
| | | | V _{CC} = 12 V, V(LOWDR) = 10.5 V | 3 | 3.5 | | |
| | Low-side source (see Note 3) | Duty cycle < 2%, t _{pw} < 100 μs (see Note 2) | V _{CC} = 4.5 V, V(LOWDR) = 0.5V | 1.4 | 1.7 | | A |
| | | | V _{CC} = 6.5 V, V(LOWDR) = 1.5 V | 2 | 2.4 | | |
| | | | V _{CC} = 12 V, V(LOWDR) = 1.5 V | 2.5 | 3 | | |
| Output resistance | High-side sink (see Note 3) | | V(BOOT) – V(BOOTLO) = 4.5 V, V(HIGHDR) = 0.5 V | | | 5 | Ω |
| | | | V(BOOT) – V(BOOTLO) = 6.5 V, V(HIGHDR) = 0.5 V | | | 5 | |
| | | | V(BOOT) – V(BOOTLO) = 12 V, V(HIGHDR) = 0.5 V | | | 5 | |
| | High-side source (see Note 3) | | V(BOOT) – V(BOOTLO) = 4.5 V, V(HIGHDR) = 4 V | | | 75 | Ω |
| | | | V(BOOT) – V(BOOTLO) = 6.5 V, V(HIGHDR) = 6 V | | | 75 | |
| | | | V(BOOT) – V(BOOTLO) = 12 V, V(HIGHDR) = 11.5 V | | | 75 | |
| | Low-side sink (see Note 3) | | V(DRV) = 4.5 V, V(LOWDR) = 0.5 V | | | 9 | Ω |
| | | | V(DRV) = 6.5 V, V(LOWDR) = 0.5 V | | | 7.5 | |
| | | | V(DRV) = 12 V, V(LOWDR) = 0.5 V | | | 6 | |
| | Low-side source (see Note 3) | | V(DRV) = 4.5 V, V(LOWDR) = 4 V | | | 75 | Ω |
| | | | V(DRV) = 6.5 V, V(LOWDR) = 6 V | | | 75 | |
| | | | V(DRV) = 12 V, V(LOWDR) = 11.5 V | | | 75 | |

NOTES: 2: Ensured by design, not production tested.

3: The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the r_{DS(on)} of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

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**electrical characteristics over recommended operating virtual junction temperature range,
 $V_{CC} = 6.5\text{ V}$, $\text{ENABLE} = \text{High}$, $C_L = 3.3\text{ nF}$ (unless otherwise noted) (continued)**

dead-time control

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|-------|---|--------------------|-----|-----|------|
| V _{IH} | High-level input voltage | LOWDR | Over the V _{CC} range (see Note 2) | 0.7V _{CC} | | | V |
| V _{IL} | Low-level input voltage | | | 1 | | | |
| V _{IH} | High-level input voltage | DT | Over the V _{CC} range | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 1 | | | V |

NOTE 2: Ensured by design, not production tested.

digital control terminals (IN, CROWBAR, SYNC, ENABLE)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|--------------------------------|-----|-----|-----|------|
| V _{IH} | High-level input voltage | Over the V _{CC} range | 2 | | | V |
| V _{IL} | Low-level input voltage | | 1 | | | V |

**switching characteristics over recommended operating virtual junction temperature range,
 $\text{ENABLE} = \text{High}$, $C_L = 3.3\text{ nF}$ (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|---|-----|-----|-----|------|
| Rise time | HIGHDR output (see Note 2) | $V_{(\text{BOOT})} = 4.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 60 | ns |
| | | $V_{(\text{BOOT})} = 6.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 50 | |
| | | $V_{(\text{BOOT})} = 12\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 50 | |
| | LOWDR output (see Note 2) | $V_{CC} = 4.5\text{ V}$ | | | 40 | ns |
| | | $V_{CC} = 6.5\text{ V}$ | | | 30 | |
| | | $V_{CC} = 12\text{ V}$ | | | 30 | |
| Fall time | HIGHDR output (see Note 2) | $V_{(\text{BOOT})} = 4.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 50 | ns |
| | | $V_{(\text{BOOT})} = 6.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 40 | |
| | | $V_{(\text{BOOT})} = 12\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 40 | |
| | LOWDR output (see Note 2) | $V_{CC} = 4.5\text{ V}$ | | | 40 | ns |
| | | $V_{CC} = 6.5\text{ V}$ | | | 30 | |
| | | $V_{CC} = 12\text{ V}$ | | | 30 | |
| Propagation delay time | HIGHDR going low (excluding dead time) (see Note 2) | $V_{(\text{BOOT})} = 4.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 95 | ns |
| | | $V_{(\text{BOOT})} = 6.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 80 | |
| | | $V_{(\text{BOOT})} = 12\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 70 | |
| | LOWDR going high (excluding dead time) (see Note 2) | $V_{(\text{BOOT})} = 4.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 80 | ns |
| | | $V_{(\text{BOOT})} = 6.5\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 70 | |
| | | $V_{(\text{BOOT})} = 12\text{ V}$, $V_{(\text{BOOTLO})} = 0\text{ V}$ | | | 60 | |
| Propagation delay time | LOWDR going low (excluding dead time) (see Note 2) | $V_{CC} = 4.5\text{ V}$ | | | 80 | ns |
| | | $V_{CC} = 6.5\text{ V}$ | | | 70 | |
| | | $V_{CC} = 12\text{ V}$ | | | 60 | |
| Driver nonoverlap time | DT to LOWDR and LOWDR to HIGHDR (see Note 2) | $V_{CC} = 4.5\text{ V}$ | 40 | | 170 | ns |
| | | $V_{CC} = 6.5\text{ V}$ | 25 | | 135 | |
| | | $V_{CC} = 12\text{ V}$ | 15 | | 85 | |

NOTE 2: Ensured by design, not production tested.



TPS2834, TPS2835 SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DEAD-TIME CONTROL

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TYPICAL CHARACTERISTICS

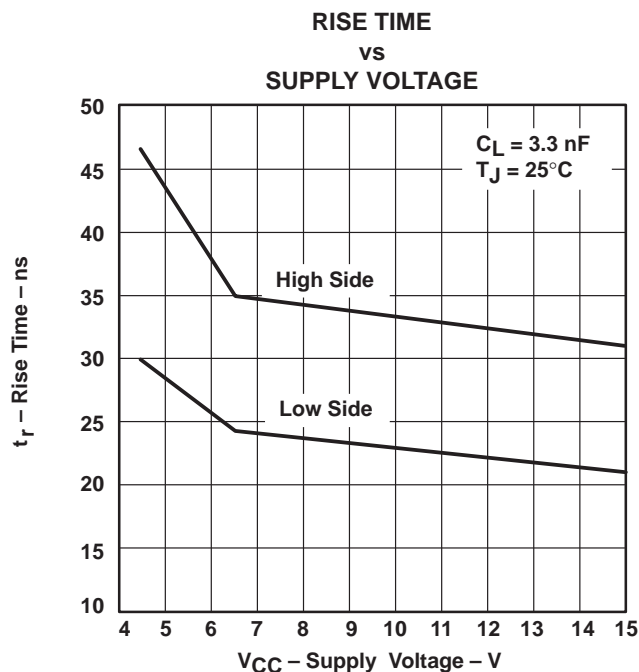


Figure 1

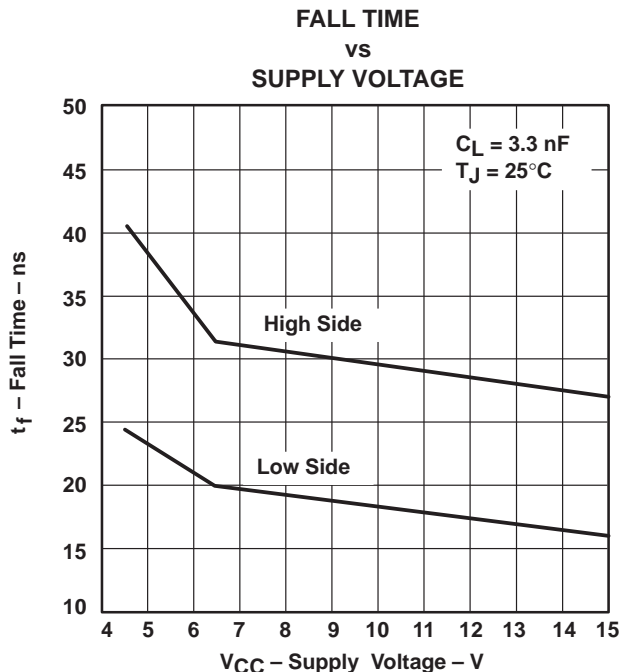


Figure 2

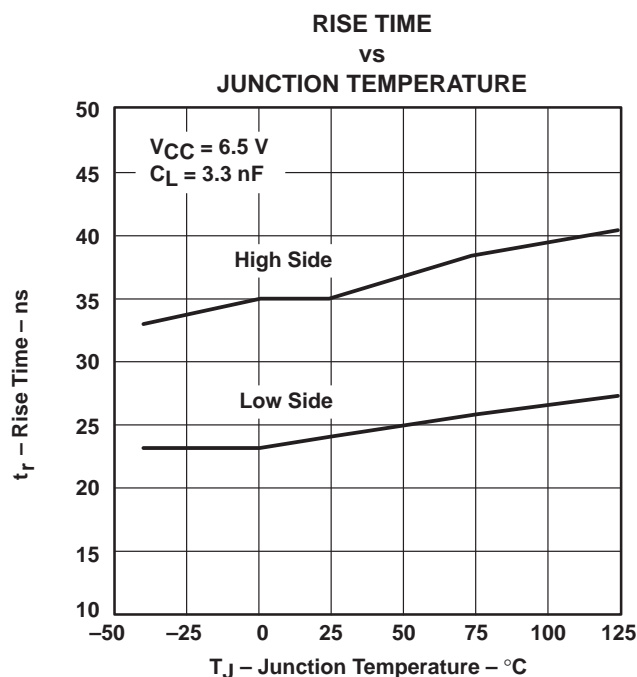


Figure 3

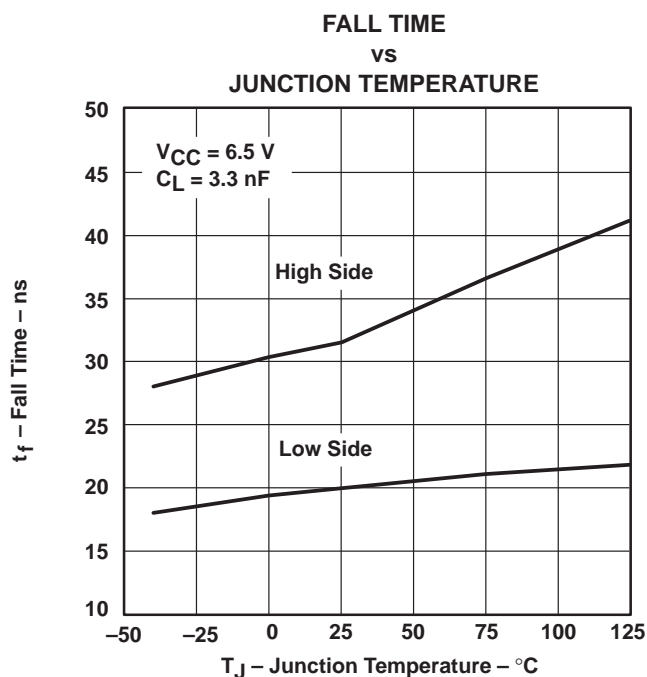


Figure 4

TYPICAL CHARACTERISTICS

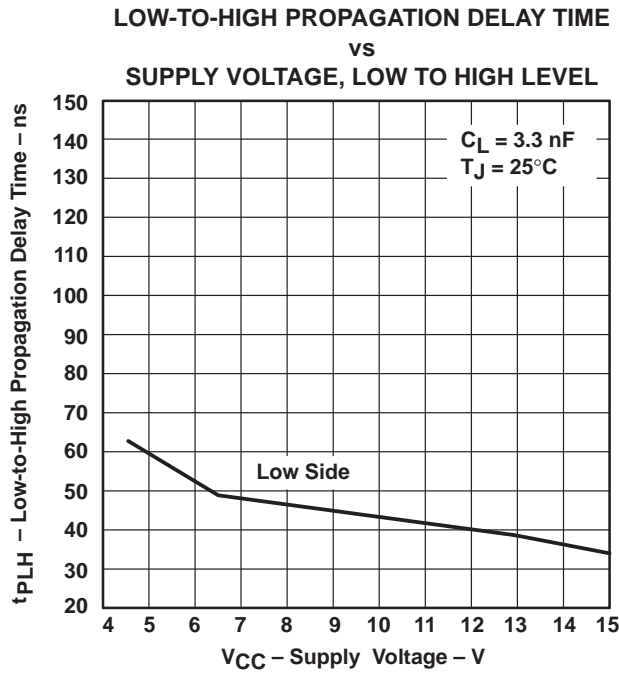


Figure 5

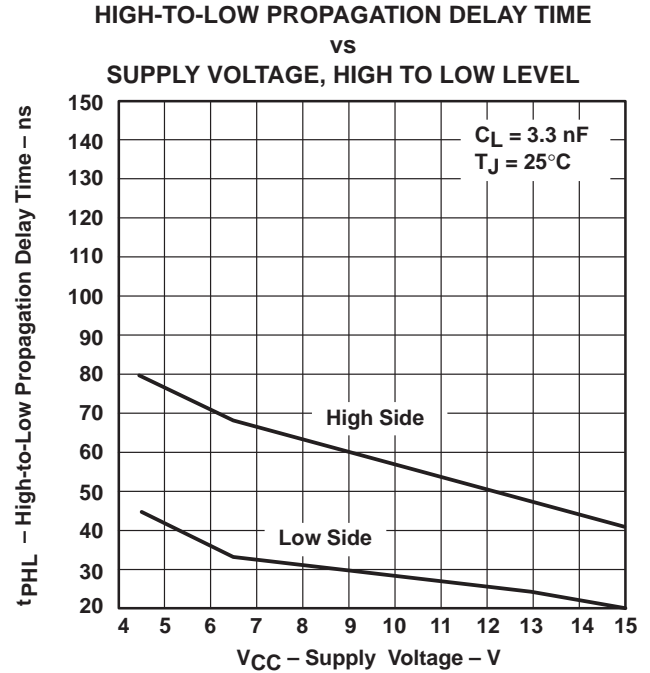


Figure 6

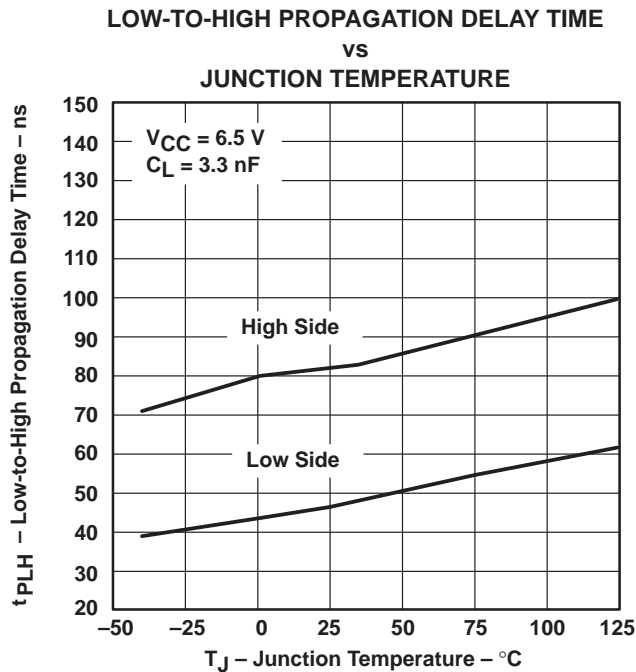


Figure 7

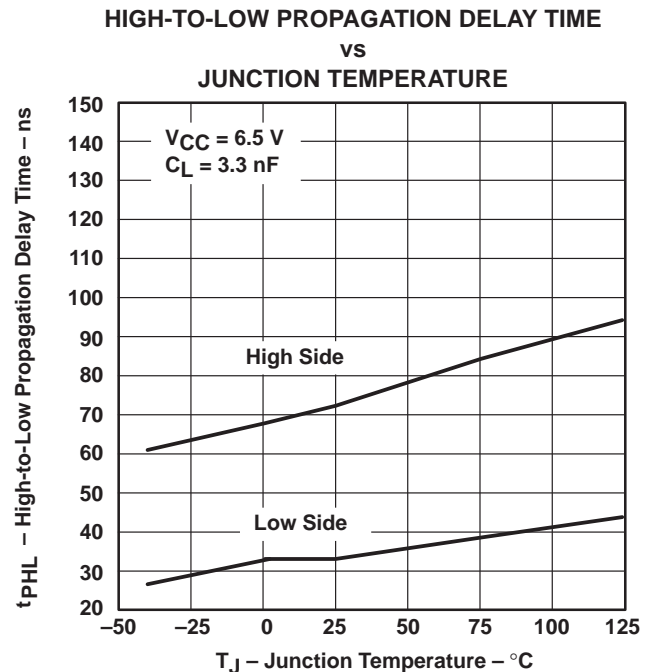


Figure 8

TPS2834, TPS2835 SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DEAD-TIME CONTROL

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TYPICAL CHARACTERISTICS

DRIVER-OUTPUT RISE TIME
vs
LOAD CAPACITANCE

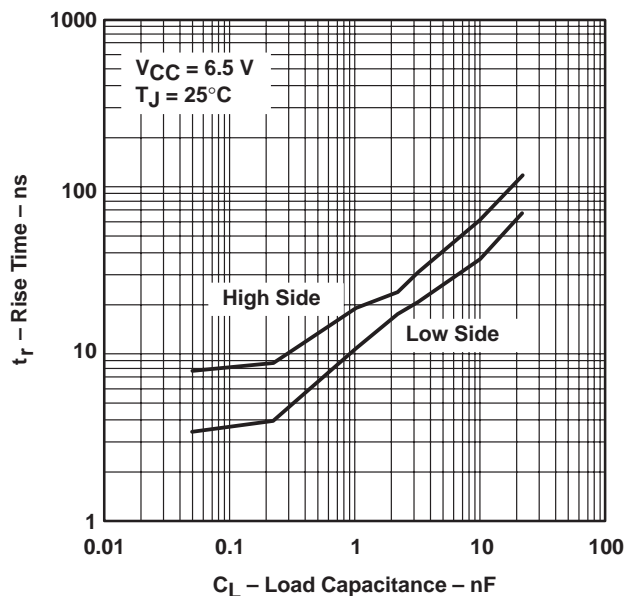


Figure 9

DRIVER-OUTPUT FALL TIME
vs
LOAD CAPACITANCE

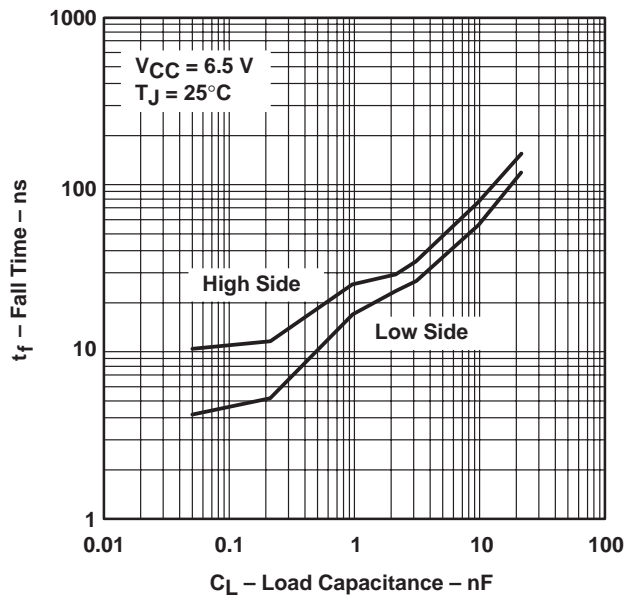


Figure 10

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

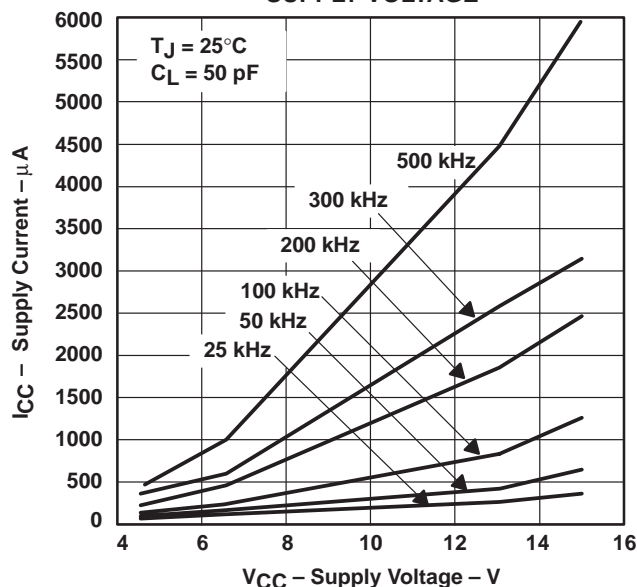


Figure 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

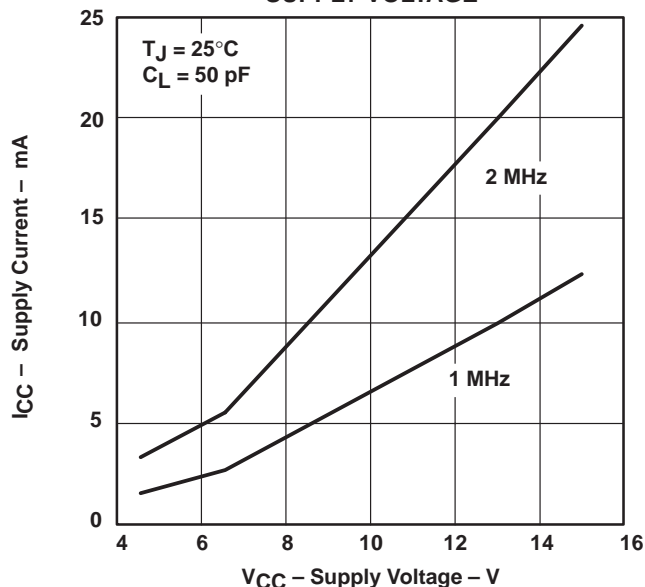


Figure 12

TYPICAL CHARACTERISTICS

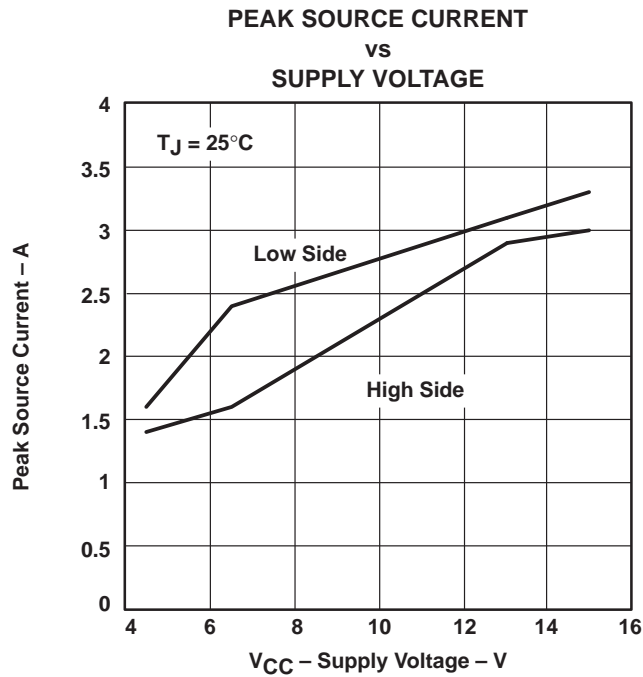


Figure 13

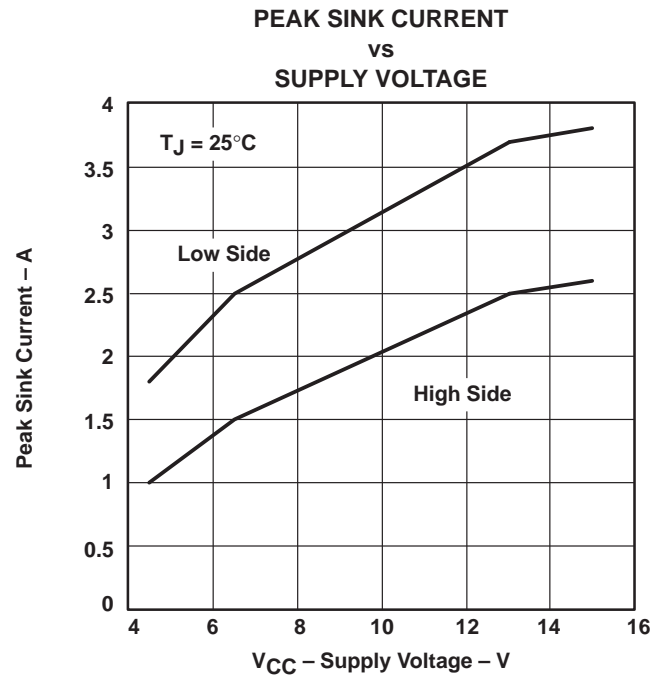


Figure 14

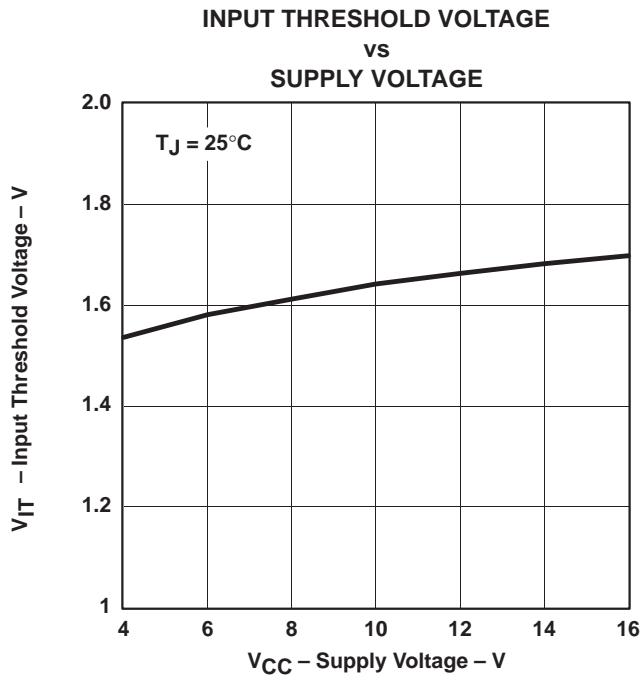


Figure 15

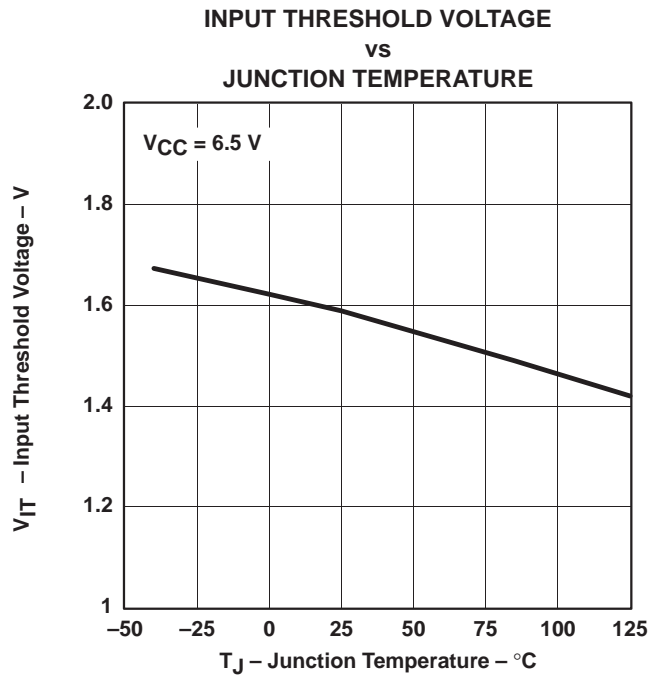


Figure 16

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Figure 17 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2835 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3 A continuous load. The converter achieves an efficiency of 94% for $V_{IN} = 5$ V, $I_{load} = 1$ A, and 93% for $V_{IN} = 5$ V, $I_{load} = 3$ A.



APPLICATION INFORMATION

Great care should be taken when laying out the PC board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A). This node is very sensitive to noise pickup and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have other EMI problems and the power supply will be relatively free of noise.

TPS2834, TPS2835
SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL

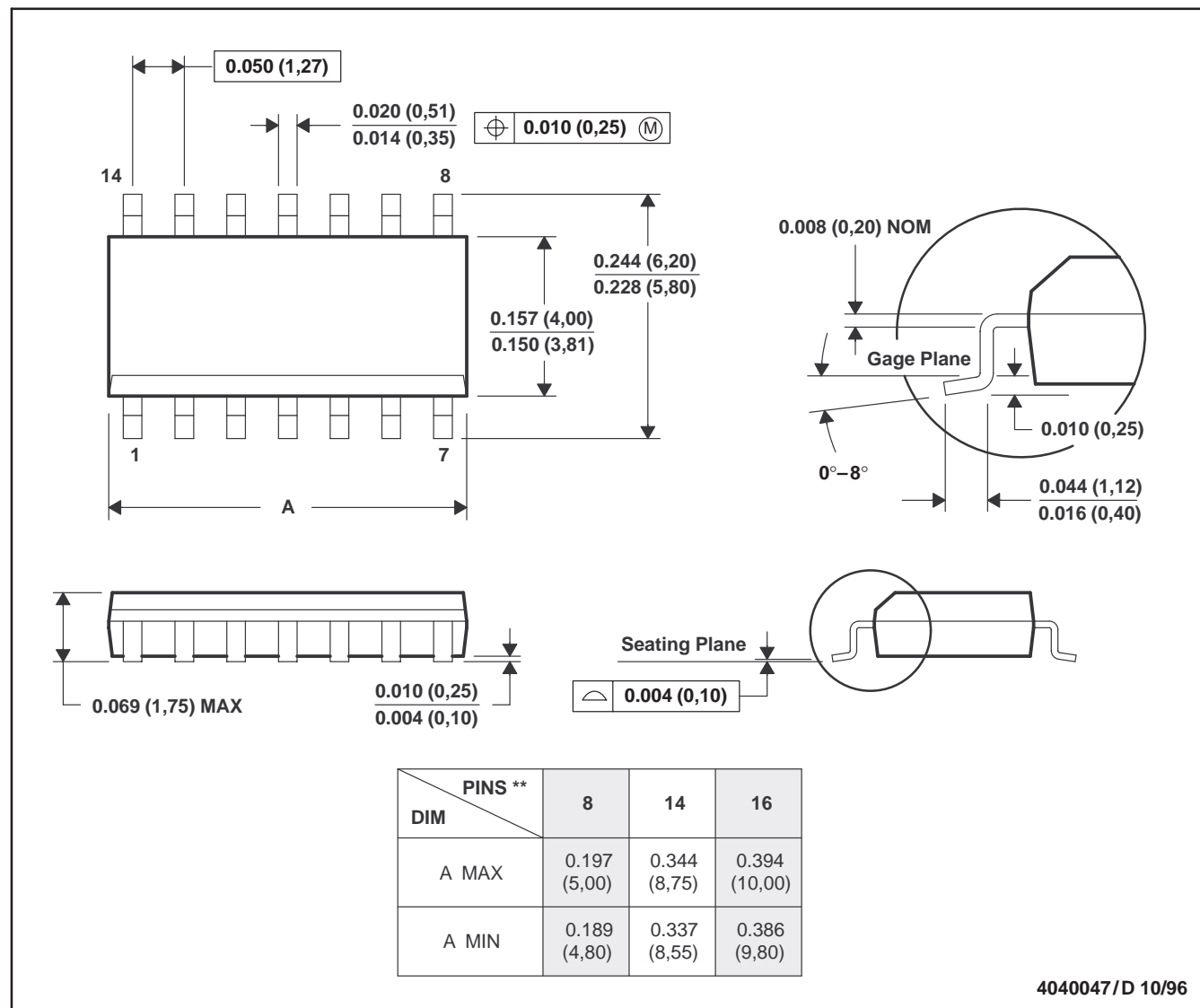
SLVS223A – NOVEMBER 1999 – REVISED JANUARY 2001

MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

TPS2834, TPS2835
SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL

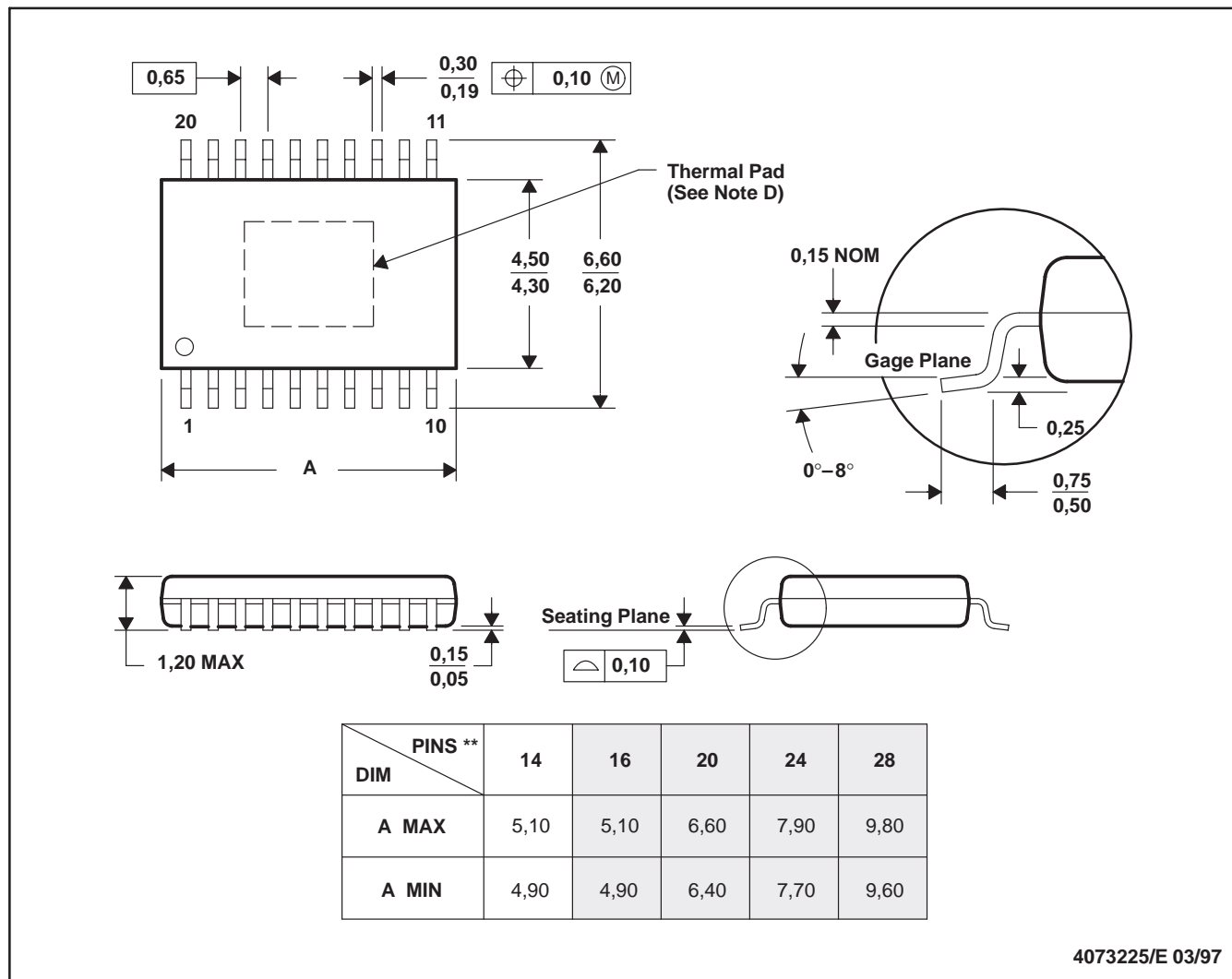
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MECHANICAL DATA

PWP (R-PDSO-G)**

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20-PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions.
 - D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 - E. Falls within JEDEC MO-153

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