features

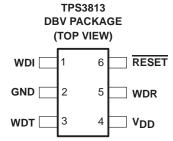
- Window-Watchdog With Programmable Delay and Window Ratio
- 6-Pin SOT-23 Package
- Supply Current of 9 μA (Typ)
- Power On Reset Generator With a Fixed Delay Time of 25 ms
- Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V
- Open-Drain Reset Output
- Temperature Range . . . –40°C to 85°C

description

The TPS3813 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

typical applications

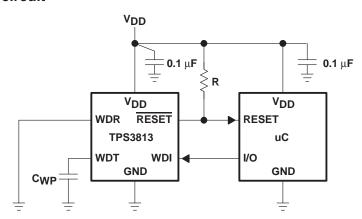
- Applications Using DSPs, Microcontrollers, or Microprocessors
- Safety Critical Systems
- Automotive Systems
- Heating Systems



During power on, \overline{RESET} is asserted when supply voltage (V_{DD}) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps \overline{RESET} active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d = 25 ms typical, starts after V_{DD} has risen above the threshold voltage (V_{IT}). When the supply voltage drops below the threshold voltage (V_{IT}), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

For safety critical applications the TPS3813 family incorporates a so-called window-watchdog with programmable delay and window ratio. The upper limit of the watchdog time-out can be set by either connecting WDT to GND, V_{DD} , or using an external capacitor. The lower limit and thus the window ratio is set by connecting WDR to GND or V_{DD} . The supervised processor now needs to trigger the TPS3813 within this window not to assert a \overline{RESET} .

typical operating circuit





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



description continued

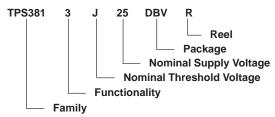
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 6-pin SOT-23 package.

The TPS3813 devices are characterized for operation over a temperature range of -40°C to 85°C.

PACKAGE INFORMATION

| TA | DEVICE NAME | THRESHOLD VOLTAGE | MARKING | |
|---------------|----------------------|-------------------|---------|--|
| | TPS3813J25DBV 2.25 V | | PCDI | |
| 4000 1- 0500 | TPS3813L30DBV | 2.64 V | PEZI | |
| -40°C to 85°C | TPS3813K33DBV | 2.93 V | PFAI | |
| | TPS3813I50DBV | 4.55 V | PFBI | |

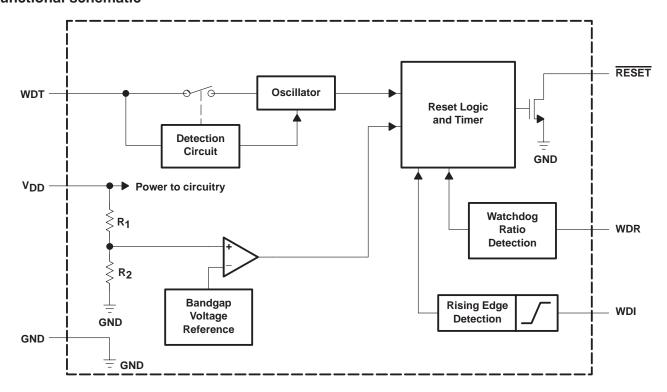
ordering information



TPS3813 FUNCTION/TRUTH TABLE

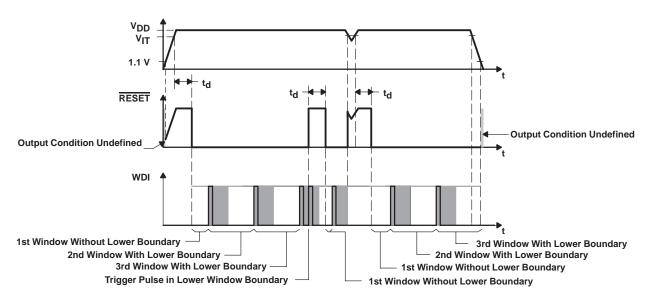
| V _{DD} > V _{IT} | RESET |
|-----------------------------------|-------|
| 0 | L |
| 1 | Н |

functional schematic





timing diagram



Terminal Functions

| TERMINAL | | | DESCRIPTION | | | | | |
|----------|-----|-----|-------------------------------------|--|--|--|--|--|
| NAME | NO. | 1/0 | DESCRIPTION | | | | | |
| GND | 2 | I | Ground | | | | | |
| RESET | 6 | 0 | pen-drain reset output | | | | | |
| V_{DD} | 4 | I | ply voltage and supervising input | | | | | |
| WDI | 1 | I | Watchdog timer input | | | | | |
| WDR | 5 | I | ectable watchdog window ratio input | | | | | |
| WDT | 3 | I | ogrammable watchdog delay input | | | | | |

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| Supply voltage, V _{DD} (see Note1) | |
|---|------------------------------|
| All other pins (see Note 1) | 0.3 V to 7 V |
| Maximum low output current, I _{OL} | 5 mA |
| Maximum high output current, I _{OH} | –5 mA |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) | ±20 mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}) | ±20 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T _A | –40°C to 85°C |
| Storage temperature range, T _{sta} | –65°C to 150°C |
| Soldering temperature | 260°C |
| | |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

| PACKAGE | T _A <25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|--------------------------------------|--|---------------------------------------|---------------------------------------|
| DBV | 437 mW | 3.5 mW/°C | 280 mW | 227 mW |



NOTE 1: All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously.

TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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recommended operating conditions at specified temperature range

| | MIN | MAX | UNIT |
|--|-----------------------|-----------------------|------|
| Supply voltage, V _{DD} | 2 | 6 | V |
| Input voltage, V _I | 0 | V _{DD} + 0.3 | V |
| High-level input voltage, V _{IH} | 0.7 x V _{DD} | | V |
| Low-level input voltage, V _{IL} | | 0.3 x V _{DD} | V |
| Input transition rise and fall rate, Δt/ΔV | | 100 | ns/V |
| Pulse width of WDI trigger pulse, t _W | 50 | | ns |
| Operating free-air temperature range, TA | -40 | 85 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|----------------------------------|--|---|------|------|------|------|
| | Low-level output voltage | | $V_{DD} = 2 \text{ V to 6 V}, I_{OL} = 500 \mu\text{A}$ | | | 0.2 | |
| VOL | | | $V_{DD} = 3.3 \text{ V}$ $I_{OL} = 2 \text{ mA}$ | | | 0.4 | V |
| | | | $V_{DD} = 6 V$, $I_{OL} = 4 mA$ | | | 0.4 | |
| | Power up reset voltage (see Note | 2) | $V_{DD} \ge 1.1 \text{ V}, \qquad I_{OL} = 50 \mu\text{A}$ | | | 0.2 | V |
| | | TPS3813J25 | | 2.2 | 2.25 | 2.3 | V |
| ., | Negative-going input threshold | TPS3813L30 | T 4000 0500 | 2.58 | 2.64 | 2.7 | |
| VIT | voltage (see Note 3) | TPS3813K33 | $T_A = -40^{\circ}C - 85^{\circ}C$ | 2.87 | 2.93 | 3 | |
| | | TPS3813I50 | 1 | 4.45 | 4.55 | 4.65 | |
| | | TPS3813J25 | | | 30 | | |
| | Hysteresis | TPS3813L30 |] | | 35 | | ., |
| V_{hys} | | TPS3813K33 | 1 | | 40 | | mV |
| | | TPS3813I50 | 1 | | 60 | | |
| | | WDI, WDR | $WDI = V_{DD} = 6 \text{ V}, WDR = V_{DD} = 6 \text{ V}$ | -25 | | 25 | |
| lн | High-level input current | WDT | $\frac{\text{WDT} = \text{V}_{DD} = 6 \text{ V}, \text{ V}_{DD} > \text{V}_{IT}}{\text{RESET} = \text{High}}$ | -100 | | 100 | nA |
| | | | WDI = 0 V, WDR = 0 V, V _{DD} = 6 V | -25 | | 25 | ПА |
| I _{IL} | Low-level input current | WDT | WDT = 0 V, $V_{DD} > V_{IT}$, $\overline{RESET} = High$ | -100 | | 100 | |
| loh | High-level output current | • | $V_{DD} = V_{IT} + 0.2 \text{ V}, V_{OH} = V_{DD}$ | | | 25 | nA |
| | • | V _{DD} = 2 V output unconnected | V _{DD} = 2 V output unconnected | | 9 | 13 | |
| IDD | Supply current | | V _{DD} = 5 V output unconnected | | 20 | 25 | μΑ |
| Ci | Input capacitance | | $V_I = 0 V \text{ to } V_{DD}$ | | 5 | | pF |

NOTES: 2. The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_r, V_{DD} \ge 15 \,\mu\text{s/V}$.

timing requirements at R_L = 1 M Ω , C_L = 50 pF, T_A = -40°C to 85°C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------|--------------------------------|---|-----|-----|-----|------|
| t_{W} | Pulse width at V _{DD} | $V_{DD} = V_{IT-} + 0.2 \text{ V}, V_{DD} = V_{IT-} - 0.2 \text{ V}$ | 3 | | | μs |

^{3.} To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals.

TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

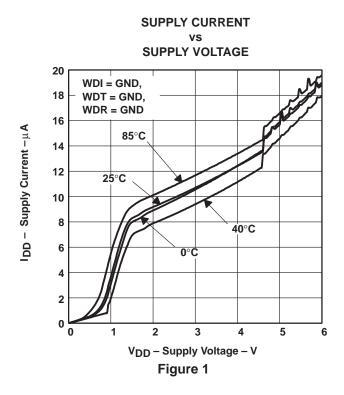
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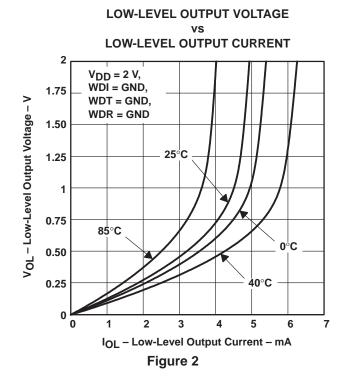
switching characteristics at R $_L$ = 1 M $\Omega,$ C $_L$ = 50 pF, T $_A$ = $-40^{\circ}C$ to 85 $^{\circ}C$

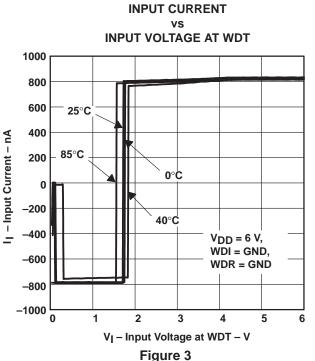
| | PARAMETER | R | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|--------------------------------|--|------|---------------|------|---------------|
| t _d | d Delay time | | $V_{DD} \ge V_{IT} + 0.2 V$, See timing diagram | 15 | 25 | 35 | ms |
| | | | WDT = 0 V | 0.15 | 0.25 | 0.35 | ms s ms |
| tu | Watchdog time-out | Upper limit | $WDT = V_{DD}$ | 1.5 | 2.5 | 3.5 | S |
| ^t t(out) | wateridog time out | оррог шин | WDT = Programmable (see Note 4) | | See Note 5 | | ms |
| | | | WDR = 0 V, WDT = 0 V | | 1:31.8 | | |
| | | | $WDR = 0 V, WDT = V_{DD}$ | | 1:32 | | |
| | Watchdog window ratio | | WDR = 0 V, WDT = Programmable | | 1:25.8 | | |
| | | | $WDR = V_{DD}$, $WDT = 0 V$ | | 1:124.9 | | |
| | | | $WDR = V_{DD}$, $WDT = V_{DD}$ | | 1:127.7 | | |
| tPHL | Propagation (delay) time, high-to-low-level output | V _{DD} to RESET delay | V _{IL} = V _{IT} - 0.2 V, V _{IH} = V _{IT} + 0.2 V | | 30 | 50 | μs |

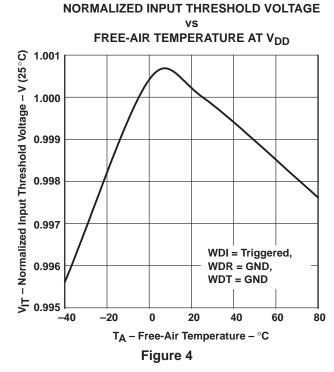
NOTES: 4. $155 \text{ pF} < C_{(EXT)} < 63 \text{ nF}$ 5. $C_{(EXT)} \div 15.55 \text{ pF} + 1 \times 6.25 \text{ ms}$

TYPICAL CHARACTERISTICS









TYPICAL CHARACTERISTICS

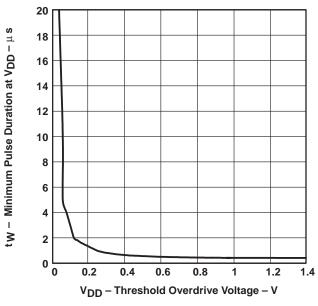
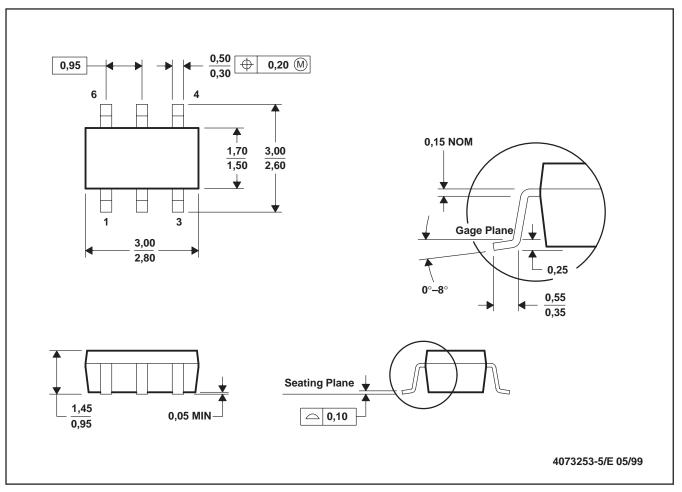


Figure 5

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

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