

PowerMOS transistor  
Logic level TOPFET

BUK108-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

- General controller for driving
- lamps
  - motors
  - solenoids
  - heaters

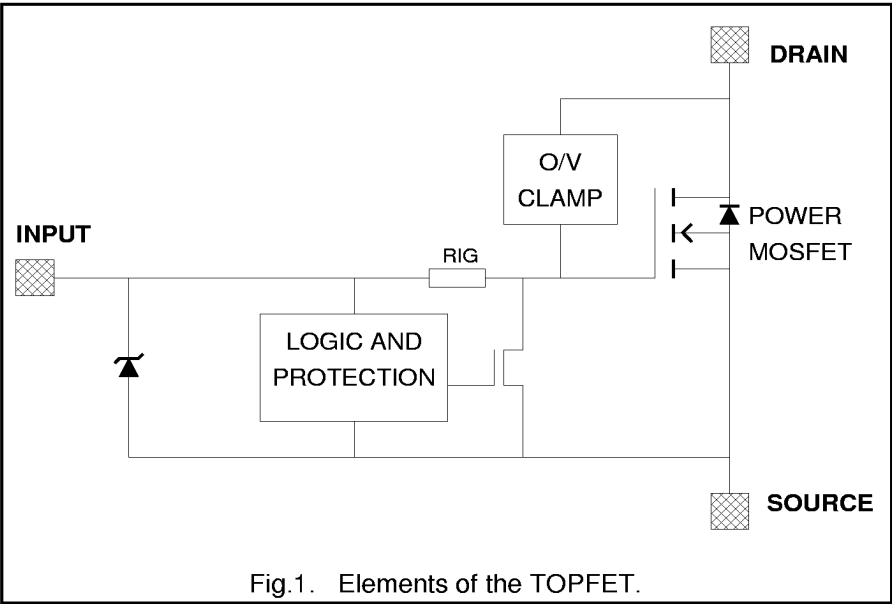
FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

| SYMBOL       | PARAMETER                                                 | MAX. | UNIT |
|--------------|-----------------------------------------------------------|------|------|
| $V_{DS}$     | Continuous drain source voltage                           | 50   | V    |
| $I_D$        | Continuous drain current                                  | 13.5 | A    |
| $P_D$        | Total power dissipation                                   | 40   | W    |
| $T_j$        | Continuous junction temperature                           | 150  | °C   |
| $R_{DS(ON)}$ | Drain-source on-state resistance<br>$V_{IS} = 5\text{ V}$ | 125  | mΩ   |

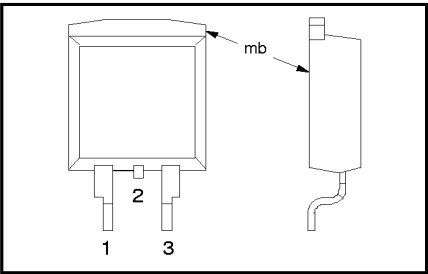
FUNCTIONAL BLOCK DIAGRAM



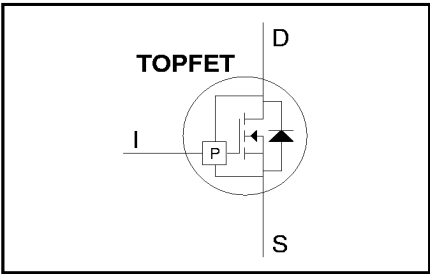
PINNING - SOT404

| PIN | DESCRIPTION |
|-----|-------------|
| 1   | input       |
| 2   | drain       |
| 3   | source      |
| mb  | drain       |

PIN CONFIGURATION



SYMBOL



# PowerMOS transistor

## Logic level TOPFET

BUK108-50GL

### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

| SYMBOL     | PARAMETER                                              | CONDITIONS                                       | MIN. | MAX. | UNIT |
|------------|--------------------------------------------------------|--------------------------------------------------|------|------|------|
| $V_{DSS}$  | Continuous off-state drain source voltage <sup>1</sup> | $V_{IS} = 0\text{ V}$                            | -    | 50   | V    |
| $V_{IS}$   | Continuous input voltage                               | -                                                | 0    | 6    | V    |
| $I_D$      | Continuous drain current                               | $T_{mb} \leq 25\text{ °C}; V_{IS} = 5\text{ V}$  | -    | 13.5 | A    |
| $I_D$      | Continuous drain current                               | $T_{mb} \leq 100\text{ °C}; V_{IS} = 5\text{ V}$ | -    | 8.5  | A    |
| $I_{DRM}$  | Repetitive peak on-state drain current                 | $T_{mb} \leq 25\text{ °C}; V_{IS} = 5\text{ V}$  | -    | 54   | A    |
| $P_D$      | Total power dissipation                                | $T_{mb} \leq 25\text{ °C}$                       | -    | 40   | W    |
| $T_{stg}$  | Storage temperature                                    | -                                                | -55  | 150  | °C   |
| $T_j$      | Continuous junction temperature <sup>2</sup>           | normal operation                                 | -    | 150  | °C   |
| $T_{sold}$ | Lead temperature                                       | during soldering                                 | -    | 250  | °C   |

### OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

| SYMBOL       | PARAMETER                                          | CONDITIONS              | MIN. | MAX. | UNIT |
|--------------|----------------------------------------------------|-------------------------|------|------|------|
| $V_{ISP}$    | Protection supply voltage <sup>3</sup>             | for valid protection    | 4    | -    | V    |
|              | <b>Over temperature protection</b>                 |                         |      |      |      |
| $V_{DDP(T)}$ | Protected drain source supply voltage              | $V_{IS} = 5\text{ V}$   | -    | 50   | V    |
|              | <b>Short circuit load protection</b>               |                         |      |      |      |
| $V_{DDP(P)}$ | Protected drain source supply voltage <sup>4</sup> | $V_{IS} = 5\text{ V}$   | -    | 35   | V    |
| $P_{DSM}$    | Instantaneous overload dissipation                 | $T_{mb} = 25\text{ °C}$ | -    | 0.6  | kW   |

### OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

| SYMBOL     | PARAMETER                        | CONDITIONS                                                                                       | MIN. | MAX. | UNIT |
|------------|----------------------------------|--------------------------------------------------------------------------------------------------|------|------|------|
| $I_{DROM}$ | Repetitive peak clamping current | $V_{IS} = 0\text{ V}$                                                                            | -    | 15   | A    |
| $E_{DSM}$  | Non-repetitive clamping energy   | $T_{mb} \leq 25\text{ °C}; I_{DM} = 15\text{ A};$<br>$V_{DD} \leq 20\text{ V};$ inductive load   | -    | 200  | mJ   |
| $E_{DRM}$  | Repetitive clamping energy       | $T_{mb} \leq 95\text{ °C}; I_{DM} = 4\text{ A};$<br>$V_{DD} \leq 20\text{ V}; f = 250\text{ Hz}$ | -    | 20   | mJ   |

### ESD LIMITING VALUE

| SYMBOL | PARAMETER                                 | CONDITIONS                                                       | MIN. | MAX. | UNIT |
|--------|-------------------------------------------|------------------------------------------------------------------|------|------|------|
| $V_C$  | Electrostatic discharge capacitor voltage | Human body model;<br>$C = 250\text{ pF}; R = 1.5\text{ k}\Omega$ | -    | 2    | kV   |

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher  $T_j$  is allowed as an overload condition but at the threshold  $T_{j(TO)}$  the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed  $V_{DDP(P)}$  maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

# PowerMOS transistor

## Logic level TOPFET

BUK108-50GL

### THERMAL CHARACTERISTICS

| SYMBOL         | PARAMETER                                       | CONDITIONS                                 | MIN. | TYP. | MAX. | UNIT |
|----------------|-------------------------------------------------|--------------------------------------------|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance<br>Junction to mounting base | -                                          | -    | 2.5  | 3.1  | K/W  |
| $R_{th\ j-a}$  | Thermal resistance<br>Junction to ambient       | minimum footprint FR4 PCB<br>(see fig. 32) | -    | 50   | -    | K/W  |

### STATIC CHARACTERISTICS

 $T_{mb} = 25\ ^\circ\text{C}$  unless otherwise specified

| SYMBOL        | PARAMETER                        | CONDITIONS                                                                                              | MIN. | TYP. | MAX. | UNIT          |
|---------------|----------------------------------|---------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{(CL)DSS}$ | Drain-source clamping voltage    | $V_{IS} = 0\ \text{V}$ ; $I_D = 10\ \text{mA}$                                                          | 50   | -    | -    | V             |
| $V_{(CL)DSS}$ | Drain-source clamping voltage    | $V_{IS} = 0\ \text{V}$ ; $I_{DM} = 1\ \text{A}$ ; $t_p \leq 300\ \mu\text{s}$ ;<br>$\delta \leq 0.01$   | -    | -    | 70   | V             |
| $I_{DSS}$     | Zero input voltage drain current | $V_{DS} = 12\ \text{V}$ ; $V_{IS} = 0\ \text{V}$                                                        | -    | 0.5  | 10   | $\mu\text{A}$ |
| $I_{DSS}$     | Zero input voltage drain current | $V_{DS} = 50\ \text{V}$ ; $V_{IS} = 0\ \text{V}$                                                        | -    | 1    | 20   | $\mu\text{A}$ |
| $I_{DSS}$     | Zero input voltage drain current | $V_{DS} = 40\ \text{V}$ ; $V_{IS} = 0\ \text{V}$ ; $T_j = 125\ ^\circ\text{C}$                          | -    | 10   | 100  | $\mu\text{A}$ |
| $R_{DS(ON)}$  | Drain-source on-state resistance | $V_{IS} = 5\ \text{V}$ ; $I_{DM} = 7.5\ \text{A}$ ; $t_p \leq 300\ \mu\text{s}$ ;<br>$\delta \leq 0.01$ | -    | 85   | 125  | m $\Omega$    |

### OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

| SYMBOL       | PARAMETER                                                               | CONDITIONS                                                                                                   | MIN. | TYP. | MAX. | UNIT             |
|--------------|-------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|------|------|------|------------------|
| $E_{DS(TO)}$ | Short circuit load protection <sup>1</sup><br>Overload threshold energy | $T_{mb} = 25\ ^\circ\text{C}$ ; $L \leq 10\ \mu\text{H}$<br>$V_{DD} = 13\ \text{V}$ ; $V_{IS} = 5\ \text{V}$ | -    | 0.2  | -    | J                |
| $t_{d\ sc}$  | Response time                                                           | $V_{DD} = 13\ \text{V}$ ; $V_{IS} = 5\ \text{V}$                                                             | -    | 0.8  | -    | ms               |
| $T_{j(TO)}$  | Over temperature protection<br>Threshold junction temperature           | $V_{IS} = 5\ \text{V}$ ; from $I_D \geq 0.5\ \text{A}^2$                                                     | 150  | -    | -    | $^\circ\text{C}$ |

### INPUT CHARACTERISTICS

 $T_{mb} = 25\ ^\circ\text{C}$  unless otherwise specified. The supply for the logic and overload protection is taken from the input.

| SYMBOL       | PARAMETER                             | CONDITIONS                                    | MIN. | TYP. | MAX. | UNIT       |
|--------------|---------------------------------------|-----------------------------------------------|------|------|------|------------|
| $V_{IS(TO)}$ | Input threshold voltage               | $V_{DS} = 5\ \text{V}$ ; $I_D = 1\ \text{mA}$ | 1.0  | 1.5  | 2.0  | V          |
| $I_{IS}$     | Input supply current                  | $V_{IS} = 5\ \text{V}$ ; normal operation     | -    | 0.2  | 0.35 | mA         |
| $V_{ISR}$    | Protection reset voltage <sup>3</sup> |                                               | 2.0  | 2.6  | 3.5  | V          |
| $V_{ISR}$    | Protection reset voltage              | $T_j = 150\ ^\circ\text{C}$                   | 1.0  | -    | -    |            |
| $I_{ISL}$    | Input supply current                  | $V_{IS} = 5\ \text{V}$ ; protection latched   | 0.5  | 1.2  | 2.0  | mA         |
| $V_{(BR)IS}$ | Input clamp voltage                   | $I_I = 10\ \text{mA}$                         | 6    | -    | -    | V          |
| $R_{IG}$     | Input series resistance               | to gate of power MOSFET                       | -    | 4    | -    | k $\Omega$ |

<sup>1</sup> The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for  $P_{DSM}$ , which is always the case when  $V_{DS}$  is less than  $V_{DSF}$  maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

<sup>2</sup> The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum  $I_D$  ensures this condition.

<sup>3</sup> The input voltage below which the overload protection circuits will be reset.

# PowerMOS transistor

## Logic level TOPFET

BUK108-50GL

### TRANSFER CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ 

| SYMBOL      | PARAMETER                  | CONDITIONS                                                                                                 | MIN. | TYP. | MAX. | UNIT |
|-------------|----------------------------|------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $g_{fs}$    | Forward transconductance   | $V_{DS} = 10\text{ V}$ ; $I_{DM} = 7.5\text{ A}$ $t_p \leq 300\text{ }\mu\text{s}$ ;<br>$\delta \leq 0.01$ | 5    | 9    | -    | S    |
| $I_{D(SC)}$ | Drain current <sup>1</sup> | $V_{DS} = 13\text{ V}$ ; $V_{IS} = 5\text{ V}$                                                             | -    | 25   | -    | A    |

### SWITCHING CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ .  $R_l = 50\text{ }\Omega$ . Refer to waveform figures and test circuits.

| SYMBOL             | PARAMETER           | CONDITIONS                                                                               | MIN. | TYP. | MAX. | UNIT          |
|--------------------|---------------------|------------------------------------------------------------------------------------------|------|------|------|---------------|
| $t_{d\text{ on}}$  | Turn-on delay time  | $V_{DD} = 13\text{ V}$ ; $V_{IS} = 5\text{ V}$<br>resistive load $R_L = 4\text{ }\Omega$ | -    | 1.5  | -    | $\mu\text{s}$ |
| $t_r$              | Rise time           |                                                                                          | -    | 8    | -    | $\mu\text{s}$ |
| $t_{d\text{ off}}$ | Turn-off delay time | $V_{DD} = 13\text{ V}$ ; $V_{IS} = 0\text{ V}$<br>resistive load $R_L = 4\text{ }\Omega$ | -    | 6    | -    | $\mu\text{s}$ |
| $t_f$              | Fall time           |                                                                                          | -    | 4.5  | -    | $\mu\text{s}$ |
| $t_{d\text{ on}}$  | Turn-on delay time  | $V_{DD} = 13\text{ V}$ ; $V_{IS} = 5\text{ V}$<br>inductive load $I_{DM} = 3\text{ A}$   | -    | 1.5  | -    | $\mu\text{s}$ |
| $t_r$              | Rise time           |                                                                                          | -    | 1    | -    | $\mu\text{s}$ |
| $t_{d\text{ off}}$ | Turn-off delay time | $V_{DD} = 13\text{ V}$ ; $V_{IS} = 0\text{ V}$<br>inductive load $I_{DM} = 3\text{ A}$   | -    | 10   | -    | $\mu\text{s}$ |
| $t_f$              | Fall time           |                                                                                          | -    | 0.5  | -    | $\mu\text{s}$ |

### REVERSE DIODE LIMITING VALUE

| SYMBOL | PARAMETER                  | CONDITIONS                                                       | MIN. | MAX. | UNIT |
|--------|----------------------------|------------------------------------------------------------------|------|------|------|
| $I_S$  | Continuous forward current | $T_{mb} \leq 25\text{ }^{\circ}\text{C}$ ; $V_{IS} = 0\text{ V}$ | -    | 13.5 | A    |

### REVERSE DIODE CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ 

| SYMBOL    | PARAMETER             | CONDITIONS                                                                   | MIN. | TYP. | MAX. | UNIT |
|-----------|-----------------------|------------------------------------------------------------------------------|------|------|------|------|
| $V_{SDS}$ | Forward voltage       | $I_S = 15\text{ A}$ ; $V_{IS} = 0\text{ V}$ ; $t_p = 300\text{ }\mu\text{s}$ | -    | 1.0  | 1.5  | V    |
| $t_{rr}$  | Reverse recovery time | not applicable <sup>2</sup>                                                  | -    | -    | -    | -    |

### ENVELOPE CHARACTERISTICS

| SYMBOL | PARAMETER                  | CONDITIONS                                                      | MIN. | TYP. | MAX. | UNIT |
|--------|----------------------------|-----------------------------------------------------------------|------|------|------|------|
| $L_d$  | Internal drain inductance  | Measured from upper edge of tab<br>to centre of die             | -    | 2.5  | -    | nH   |
| $L_s$  | Internal source inductance | Measured from source lead<br>soldering point to source bond pad | -    | 7.5  | -    | nH   |

<sup>1</sup> During overload before short circuit load protection operates.

<sup>2</sup> The reverse diode of this type is not intended for applications requiring fast reverse recovery.

# PowerMOS transistor

## Logic level TOPFET

BUK108-50GL

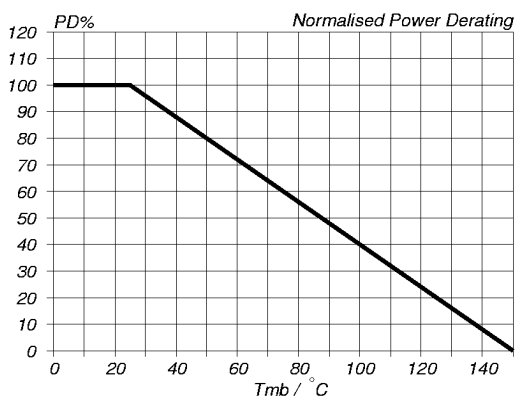


Fig.2. Normalised limiting power dissipation.  
 $P_D\% = 100 \cdot P_D / P_D(25^\circ\text{C}) = f(T_{mb})$

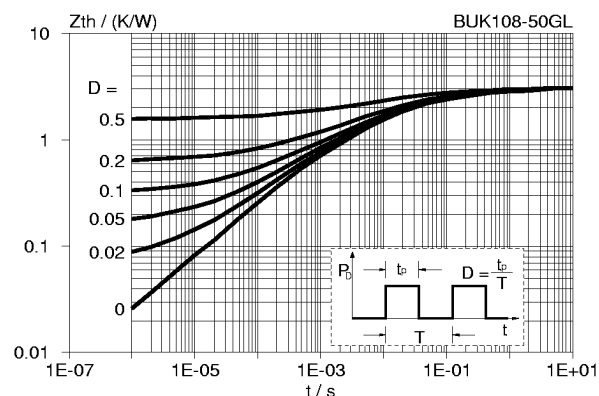


Fig.5. Transient thermal impedance.  
 $Z_{th\ j-mb} = f(t)$ ; parameter  $D = t_p / T$

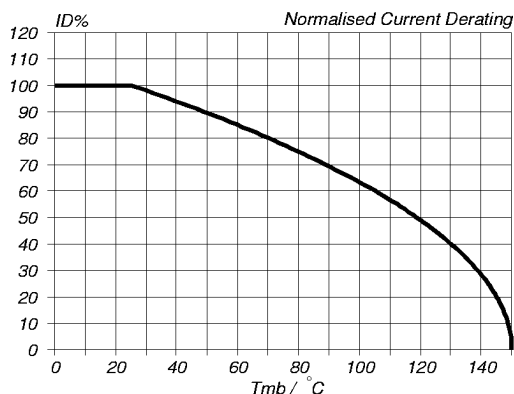


Fig.3. Normalised continuous drain current.  
 $I_D\% = 100 \cdot I_D / I_D(25^\circ\text{C}) = f(T_{mb})$ ; conditions:  $V_{IS} = 5\text{ V}$

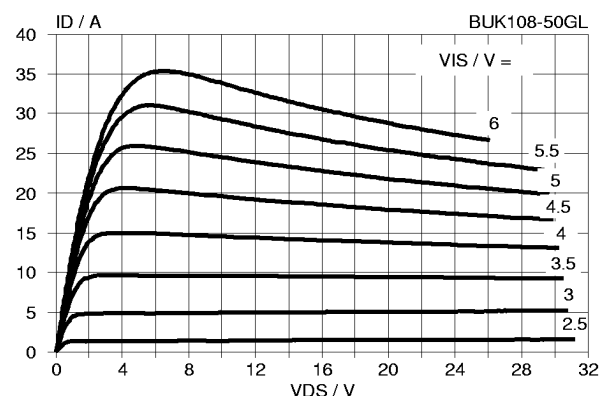


Fig.6. Typical output characteristics,  $T_j = 25^\circ\text{C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{IS}$ ;  $t_p = 250\ \mu\text{s}$  &  $t_p < t_{dsc}$

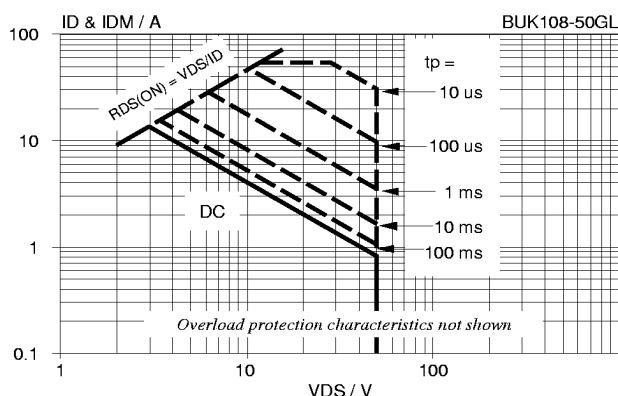


Fig.4. Safe operating area.  $T_{mb} = 25^\circ\text{C}$   
 $I_D$  &  $I_{DM} = f(V_{DS})$ ;  $I_{DM}$  single pulse; parameter  $t_p$

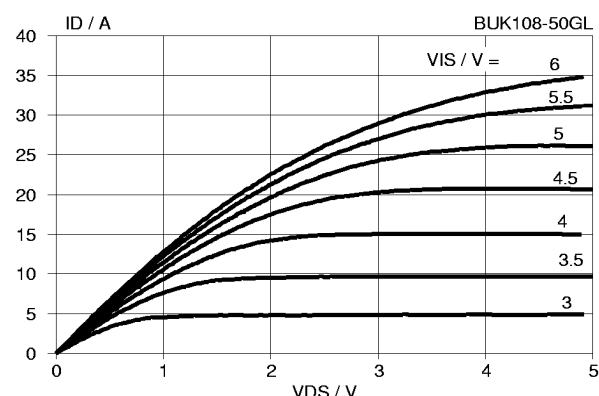
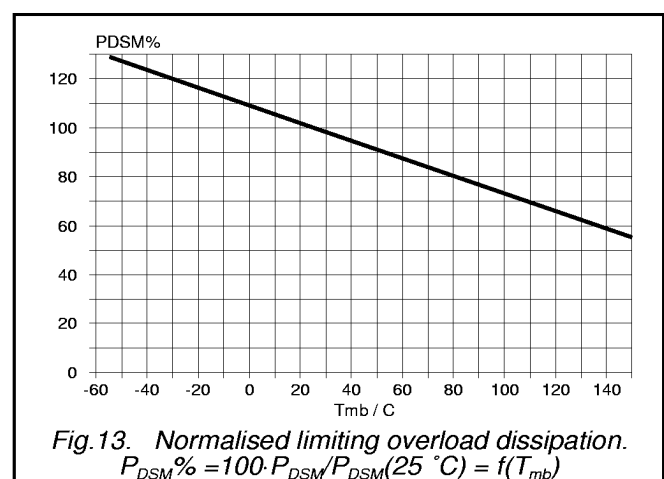
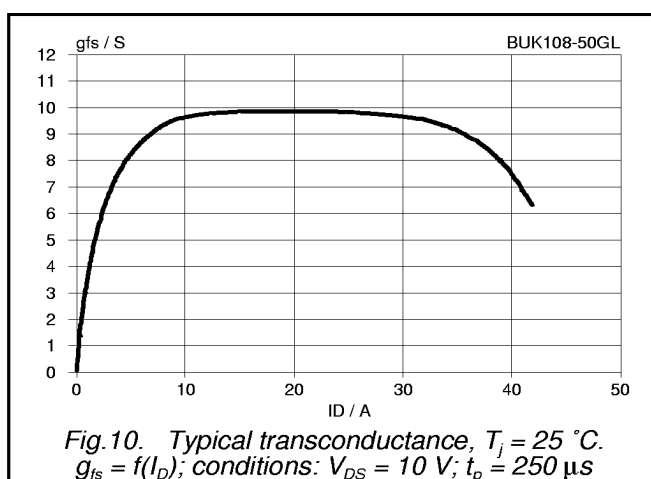
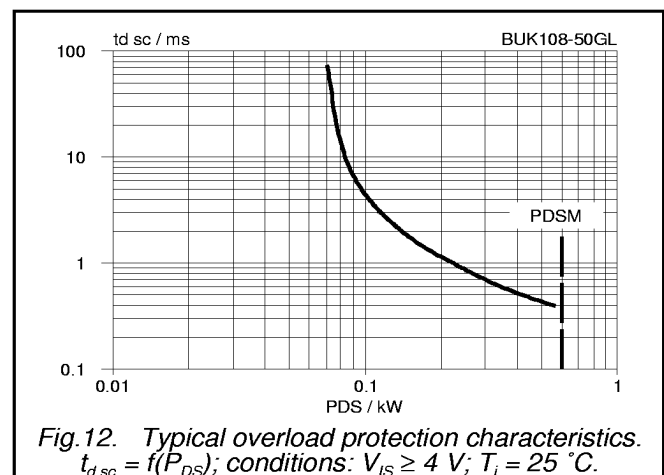
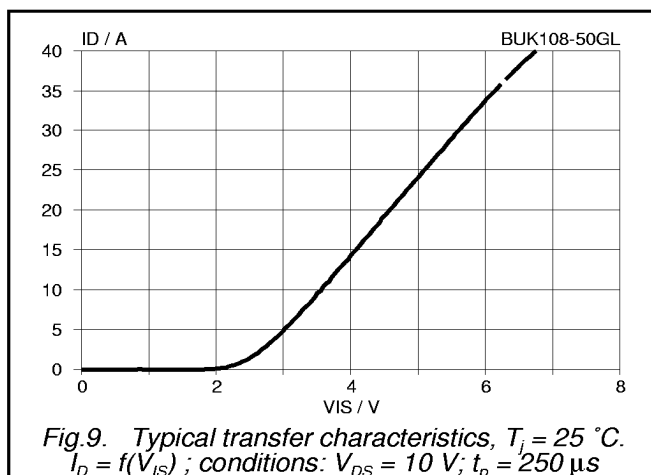
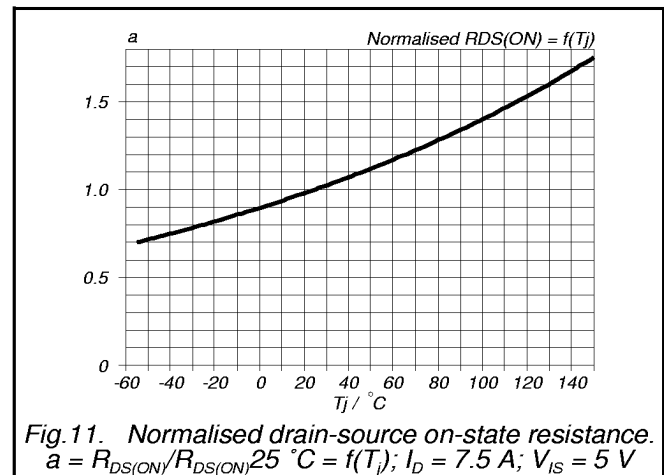
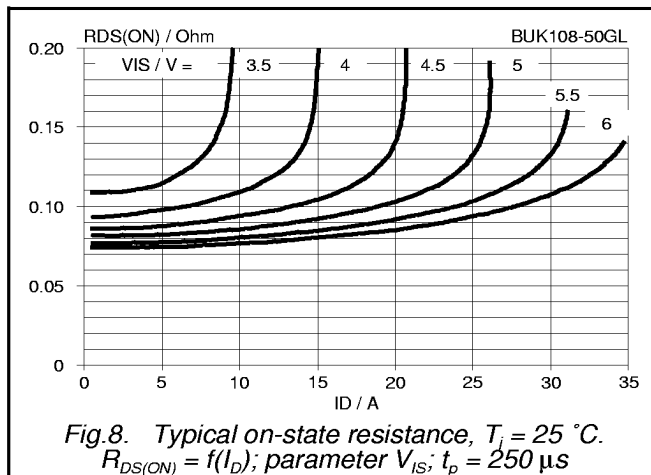


Fig.7. Typical on-state characteristics,  $T_j = 25^\circ\text{C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{IS}$ ;  $t_p = 250\ \mu\text{s}$

# PowerMOS transistor

## Logic level TOPFET

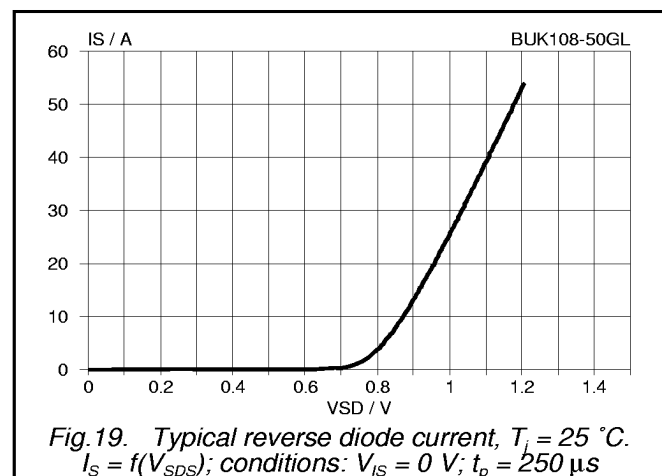
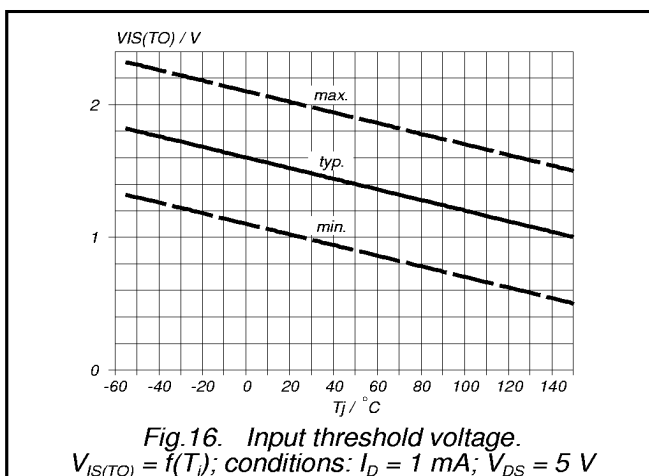
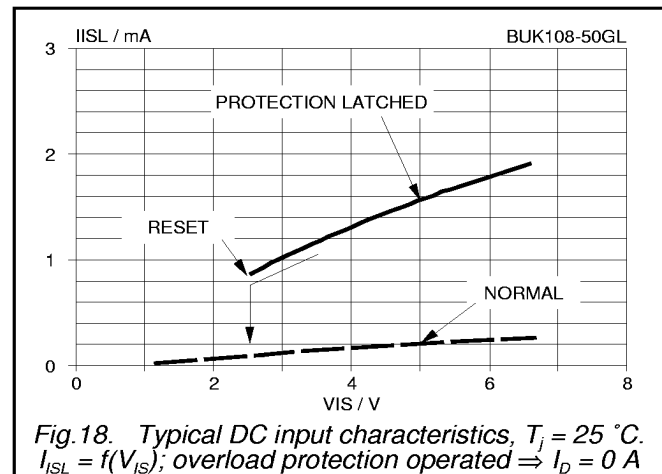
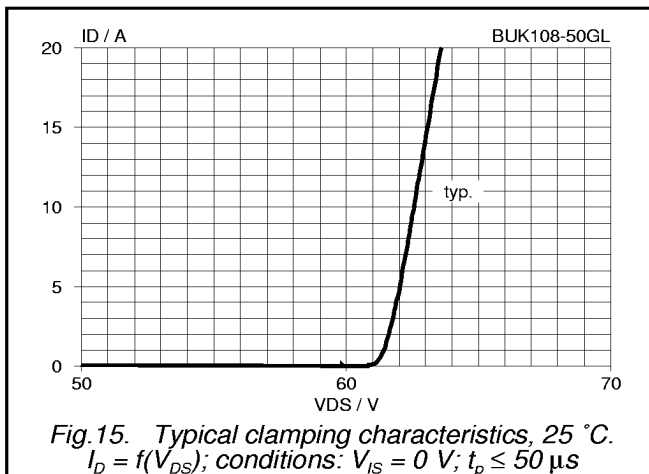
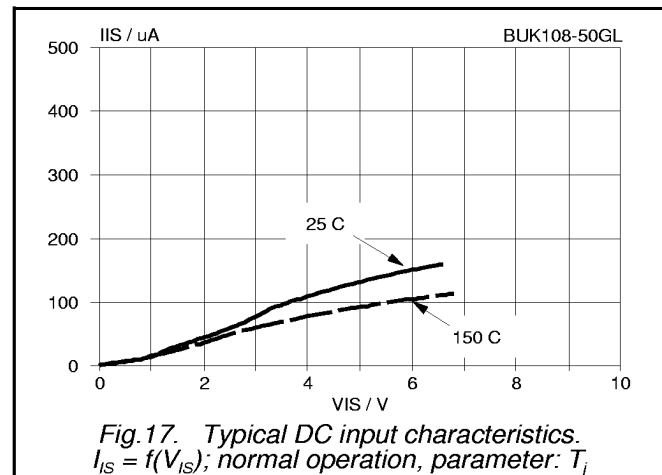
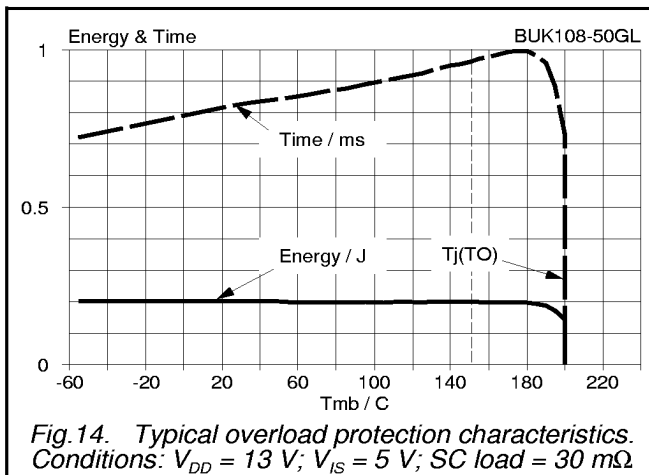
# BUK108-50GL



# PowerMOS transistor

## Logic level TOPFET

# BUK108-50GL



# PowerMOS transistor

## Logic level TOPFET

# BUK108-50GL

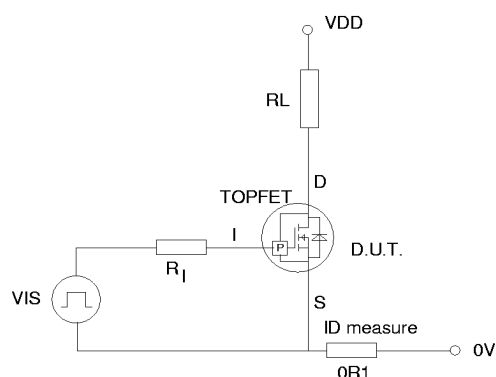


Fig.20. Test circuit for resistive load switching times.

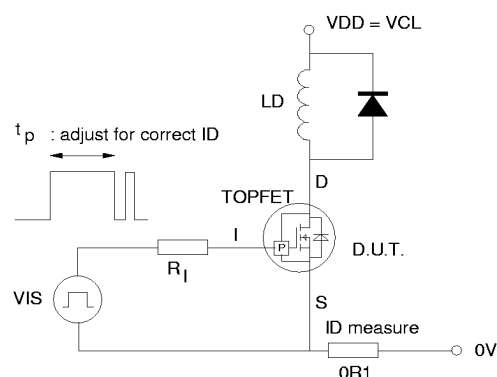


Fig.23. Test circuit for inductive load switching times.

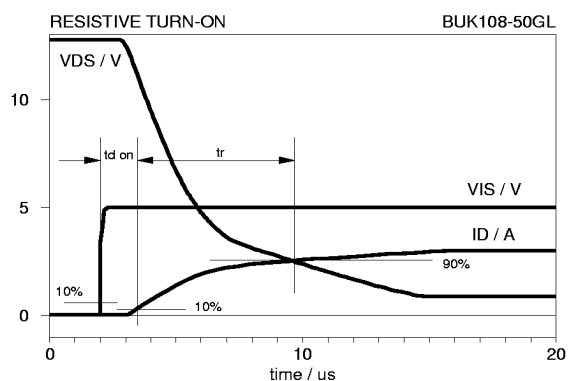


Fig.21. Typical switching waveforms, resistive load.  
 $V_{DD} = 13\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $R_i = 50\ \Omega$ ;  $T_j = 25\ ^\circ\text{C}$ .

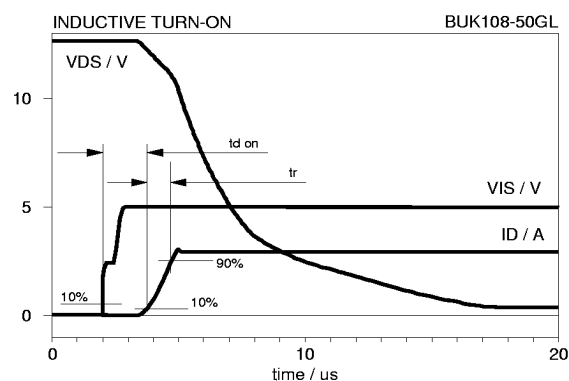


Fig.24. Typical switching waveforms, inductive load.  
 $V_{DD} = 13\text{ V}$ ;  $I_D = 3\text{ A}$ ;  $R_i = 50\ \Omega$ ;  $T_j = 25\ ^\circ\text{C}$ .

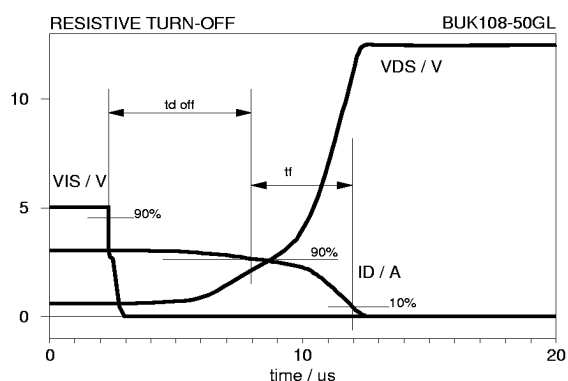


Fig.22. Typical switching waveforms, resistive load.  
 $V_{DD} = 13\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $R_i = 50\ \Omega$ ;  $T_j = 25\ ^\circ\text{C}$ .

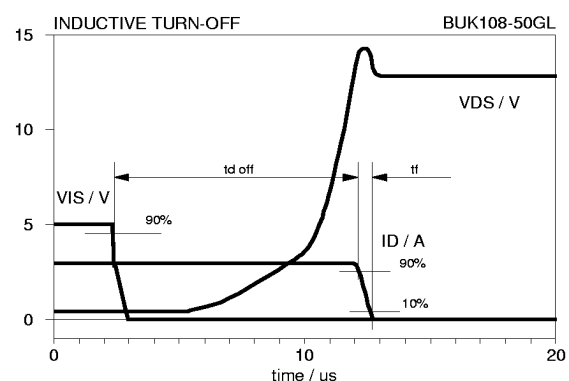


Fig.25. Typical switching waveforms, inductive load.  
 $V_{DD} = 13\text{ V}$ ;  $I_D = 3\text{ A}$ ;  $R_i = 50\ \Omega$ ;  $T_j = 25\ ^\circ\text{C}$ .

# PowerMOS transistor Logic level TOPFET

## BUK108-50GL

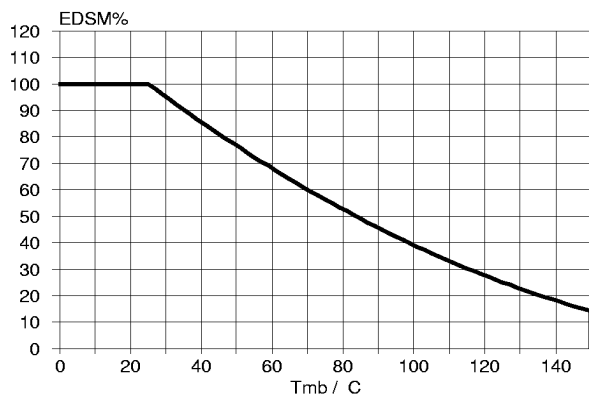


Fig.26. Normalised limiting clamping energy.  
 $E_{DSM}\% = f(T_{mb})$ ; conditions:  $I_D = 15\text{ A}$ ;  $V_{IS} = 5\text{ V}$

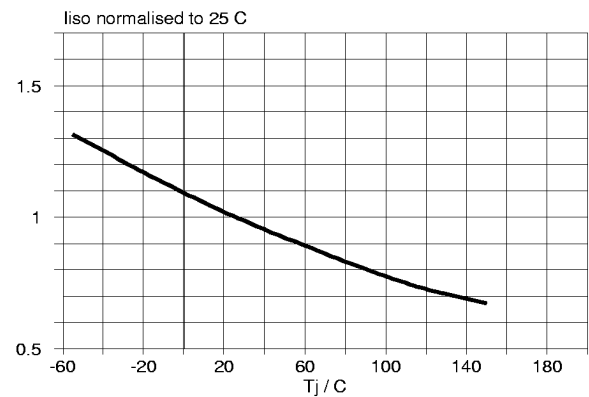


Fig.29. Normalised input current (normal operation).  
 $I_{IS}/I_{IS25^\circ\text{C}} = f(T_J)$ ;  $V_{IS} = 5\text{ V}$

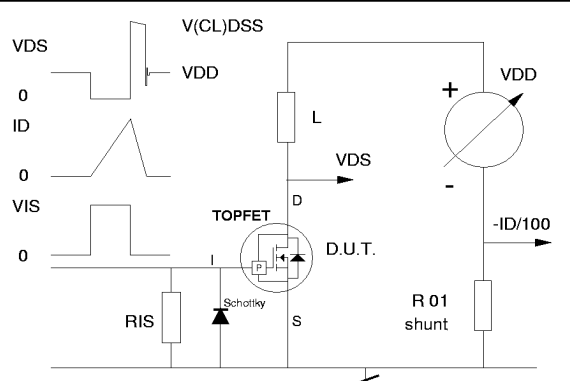


Fig.27. Clamping energy test circuit,  $R_{IS} = 50\ \Omega$ .  
 $E_{DSM} = 0.5 \cdot L I_D^2 \cdot V_{(CL)DSS} / (V_{(CL)DSS} - V_{DD})$

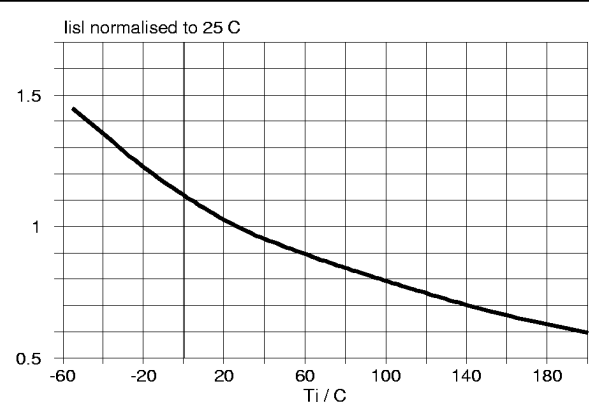


Fig.30. Normalised input current (protection latched).  
 $I_{ISL}/I_{ISL25^\circ\text{C}} = f(T_J)$ ;  $V_{IS} = 5\text{ V}$

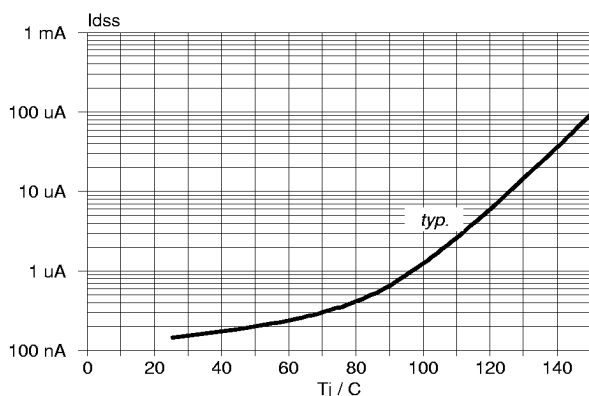


Fig.28. Typical off-state leakage current.  
 $I_{DSS} = f(T_J)$ ; Conditions:  $V_{DS} = 40\text{ V}$ ;  $I_{IS} = 0\text{ V}$ .

# PowerMOS transistor Logic level TOPFET

BUK108-50GL

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

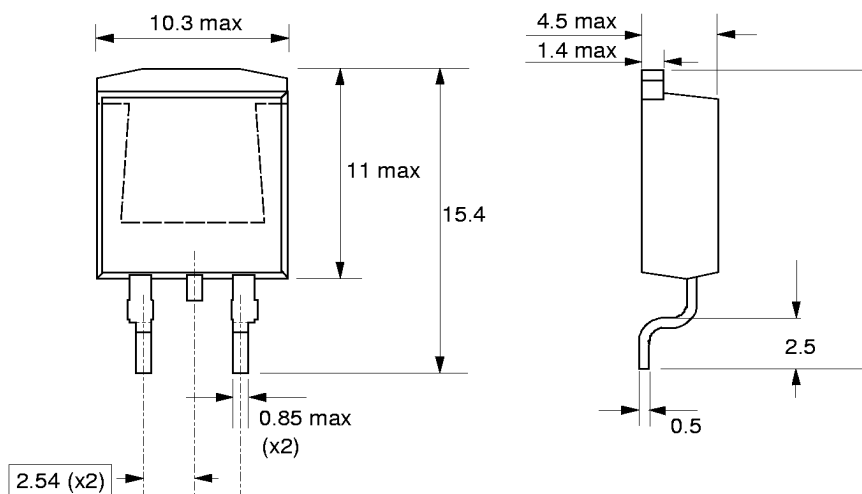


Fig.31. SOT404 : centre pin connected to mounting base.

### Notes

1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

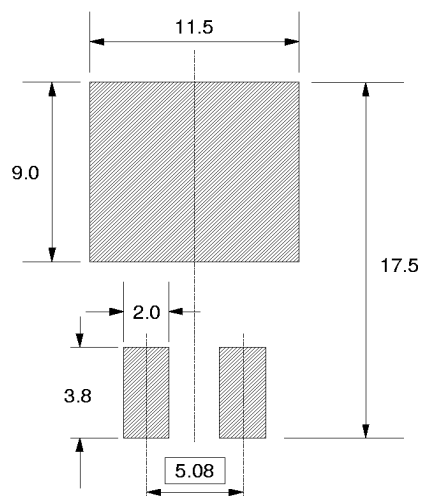


Fig.32. SOT404 : minimum pad sizes for surface mounting.

### Notes

1. Plastic meets UL94 V0 at 1/8".