

PowerMOS transistor

Logic level TOPFET

BUK109-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving

- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	26	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	60	$m\Omega$
I_{ISL}	Input supply current $V_{IS} = 5$ V	650	μA

FUNCTIONAL BLOCK DIAGRAM

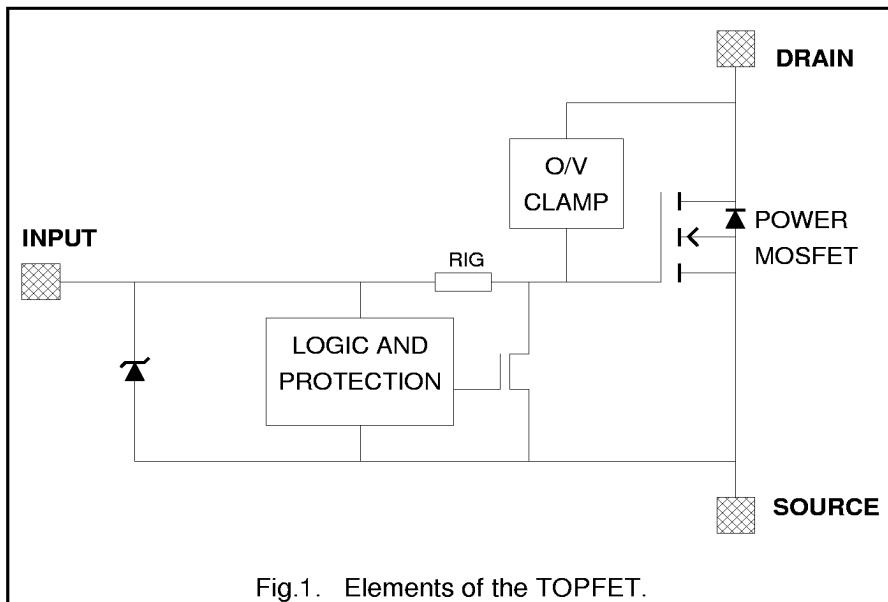
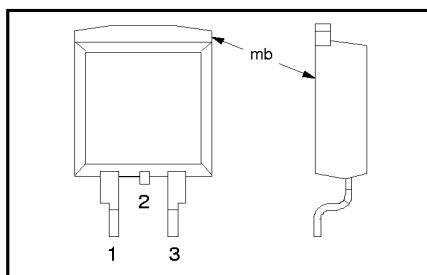


Fig.1. Elements of the TOPFET.

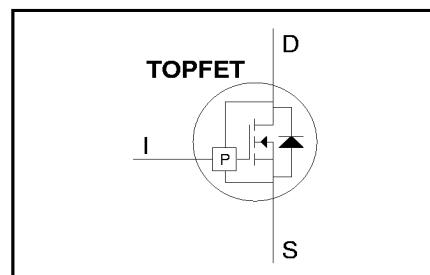
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage ¹	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25^\circ\text{C}; V_{IS} = 5\text{ V}$	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100^\circ\text{C}; V_{IS} = 5\text{ V}$	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25^\circ\text{C}; V_{IS} = 5\text{ V}$	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25^\circ\text{C}$	-	75	W
T_{stg}	Storage temperature	-	-55	150	$^\circ\text{C}$
T_j	Continuous junction temperature ²	normal operation	-	150	$^\circ\text{C}$
T_{sold}	Lead temperature	during soldering	-	250	$^\circ\text{C}$

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage ³	for valid protection	4	-	V
$V_{DDP(T)}$	Over temperature protection				
	Protected drain source supply voltage	$V_{IS} = 5\text{ V}$	-	50	V
$V_{DDP(P)}$	Short circuit load protection ⁴				
	Protected drain source supply voltage ⁵	$V_{IS} = 5\text{ V}$	-	20	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25^\circ\text{C}$	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0\text{ V}$	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25^\circ\text{C}; I_{DM} = 26\text{ A}; V_{DD} \leq 20\text{ V};$ inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95^\circ\text{C}; I_{DM} = 8\text{ A}; V_{DD} \leq 20\text{ V}; f = 250\text{ Hz}$	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; $C = 250\text{ pF}; R = 1.5\text{ k}\Omega$	-	2	kV

¹ Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

² A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

³ The input voltage for which the overload protection circuits are functional.

⁴ For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

⁵ The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM} , which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j-a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 23)	-	50	-	K/W

STATIC CHARACTERISTICS $T_{mb} = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0 V; I_D = 10 \text{ mA}$	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0 V; I_{DM} = 2 A; t_p \leq 300 \mu s; \delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12 V; V_{IS} = 0 V$	-	0.5	10	μA
I_{DSS}	Zero input voltage drain current	$V_{DS} = 50 V; V_{IS} = 0 V$	-	1	20	μA
I_{DSS}	Zero input voltage drain current	$V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125^\circ C$	-	10	100	μA
$R_{DS(ON)}$	Drain-source on-state resistance ¹	$V_{IS} = 5 V; I_{DM} = 13 A; t_p \leq 300 \mu s; \delta \leq 0.01$	-	45	60	$m\Omega$

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$E_{DS(TO)}$	Short circuit load protection² Overload threshold energy	$T_{mb} = 25^\circ C; L \leq 10 \mu H; R_L = 10 m\Omega$	-	0.4	-	J
$t_{d\ sc}$	Response time	$V_{DD} = 13 V; V_{IS} = 5 V$	-	0.8	-	ms
$I_{D(SC)}$	Drain current ³	$V_{DD} = 13 V; V_{IS} = 5 V$	-	45	-	A
$I_{DM(SC)}$	Peak drain current ⁴	$V_{IS} = 5 V; V_{DD} = 13 V$	-	105	-	A
$T_{j(TO)}$	Over temperature protection Threshold junction temperature	$V_{IS} = 5 V; \text{from } I_D \geq 1 A^5$	150	-	-	°C

TRANSFER CHARACTERISTIC $T_{mb} = 25^\circ C$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10 V; I_{DM} = 13 A; t_p \leq 300 \mu s; \delta \leq 0.01$	10	16	-	S

¹ Continuous input voltage. The specified pulse width is for the drain current.² Refer to OVERLOAD PROTECTION LIMITING VALUES.³ Continuous drain-source supply voltage. Pulsed input voltage.⁴ Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).⁵ The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

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INPUT CHARACTERISTICS $T_{mb} = 25^\circ\text{C}$ unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$ I_{IS}	Input threshold voltage Input supply current	$V_{DS} = 5 \text{ V}$; $I_D = 1 \text{ mA}$ normal operation; $V_{IS} = 5 \text{ V}$ $V_{IS} = 4 \text{ V}$ $T_j = 25^\circ\text{C}$ $T_j = 150^\circ\text{C}$	1.0 100 - 2.0 1.0	1.5 200 160 2.6 -	2.0 350 270 3.5 -	V μA μA V
V_{ISR}	Protection reset voltage ¹					
I_{ISL}	Input supply current	protection latched; $V_{IS} = 5 \text{ V}$ $V_{IS} = 3.5 \text{ V}$	- -	330 240	650 430	μA μA
$V_{(BR)IS}$ R_{IG}	Input breakdown voltage Input series resistance to gate of power MOSFET	$I_I = 10 \text{ mA}$ $T_j = 25^\circ\text{C}$ $T_j = 150^\circ\text{C}$	6 -	- 33 50	- -	V k Ω k Ω

SWITCHING CHARACTERISTICS $T_{mb} = 25^\circ\text{C}$. $R_L = 50 \Omega$. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 13 \text{ V}$; $V_{IS} = 5 \text{ V}$ resistive load $R_L = 2.1 \Omega$	-	17	-	μs
t_r	Rise time		-	75	-	μs
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 13 \text{ V}$; $V_{IS} = 0 \text{ V}$ resistive load $R_L = 2.1 \Omega$	-	60	-	μs
t_f	Fall time		-	70	-	μs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_s	Continuous forward current	$T_{mb} \leq 25^\circ\text{C}$; $V_{IS} = 0 \text{ V}$	-	26	A

REVERSE DIODE CHARACTERISTICS $T_{mb} = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SD0}	Forward voltage	$I_s = 26 \text{ A}$; $V_{IS} = 0 \text{ V}$; $t_p = 300 \mu\text{s}$ not applicable ²	-	1.0	1.5	V
t_{rr}	Reverse recovery time		-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

¹ The input voltage below which the overload protection circuits will be reset.² The reverse diode of this type is not intended for applications requiring fast reverse recovery.

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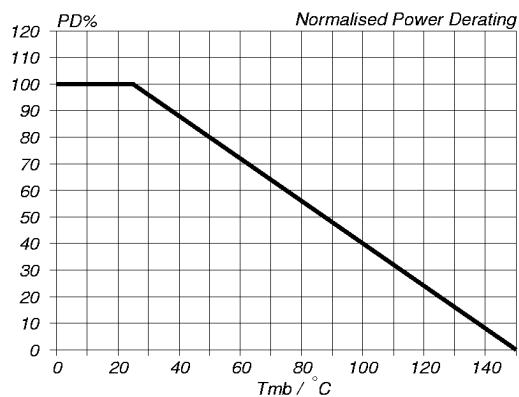


Fig.2. Normalised power dissipation.
 $P_D\% = 100 \cdot P_D/P_D(25^\circ\text{C}) = f(T_{mb})$

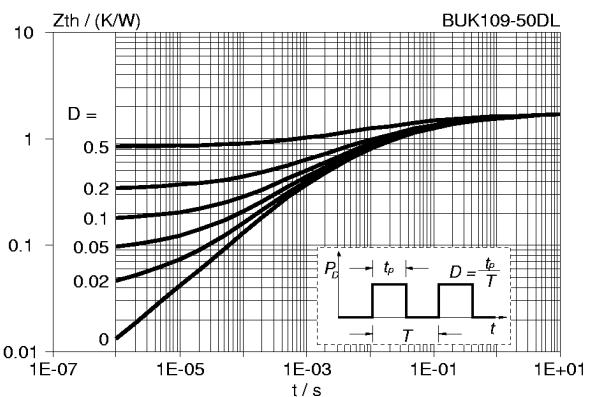


Fig.5. Transient thermal impedance.
 $Z_{th,j-mb} = f(t)$; parameter $D = t_p/T$

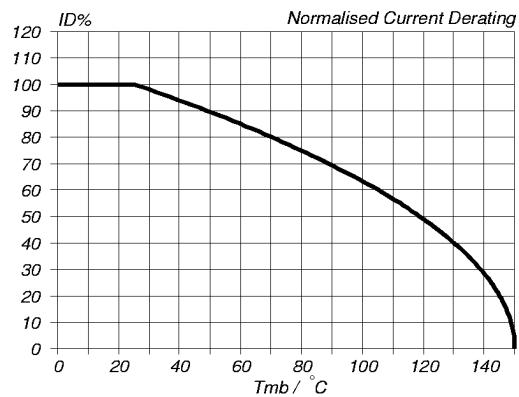


Fig.3. Normalised continuous drain current.
 $I_D\% = 100 \cdot I_D/I_D(25^\circ\text{C}) = f(T_{mb})$; conditions: $V_{IS} = 5\text{ V}$

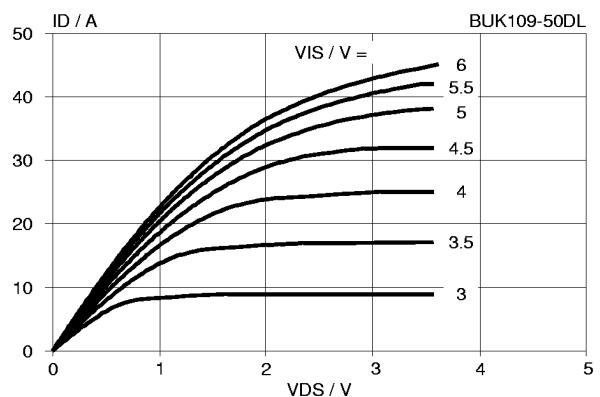


Fig.6. Typical on-state characteristics, $T_j = 25^\circ\text{C}$.
 $ID = f(V_{DS})$; parameter V_{IS} ; $t_p = 2\text{ ms}$

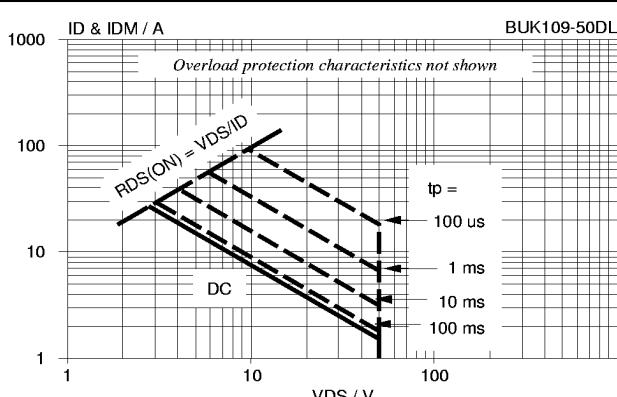


Fig.4. Safe operating area. $T_{mb} = 25^\circ\text{C}$
 I_D & I_{DM} = $f(V_{DS})$; I_{DM} single pulse; parameter t_p

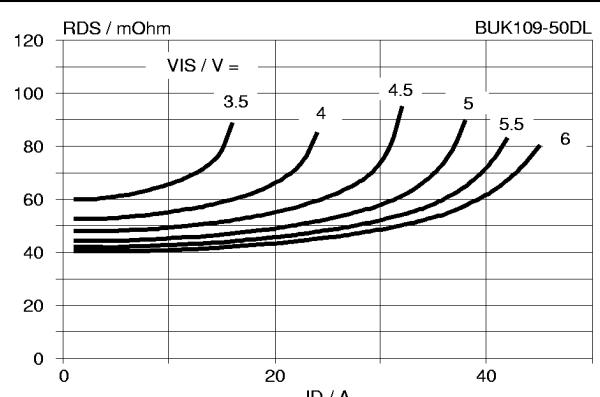


Fig.7. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{IS} ; $t_p = 2\text{ ms}$

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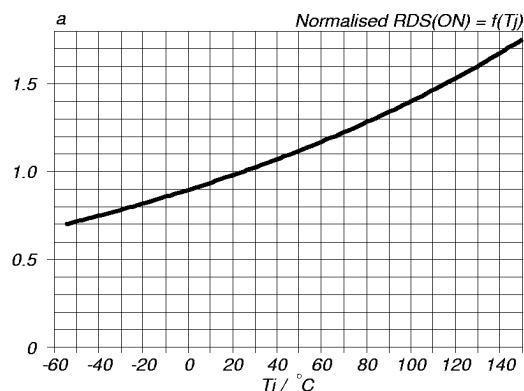


Fig.8. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)}|_{25\text{ }^{\circ}\text{C}} = f(T_j)$; $I_D = 13\text{ A}$; $V_{IS} = 5\text{ V}$

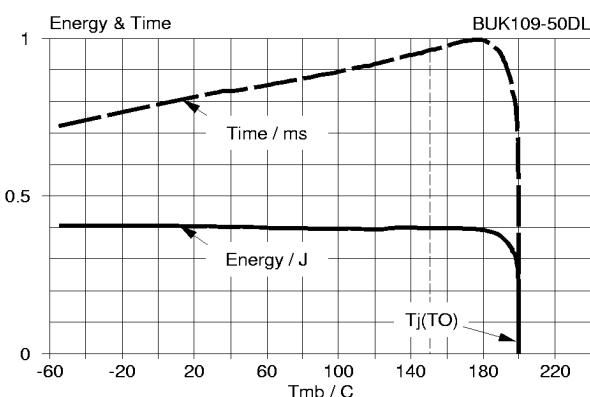


Fig.11. Typical overload protection characteristics.
 Conditions: $V_{DD} = 13\text{ V}$; $V_{IS} = 5\text{ V}$; SC load = $30\text{ m}\Omega$

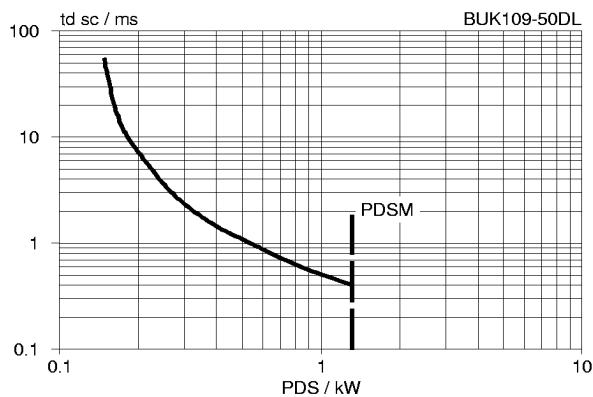


Fig.9. Typical overload protection characteristics.
 $t_{d,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.

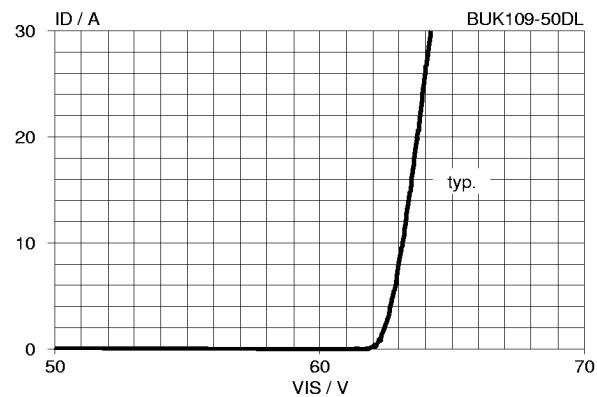


Fig.12. Typical clamping characteristics, $25\text{ }^{\circ}\text{C}$.
 $I_D = f(V_{DS})$; conditions: $V_{IS} = 0\text{ V}$; $t_p \leq 50\text{ }\mu\text{s}$

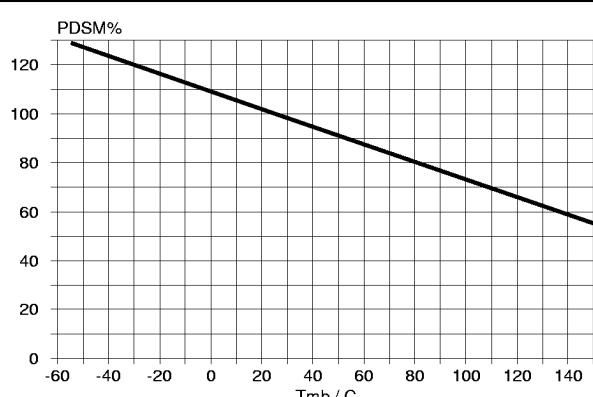


Fig.10. Normalised limiting overload dissipation.
 $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\text{ }^{\circ}\text{C}) = f(T_{mb})$

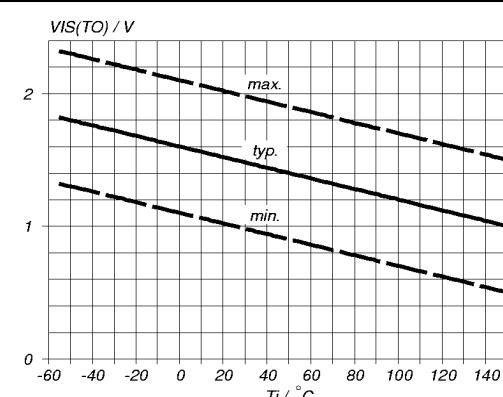


Fig.13. Input threshold voltage.
 $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = 5\text{ V}$

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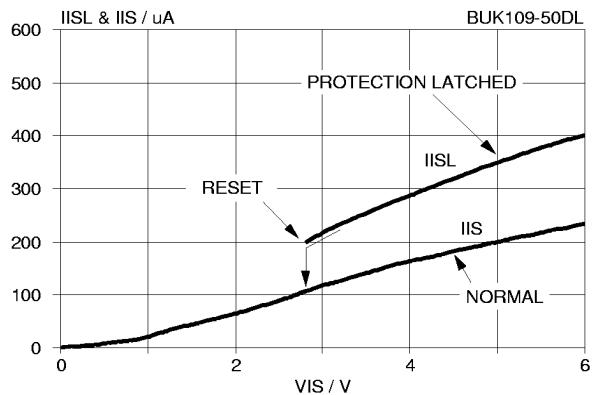


Fig. 14. Typical DC input characteristics, $T_j = 25^\circ\text{C}$.
 $I_{ISL} \& I_{IS} = f(V_{IS})$; protection latched & normal operation

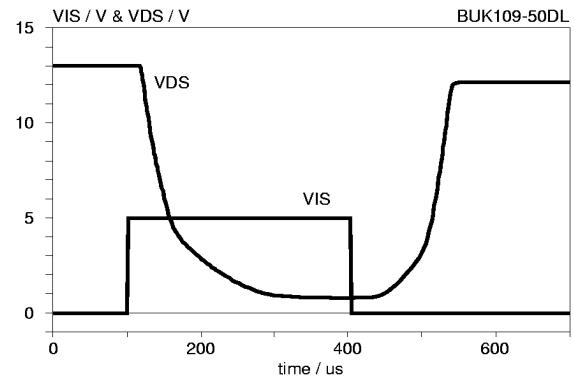


Fig. 17. Typical switching waveforms, resistive load.
 $V_{DD} = 13\text{ V}$; $R_L = 2.1\Omega$; $R_I = 50\Omega$, $T_j = 25^\circ\text{C}$.

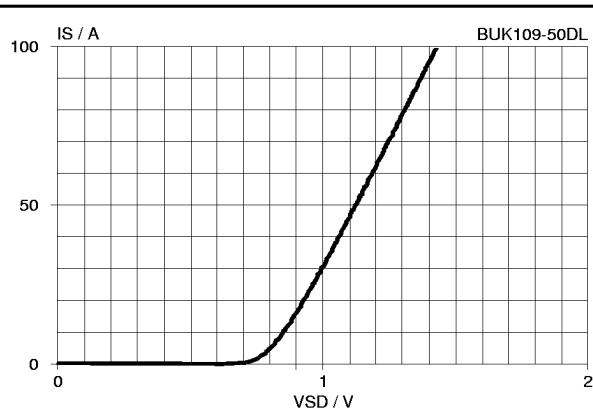


Fig. 15. Typical reverse diode current, $T_j = 25^\circ\text{C}$.
 $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0\text{ V}$

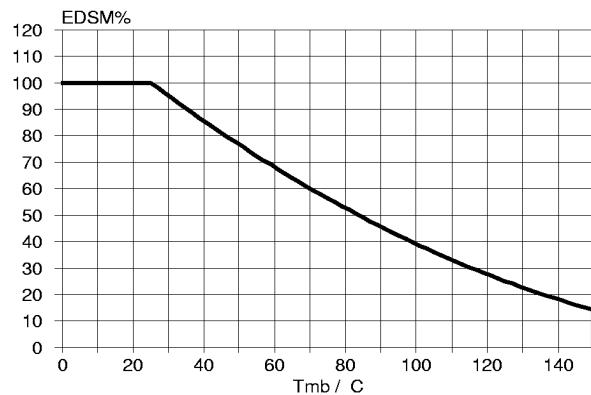


Fig. 18. Normalised clamping energy rating.
 $E_{DSM}\% = f(T_{mb})$; conditions: $I_D = 26\text{ A}$; $V_{IS} = 5\text{ V}$

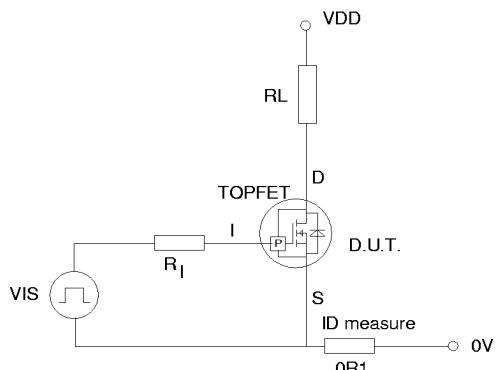


Fig. 16. Test circuit for resistive load switching times.

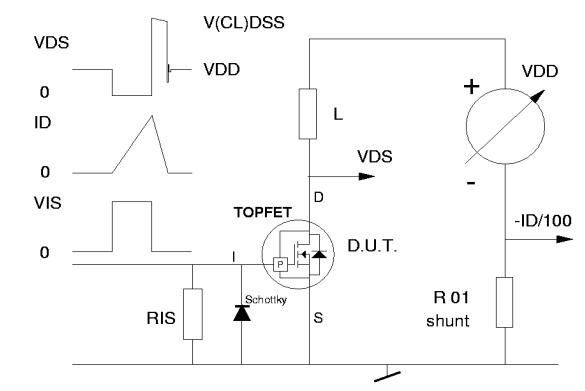


Fig. 19. Clamping energy test circuit, $R_{IS} = 50\Omega$.
 $E_{DSM} = 0.5 \cdot L I_D^2 \cdot V_{(CL)DSS} / (V_{(CL)DSS} - V_{DD})$

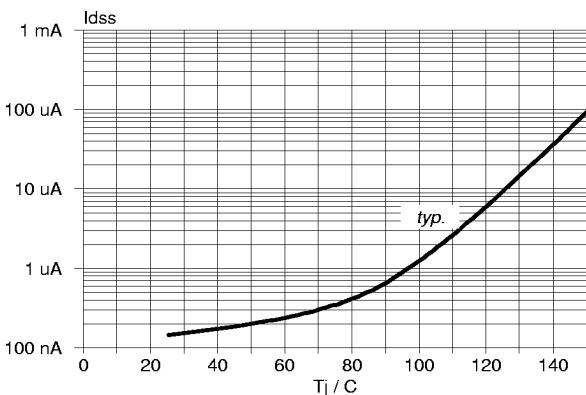
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Fig.20. Typical off-state leakage current.
 $I_{DSS} = f(T_J)$; Conditions: $V_{DS} = 40$ V; $I_{IS} = 0$ V.

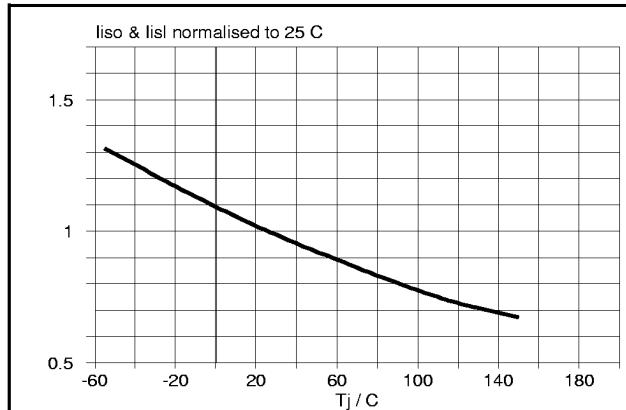


Fig.21. Normalised input currents (normal & latched).
 $I_{ISO}/I_{ISO}25^{\circ}\text{C}$ & $I_{ISL}/I_{ISL}25^{\circ}\text{C} = f(T_J)$; $V_{IS} = 5$ V

**PowerMOS transistor
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BUK109-50DL**MECHANICAL DATA***Dimensions in mm*

Net Mass: 1.4 g

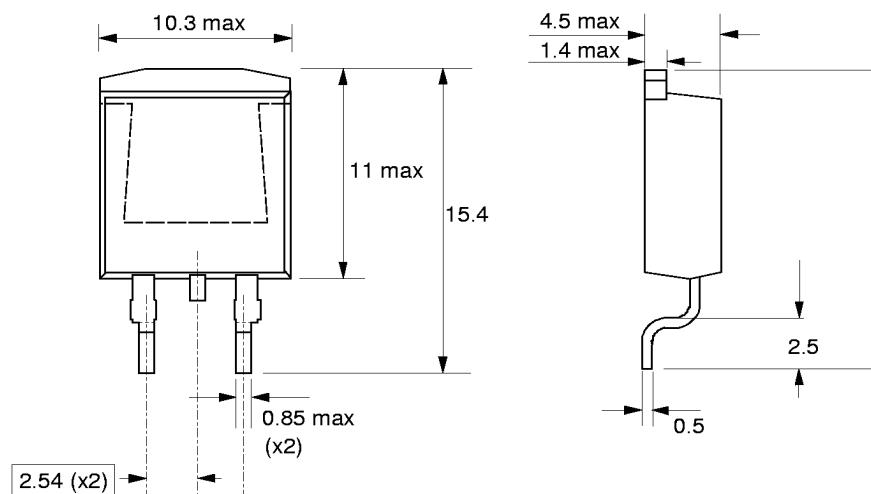


Fig.22. SOT404 : centre pin connected to mounting base.

Notes

1. Epoxy meets UL94 V0 at 1/8".

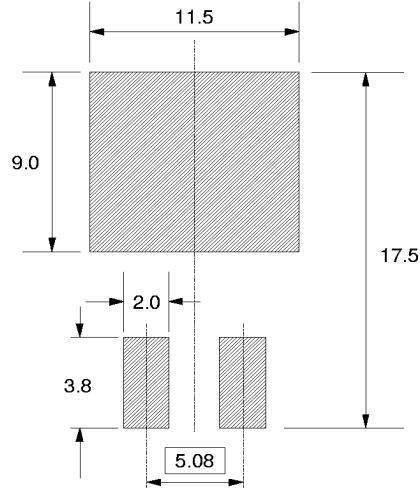
MOUNTING INSTRUCTIONS*Dimensions in mm*

Fig.23. SOT404 : minimum pad sizes for surface mounting.

Notes

1. Plastic meets UL94 V0 at 1/8".