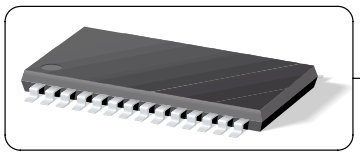


Typical Size
(6,4 mm X 9,7 mm)

SLVS397A – JULY 2001 – REVISED AUGUST 2001

TRACKING/TERMINATION SYNCHRONOUS PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- **Tracks Externally Applied Reference Voltage**
- **30-mΩ, 12-A Peak MOSFET Switches for High Efficiency at 6-A Continuous Output Source or Sink Current**
- **6% to 90% VIN Output Tracking Range**
- **PWM Frequency Range: Fixed 350 kHz or Adjustable 280 to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Component Count**

APPLICATIONS

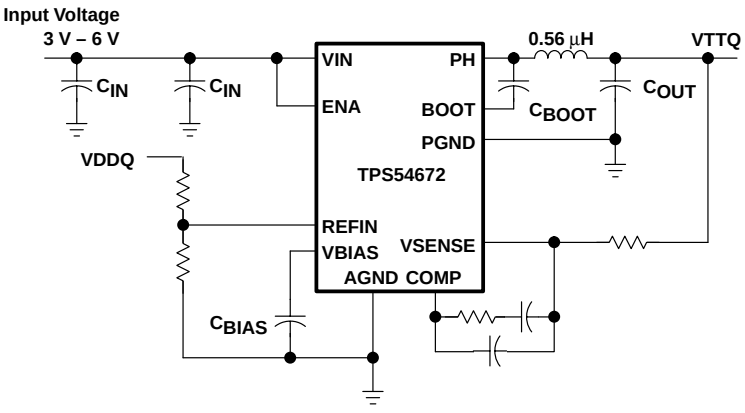
- **DDR Memory Termination Voltage**
- **Active Termination of GTL and STL High-Speed Logic Families**
- **DAC Controlled High Current Output Stage**
- **Precision Point of Load Power Supply**

DESCRIPTION

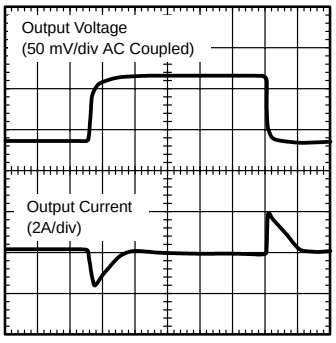
As a member of the SWIFT™ family of dc/dc regulators, the TPS54672 tracking/termination synchronous PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; a slow-start control to limit in-rush currents; and a status output to indicate valid operating conditions.

The TPS54672 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

Typical DDR Memory Termination Regulator Circuit

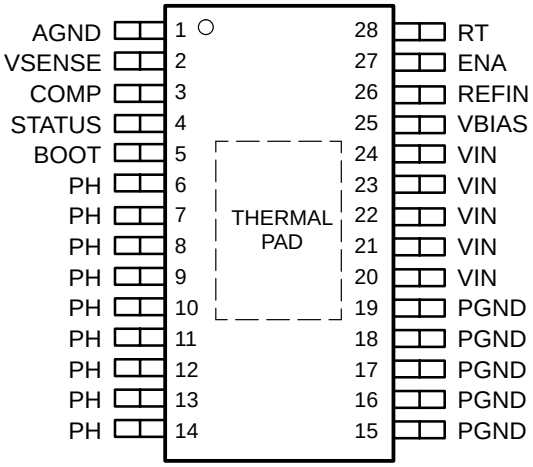


LOAD TRANSIENT RESPONSE



10 µs/div

PWP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE
	PLASTIC HTSSOP (PWP)†
–40°C to 85°C	TPS54672PWP

† The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54672PWPR). See the application section of the data sheet for PowerPAD™ drawing and layout information.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Input voltage range, V_I: VIN, ENA . . . . . –0.3 V to 7 V
RT . . . . . –0.3 V to 6 V
VSENSE, REFIN . . . . . –0.3 V to 4 V
BOOT . . . . . –0.3 V to 17 V
Output voltage range, V_O: VBIAS, COMP, STATUS . . . . . –0.3 V to 7 V
PH . . . . . –0.3 V to 10 V
Source current, I_O: PH . . . . . Internally Limited
COMP, VBIAS . . . . . 6 mA
Sink current, I_S: PH . . . . . 12 A
COMP . . . . . 6 mA
STATUS . . . . . 10 mA
Voltage differential, AGND to PGND . . . . . ±0.6 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 125°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
28 Pin PWP with solder	3.58 W	0.0358 mW/°C	1.96 W	1.43 W
28 Pin PWP without solder	1.78 W	0.0178 mW/°C	0.98 W	0.71 W

† Test Board Conditions:
1. Thickness: 0.062”
2. 3” x 3”
3. 2 oz. Copper traces located on the top and bottom of the PCB for soldering
4. Copper areas located on the top and bottom of the PCB for soldering
5. Power and ground planes, 1 oz. Copper (0.036 mm thick)
6. Thermal vias, 0,33 mm diameter, 1,5 mm pitch (See applications section in this datasheet)
7. Thermal isolation of power plane

For more information on the PWP package, refer to TI technical brief, literature number SLMA002.

ADDITIONAL 6A SWIFT™ DEVICES, (REFER TO SLVS398 AND SLVS400)

DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE
TPS54611	0.9 V	TPS54614	1.8 V	TPS54610	Adjustable
TPS54612	1.2 V	TPS54615	2.5 V		
TPS54613	1.5 V	TPS54616	3.3 V		

electrical characteristics, T_J = –40°C to +125°C, V_I = 3 V to 6 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range, VIN		3.0		6.0	V
V_{ID}	Differential voltage, AGND to PGND		–0.30		0.30	V
$I_{(Q)}$	Quiescent current	Switching freq. = 350 kHz, RT open		10	16	mA
		Switching freq. = 500 kHz, RT = 100 kΩ		16	24	
		Shutdown, SS/ENA = 0 V		1	1.4	
	Start threshold voltage, UVLO			2.95	3.00	V
	Stop threshold voltage, UVLO		2.70	2.80		V
	Hysteresis voltage, UVLO		0.14	0.16		V
	Rising and falling edge deglitch, UVLO	See Note 1		2.5		µs
	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
	Output current, VBIAS	See Note 2			100	µA
	Cumulative regulation accuracy (relative to REFIN)	I_O = – 6A to 6A, Switching freq. = 350 kHz, REFIN = 1.25 V (see Note 1)	–1.5%		1.5%	
	Internally set—free running frequency	RT open	280	350	420	kHz
	Externally set—free running frequency range	RT = 68 kΩ to 180 kΩ	280		700	kHz
	Externally set—free running frequency accuracy	RT = 100 kΩ (1% resistor to AGND)	460	500	540	kHz
	Ramp valley			0.75		V
	Ramp amplitude (peak-to-peak)			1		V
	Minimum controllable on time	See Note 1			200	ns
	Maximum duty cycle	See Note 1	90%			
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND (see Note 1)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND (see Note 1)	3	5		MHz

NOTE 1: Ensured by design
2. Static resistive loads only

electrical characteristics, T_J = –40°C to +125°C, V_I = 3 V to 6 V (unless otherwise noted) (continued)

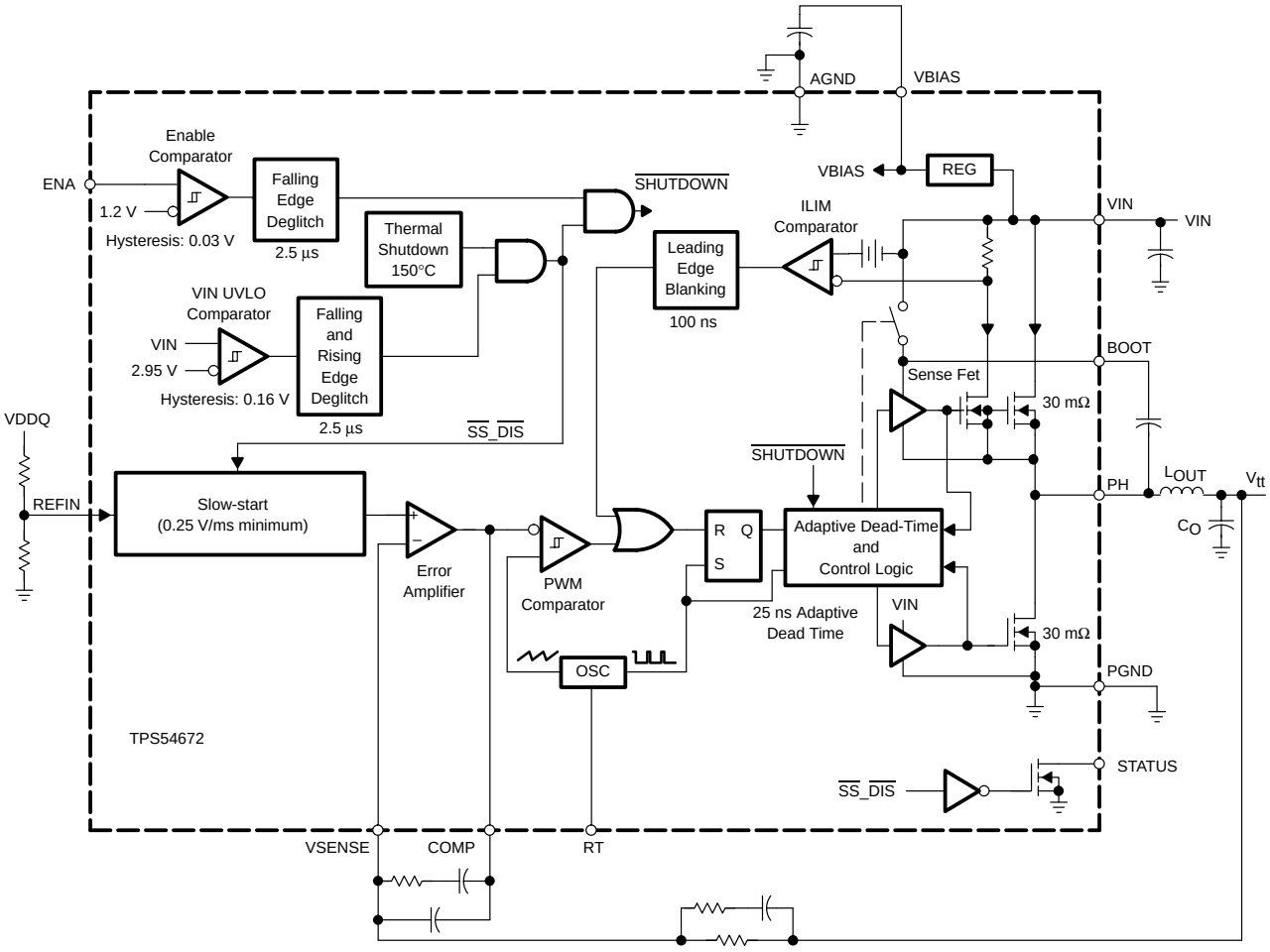
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Error amplifier common mode input voltage range	See Note 1	0		2.85	V
	Error amplifier common mode rejection ratio	See Note 1		65		dB
	Input bias current, VSENSE	VSENSE = REFIN = 1 V		60	250	nA
	Input bias current, REFIN	VSENSE = REFIN = 1.25 V		60	250	nA
	Input offset voltage, REFIN	VSENSE = REFIN = 1.25 V	–1.5		1.5	mV
	Input voltage range, REFIN	See Note 1	0		1.8	V
	Output voltage slew rate (symmetric), COMP		1	1.4		V/µs
	Common mode output voltage range, COMP	I_O = 3 mA			2.65	V
		I_O = –3 mA	0.2			
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive (see Note 1)		70	85	ns
	Enable threshold voltage, ENA		0.95	1.20	1.40	V
	Enable hysteresis voltage, ENA	See Note 1		0.03		V
	Falling edge deglitch, ENA	See Note 1		2.5		µs
	Leakage current, ENA	V_I= 5.5 V			1	µA
	Output saturation voltage, STATUS	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, STATUS	V_I = 5.5 V			1	µA
	Current limit trip point	VIN = 3 V, (see Note 1)	7	10		A
		VIN = 6 V, (see Note 1)	10	12		
	Current limit leading edge blanking time			100		ns
	Current limit total response time			200		ns
	Thermal shutdown trip point	See Note 1	135	150	165	°C
	Thermal shutdown hysteresis	See Note 1		10		°C
$r_{DS(on)}$	Low/high-side N-MOSFET	I_O = 6A, V_I = 6 V (see Note 3)		26	47	mΩ
		I_O = 6A, V_I = 3 V (see Note 3)		36	65	

NOTES: 1: Ensured by design
2. Static resistive loads only
3. Matched MOSFETs, low side $r_{DS(on)}$ production tested, high side $r_{DS(on)}$ ensured by design

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and SYNC pin. Connect PowerPAD to AGND.
BOOT	5	Bootstrap output. 0.022 μF to 0.1 μF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
ENA	27	Enable input. Logic high enables oscillator, PWM control and MOSFET driver circuits. Logic low disables operation and places device in low quiescent current state.
PGND	15–19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6–14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
REFIN	26	External reference input. High impedance input to slow-start and error amplifier circuits.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency. When using the SYNC pin, set the RT value for a frequency at or slightly lower than the external oscillator frequency.
STATUS	4	Open drain output. Asserted low when VIN < UVLO threshold, VBIAS and internal reference are not settled or thermal shutdown active. Otherwise STATUS is high.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-μF to 1.0-μF ceramic capacitor.
VIN	20–24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high-quality, low-ESR 10-μF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage through compensation network/output divider.

internal block diagram



detailed description

under voltage lock out (UVLO)

The TPS54672 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Note that hysteresis in the UVLO comparator and a 2.5-μs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

enable (ENA)

The enable pin, ENA, provides a digital control to enable or disable (shutdown) the TPS54672. An input voltage of 1.4 V or greater ensures that the TPS54672 is enabled. An input of 0.9 V or less ensures that device operation is disabled. These are not standard logic thresholds, even though they are compatible with TTL outputs.

When ENA is low, the oscillator, slow-start, PWM control and MOSFET drivers are disabled and held in an initial state ready for device start-up. On an ENA transition from low to high, device start-up begins with the output starting from 0 V.

slow-start

The slow-start circuit provides start-up slope control of the output voltage to limit in-rush currents. The nominal internal slow-start rate is 0.25 V/ms with the maximum rate being 0.35 V/ms. When the voltage on REFIN rises faster than the internal slope or is present when device operation is enabled, the output rises at the internal rate. If the reference voltage on REFIN rises more slowly, then the output rises at about the same rate as REFIN.

VBIAS regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and that loads with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

oscillator frequency (RT)

The oscillator frequency can be set to an internally fixed value of 350 kHz by leaving the RT pin unconnected (floating). If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 700 kHz by connecting a resistor to the RT pin to ground. The operating frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ \text{[kHz]} \quad (1)$$

The following table summarizes the frequency selection configurations:

FREE RUNNING FREQUENCY	RT PIN
350 kHz, internally set	Float
Externally set 280 kHz to 700 kHz	R = 68 k to 180 k

detailed description (continued)

error amplifier (REFIN, VSENSE, COMP)

The high performance voltage error amplifier, with wide 5MHz bandwidth, low 1.5 mV-max offset, 1.4 V/µs slew rate, and ground rail input range differentiates the TPS54672 from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

The REFIN input range includes ground which allows 0% duty cycle during transient conditions. The user should note that steady state regulation accuracy of voltages less than 0.84 V is limited by the minimum controllable ON time.

PWM control

Signals from the error amplifier output, oscillator and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch and portions of the adaptive dead time and control logic block. During steady state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as REFIN. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54672 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET on to decrease the output current. This process is repeated each cycle in which the current limit comparator is tripped.

dead-time control and MOSFET drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V, while the low-side driver does not turn on until the voltage at the junction of the power MOSFETs (PH pin) is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The bootstrap switch is turned on when the low-side FET is on to charge the BOOT capacitor. The low resistance of the bootstrap switch improves drive efficiency and reduces external component count.

detailed description (continued)

overcurrent protection

The cycle by cycle current limiting is achieved using a sense-FET on the high-side MOSFET and differential amplifier with preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of the voltage on the sense-FET exceeding the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of the current limit when the high-side switch is turning on. Current limit detection occurs only when current flows from VIN to PH when current is being sourced to the output filter. Load protection during current sink operation is provided by thermal shutdown.

thermal shutdown

Thermal shutdown turns off the power MOSFETs and disables the control circuits if the junction temperature exceeds the 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C, and starts up under control of the slow-start circuit.

status (STATUS)

The status pin is an open drain output that indicates when internal conditions are sufficient for proper operation. STATUS can be coupled back to a system controller or monitor circuit to indicate that the termination or tracking regulator is ready for start up. STATUS is high impedance when the TPS54672 is operating or ready to be enabled.

STATUS is active low if any of the following occur:

- VIN < UVLO threshold
- VBIAS or internal reference have not settled.
- Thermal shutdown is active.

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

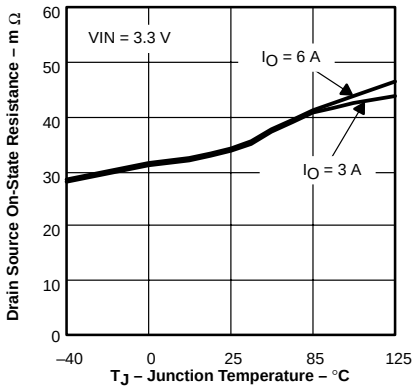


Figure 1

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

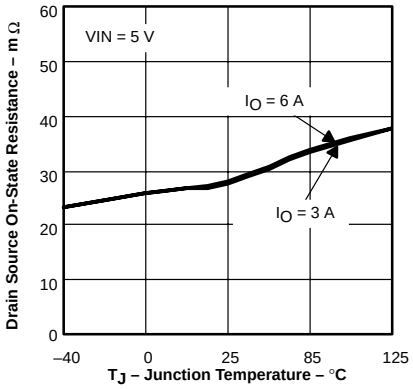


Figure 2

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

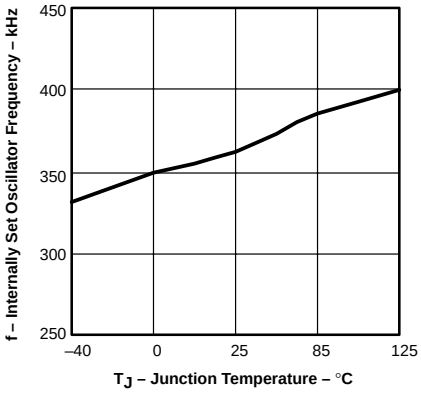


Figure 3

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

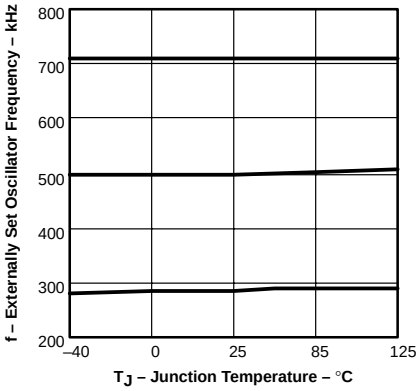


Figure 4

OUTPUT VOLTAGE REGULATION vs OUTPUT CURRENT

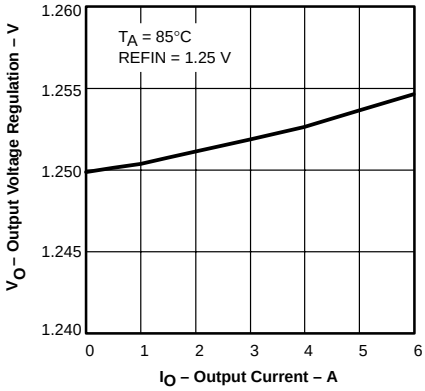


Figure 5

OUTPUT VOLTAGE REGULATION vs INPUT VOLTAGE

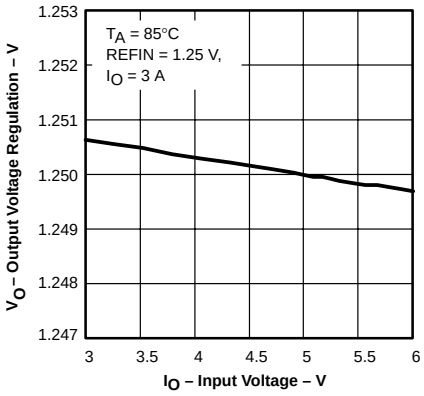


Figure 6

ERROR AMPLIFIER OPEN LOOP RESPONSE

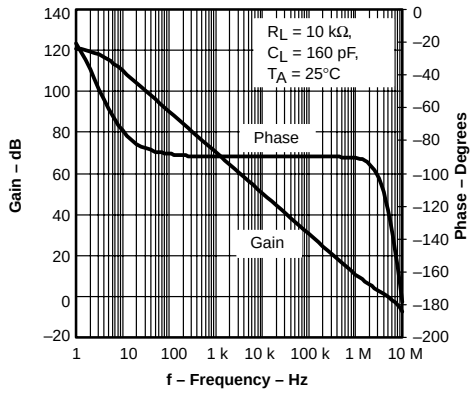


Figure 7

SLOW-START TIME vs JUNCTION TEMPERATURE

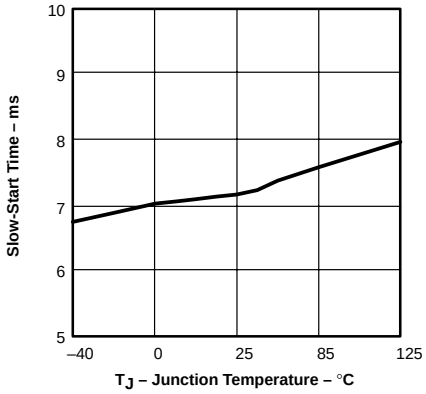


Figure 8

APPLICATION INFORMATION

Figure 9 shows the schematic diagram for a typical DDR memory or GTL bus termination application using the TPS54672. The TPS54672 (U1) can provide greater than 6 A of output current. For proper operation, the exposed thermal PowerPAD underneath the integrated circuit package needs to be soldered to the printed-circuit board.

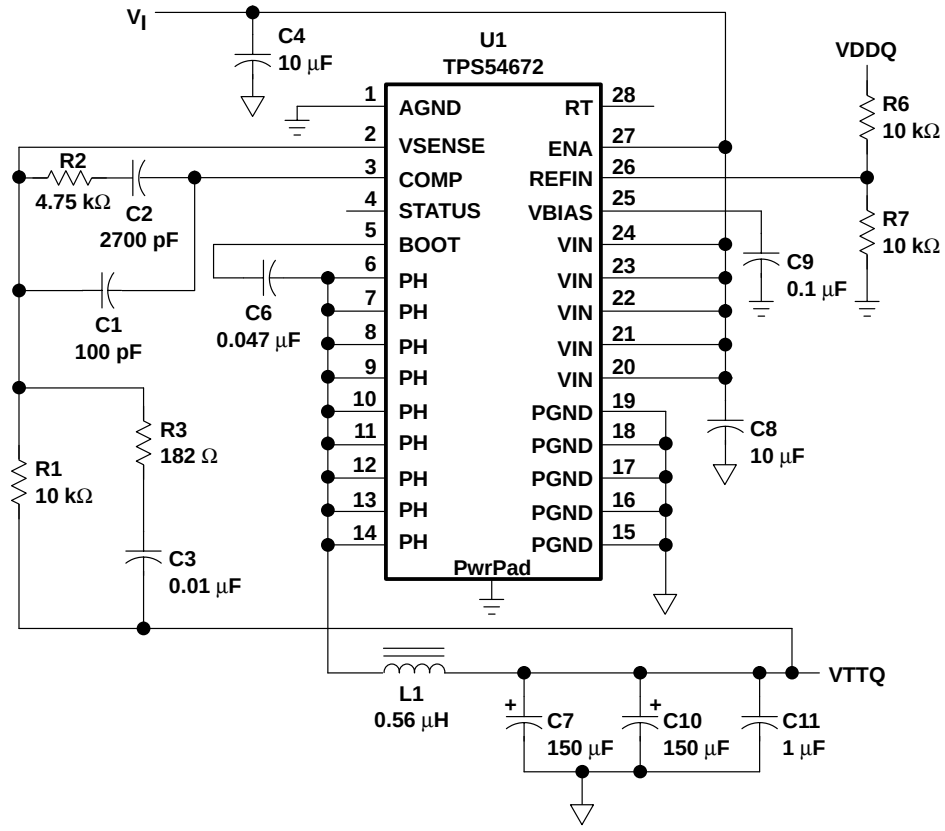


Figure 9. Application Circuit Optimized For Size And Performance

component selection

The values for the components used in this design example were selected for best load transient and tracking response. Additional design information is available at www.ti.com.

input voltage

The input voltage range is 3 to 5.5 VDC. The input filter (C4) is a 10-µF ceramic capacitor (Taiyo Yuden). C8, also a 10-µF ceramic capacitor (Taiyo Yuden) that provides high frequency decoupling of the TPS54672 from the input supply, must be located as close as possible to the device. Ripple current is carried in both C8 and C4, and the return path to PGND should avoid the current circulating in the output capacitors C7 and C10.

feedback circuit

R1, R2, R3, C1, C2 and C3 form the loop compensation network for the circuit. For this design, a Type 3 topology is used. The compensation network, along with the output filter inductor and capacitor delivers a crossover frequency of 135 kHz with 50° of phase margin.

APPLICATION INFORMATION

operating frequency

In the application circuit, RT is grounded through a 71.5-kΩ resistor to select the maximum frequency of 700 kHz. To set a different frequency, place a 68-kΩ to 180-kΩ resistor between RT (pin 28) and analog ground or leave RT floating to select the default 350 kHz. The resistance can be calculated using the following equation:

$$R = \frac{500\ \text{kHz}}{\text{SwitchingFrequency}} \times 100\ [\text{k}\Omega] \quad (2)$$

output filter

The output filter is composed of a 0.56-µH Coilcraft inductor (D01813P–561HC) and two 150-µF Cornell Dublier capacitors (ESRD151M06R). The inductor is a low dc resistance type. The capacitors used are 4 V POSCAP types with a maximum ESR of 0.040 Ω.

grounding

Maintaining proper grounding is important for optimum circuit performance. For this design, separate analog and power grounds, tied together at a *single* point, are used. The power ground is tied to the negative leads of the input and output filter capacitors, as well as the PGND pins (15–19) of the TPS54672. All other ground pins in the circuit are tied to the analog ground including the AGND pin and thermal PowerPAD of the TPS54672. The single connection point for the analog and power grounds can be made near the IC pins, or connection can be made near the negative leads of the output filter capacitor to marginally improve output regulation accuracy. In either case, the input ripple current return path should be strictly avoided. The voltage differential between AGND pins or PowerPAD and the PGND pins should be limited to 300 mV_{PP} to avoid spurious operation. Refer to the layout examples in the user guides for the TPS54672 EVM, TPS54610 EVM (SLVU054) and TPS54614 EVM (SLVU053).

layout considerations for thermal performance

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance should be included in areas not under the device package.

APPLICATION INFORMATION

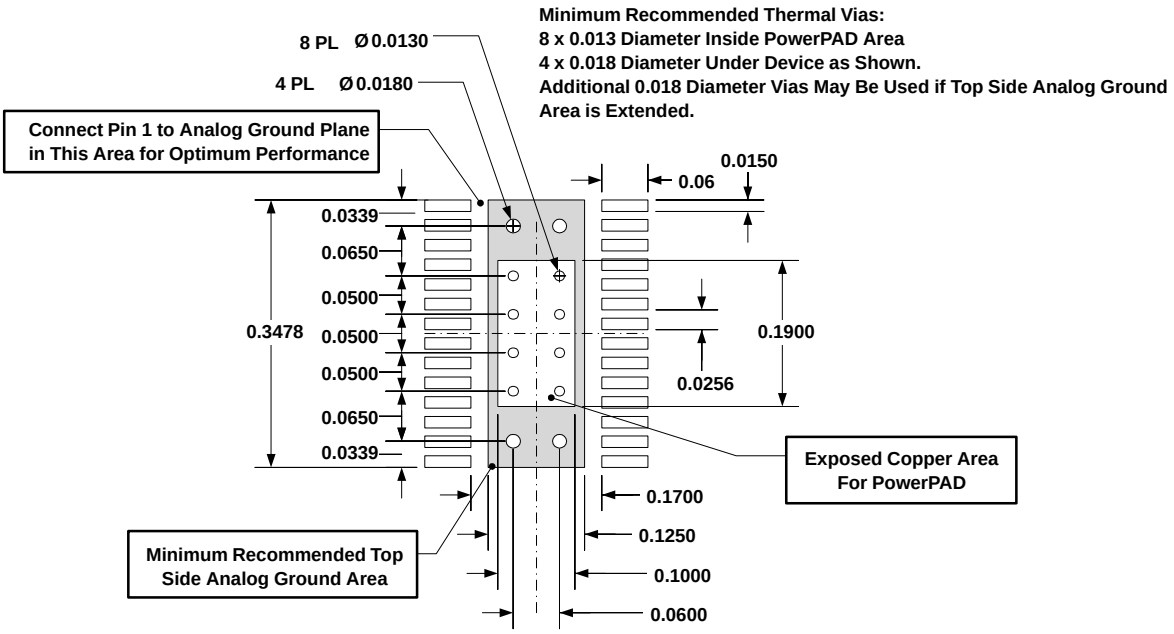


Figure 10. Recommended Land Pattern for 28-Pin PWP PowerPAD

LOAD TRANSIENT RESPONSE

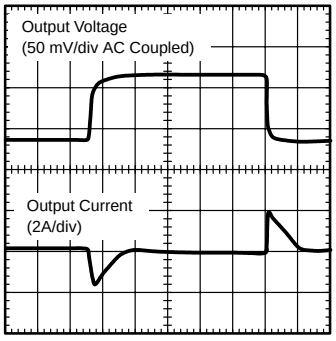


Figure 11

EFFICIENCY vs OUTPUT CURRENT

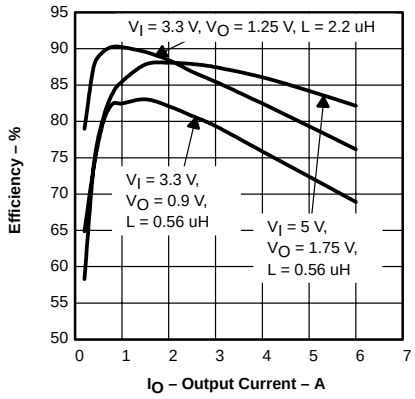
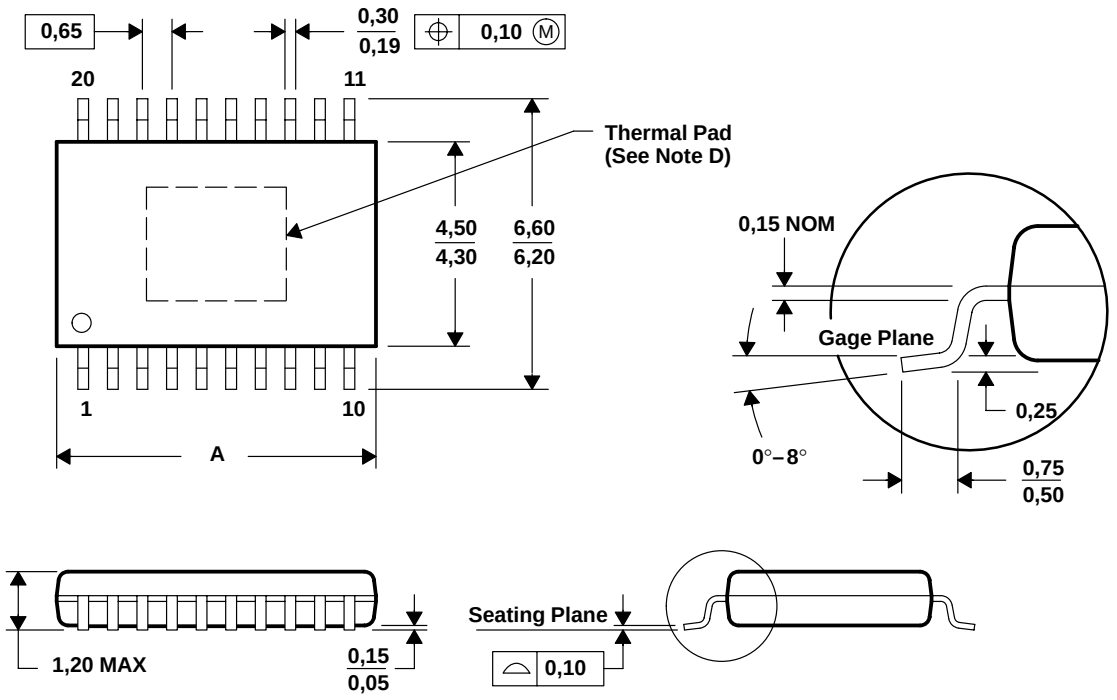


Figure 12

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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