

## PowerMOS transistor

BUK454-600B

## GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

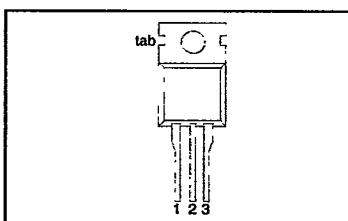
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	600	V
$I_D$	Drain current (DC)	2.6	A
$P_{tot}$	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	4.5	$\Omega$

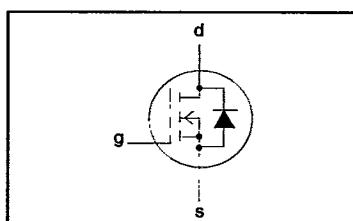
## PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	600	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	600	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
$I_D$	Drain current (DC)	$T_{mb} = 25^\circ\text{C}$	-	2.6	A
$I_D$	Drain current (DC)	$T_{mb} = 100^\circ\text{C}$	-	1.6	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25^\circ\text{C}$	-	10.4	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	75	W
$T_{sig}$	Storage temperature	-	-55	150	°C
$T_j$	Junction Temperature	-	-	150	°C

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-mb)}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient		-	60	-	K/W

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**STATIC CHARACTERISTICS** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA}$	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	2.1	3.0	4.0	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 600 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25^\circ\text{C}$	-	2	20	$\mu\text{A}$
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 600 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 125^\circ\text{C}$	-	0.1	1.0	mA
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 30 \text{ V}; V_{DS} = 0 \text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 1.2 \text{ A}$	-	4.0	4.5	$\Omega$

**DYNAMIC CHARACTERISTICS** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

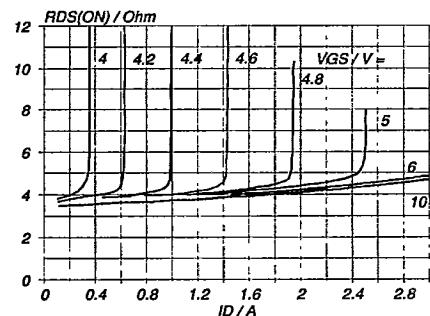
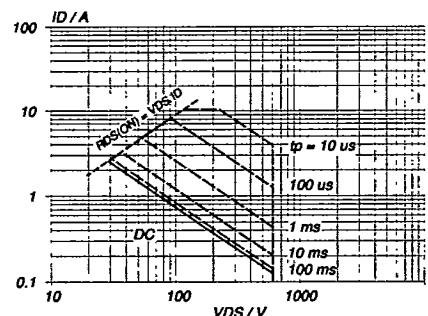
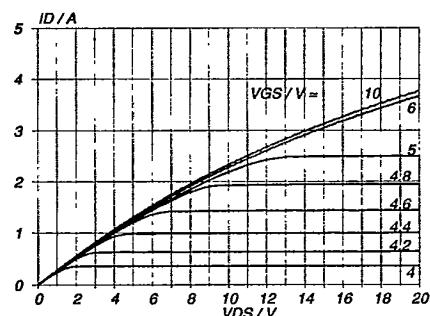
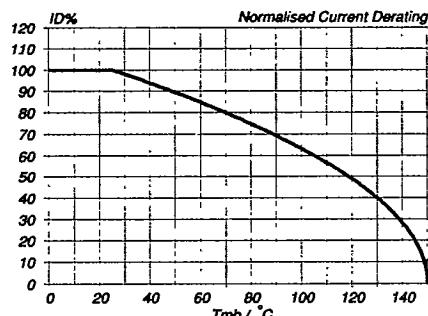
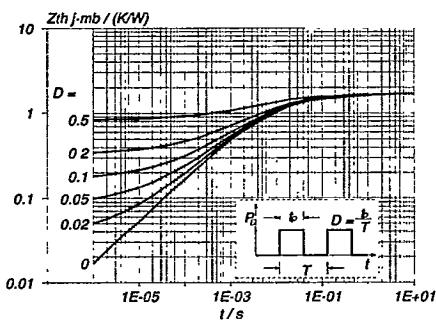
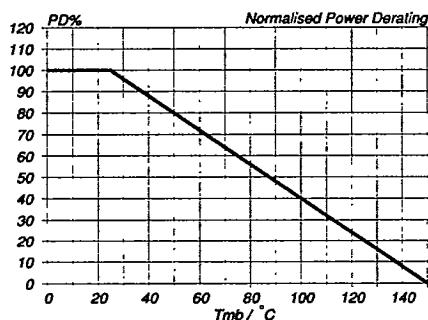
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 25 \text{ V}; I_D = 1.2 \text{ A}$	1.9	2.5	-	S
$C_{iss}$	Input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	-	300	500	pF
$C_{oss}$	Output capacitance		-	50	80	pF
$C_{rss}$	Feedback capacitance		-	30	55	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30 \text{ V}; I_D = 2.1 \text{ A}; V_{GS} = 10 \text{ V}; R_{GS} = 50 \Omega; R_{gen} = 50 \Omega$	-	15	20	ns
$t_r$	Turn-on rise time		-	40	60	ns
$t_{d(off)}$	Turn-off delay time		-	50	65	ns
$t_f$	Turn-off fall time		-	30	40	ns
$L_d$	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	-	-	-	2.8	A
$I_{DRM}$	Pulsed reverse drain current	-	-	-	11.2	A
$V_{SD}$	Diode forward voltage	$I_F = 2.8 \text{ A}; V_{GS} = 0 \text{ V}$	-	1.0	1.3	V
$t_{rr}$	Reverse recovery time	$I_F = 2.8 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	350	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = 0 \text{ V}; V_R = 100 \text{ V}$	-	3.5	-	$\mu\text{C}$

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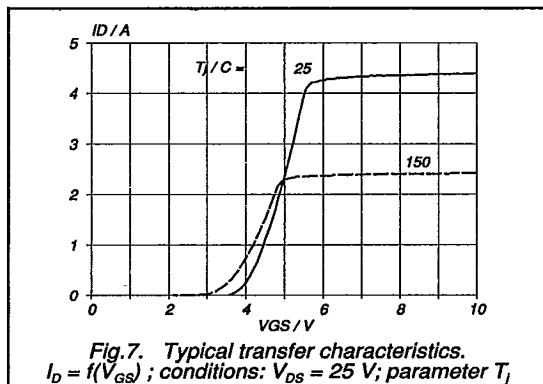


Fig.7. Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25\text{ V}$ ; parameter  $T_J$

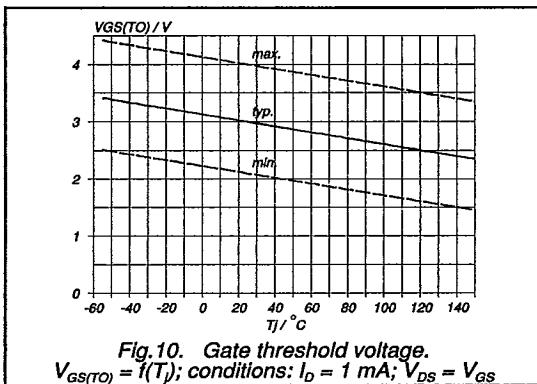


Fig.10. Gate threshold voltage.  
 $V_{GS(To)} = f(T_J)$ ; conditions:  $I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

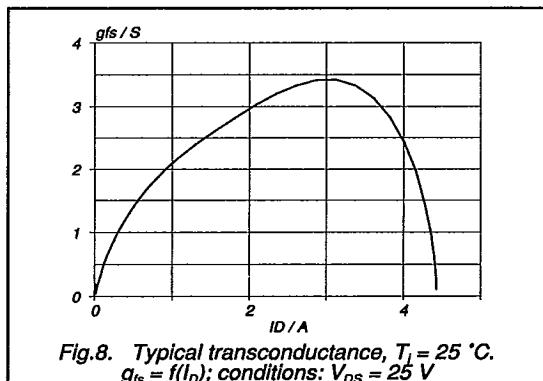


Fig.8. Typical transconductance,  $T_J = 25^\circ\text{C}$ .  
 $g_{fs} = f(I_D)$ ; conditions:  $V_{DS} = 25\text{ V}$

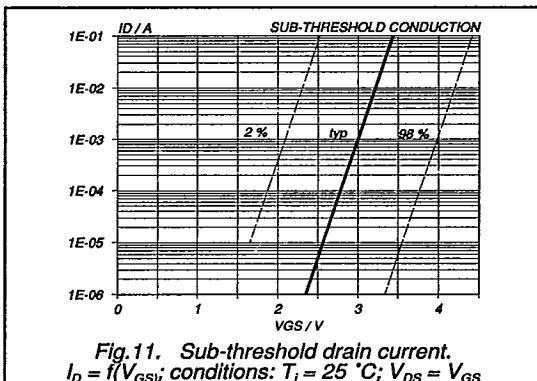


Fig.11. Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_J = 25^\circ\text{C}$ ;  $V_{DS} = V_{GS}$

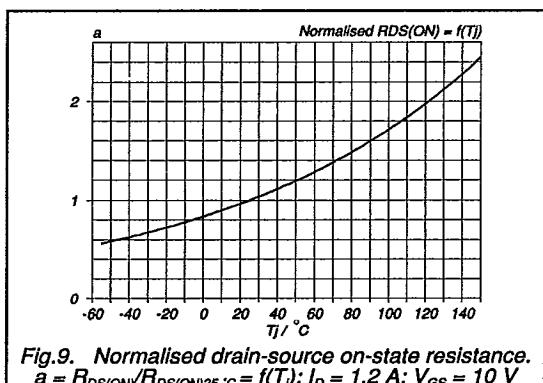


Fig.9. Normalised drain-source on-state resistance.  
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_J)$ ;  $I_D = 1.2\text{ A}$ ;  $V_{GS} = 10\text{ V}$

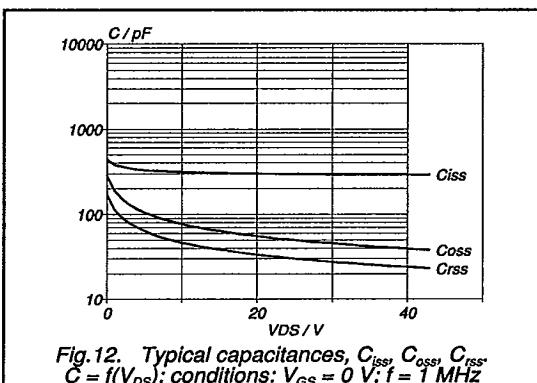


Fig.12. Typical capacitances,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ .  
 $C = f(V_{DS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

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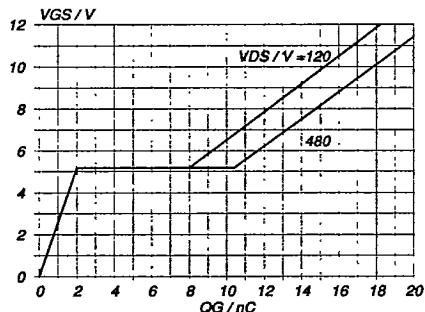


Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 2.8 \text{ A}$ ; parameter  $V_{DS}$

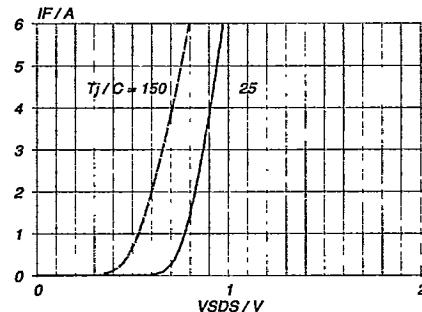


Fig.14. Typical reverse diode current.  
 $I_F = f(V_{DS})$ ; conditions:  $V_{GS} = 0 \text{ V}$ ; parameter  $T_j$