PowerMOS transistor Logic level FET

BUK551-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

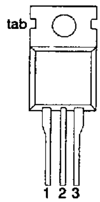
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK551	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	3.0	3.0	A
P_{tot}	Total power dissipation	40	40	W
T_j	Junction temperature	175	175	˚C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.85	1.1	Ω

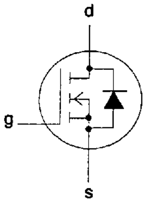
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ μs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 ˚C	-	3.0	3.0	A
I_D	Drain current (DC)	T_{mb} = 100 ˚C	-	3.0	2.8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 ˚C	-	12	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 ˚C	-	40		W
T_{stg}	Storage temperature	-	- 55	175		˚C
T_j	Junction Temperature	-	-	175		˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 ˚C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 ˚C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 2.5 A BUK551-100A	-	0.75	0.85	Ω
		BUK551-100B	-	0.90	1.10	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2.5 A	1.8	2.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	200	300	pF
C_{oss}	Output capacitance		-	45	60	pF
C_{rss}	Feedback capacitance		-	16	25	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 5 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	-	6	10	ns
t_r	Turn-on rise time		-	30	40	ns
$t_{d\,off}$	Turn-off delay time		-	10	20	ns
t_f	Turn-off fall time		-	20	30	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	3.0	A
I_{DRM}	Pulsed reverse drain current	-	-	-	12	A
V_{SD}	Diode forward voltage	I_F = 3.0 A ; V_{GS} = 0 V	-	1.1	1.4	V
t_{rr}	Reverse recovery time	I_F = 3.0 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	100	-	ns
Q_{rr}	Reverse recovery charge		-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.0 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	10	mJ

PowerMOS transistor Logic level FET

BUK551-100A/B

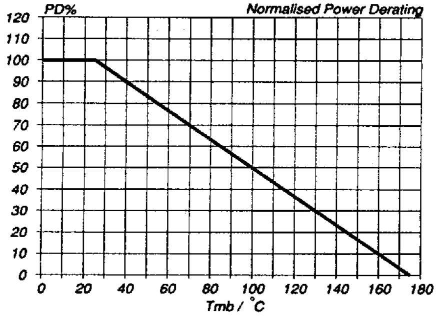


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\,25\,^\circ C} = f(T_{mb})$

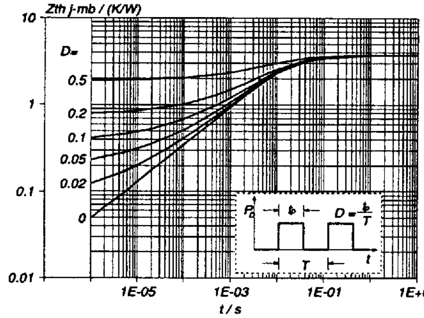


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

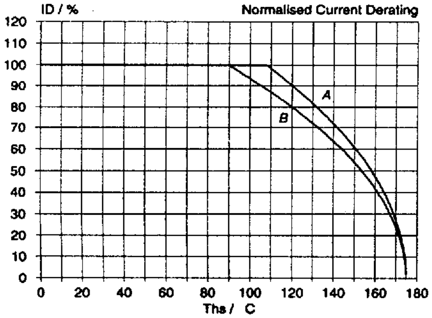


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\,25\,^\circ C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

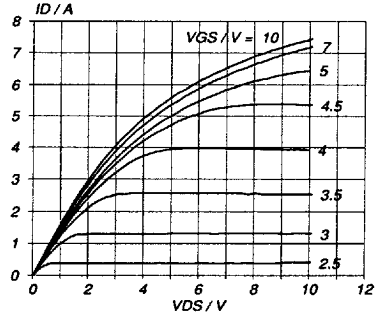


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{GS}

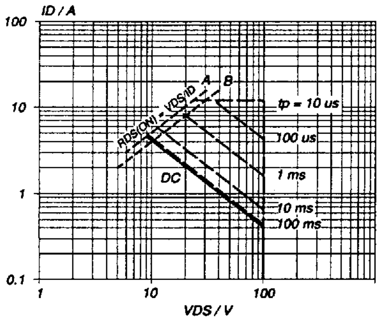


Fig.3. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

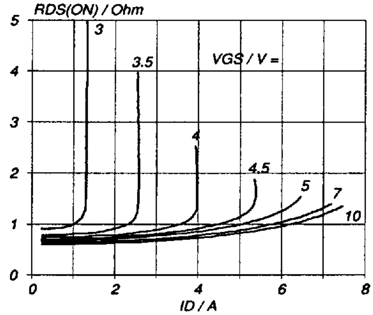


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

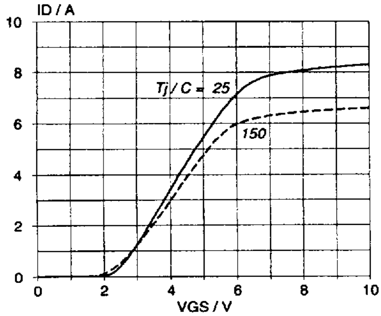


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

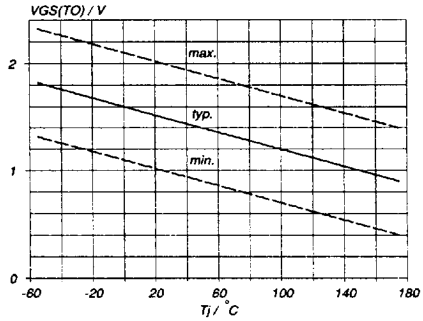


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

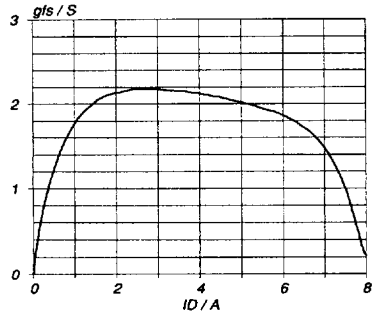


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

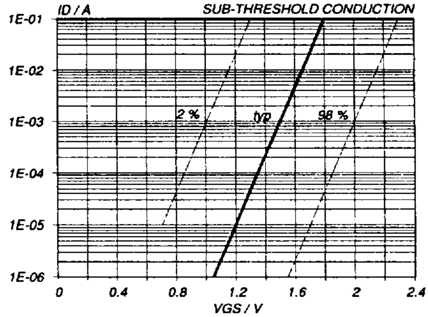


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

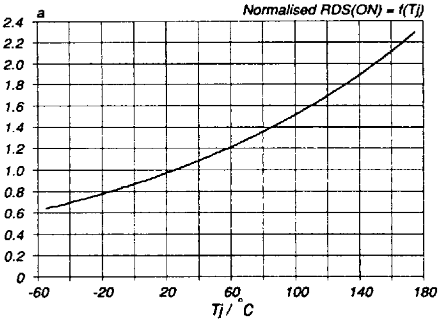


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.5 A; V_{GS} = 5 V

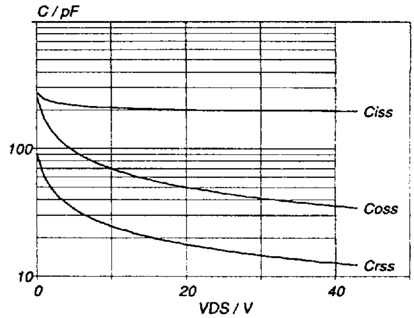


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

PowerMOS transistor
Logic level FET

BUK551-100A/B

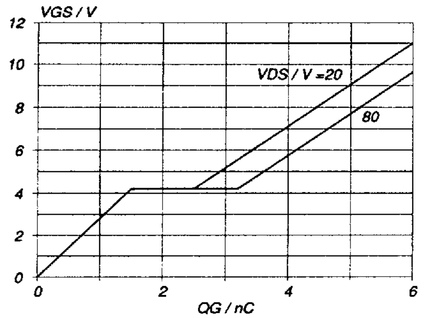


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 3 A; parameter V_{DS}

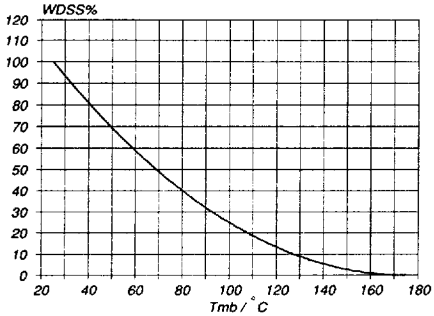


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 3 A

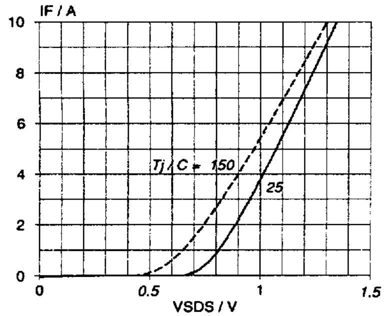


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

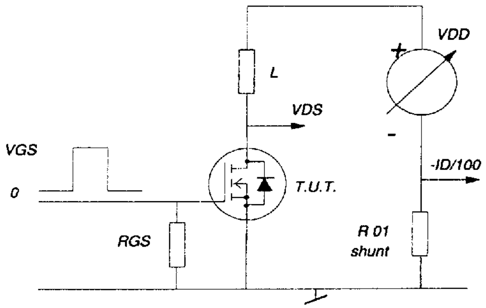


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$