PowerMOS transistor Fast Recovery Diode FET

BUK627-450B

T-39-11

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full pack envelope. FREDFET with fast recovery reverse diode, particularly suitable for motor control applications, eg. in full bridge configurations for which faster recovery characteristics simplify design for inductive loads.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	450	V
I_D	Drain current (DC)	5.6	A
P_{tot}	Total power dissipation	45	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.65	Ω
t_{rr}	Diode reverse recovery time	250	ns

MECHANICAL DATA

Dimensions in mm

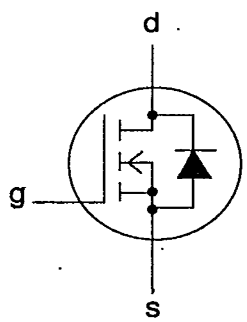
Net Mass: 5.5 g

Pinning:

1 = Gate

2 = Drain

3 = Source



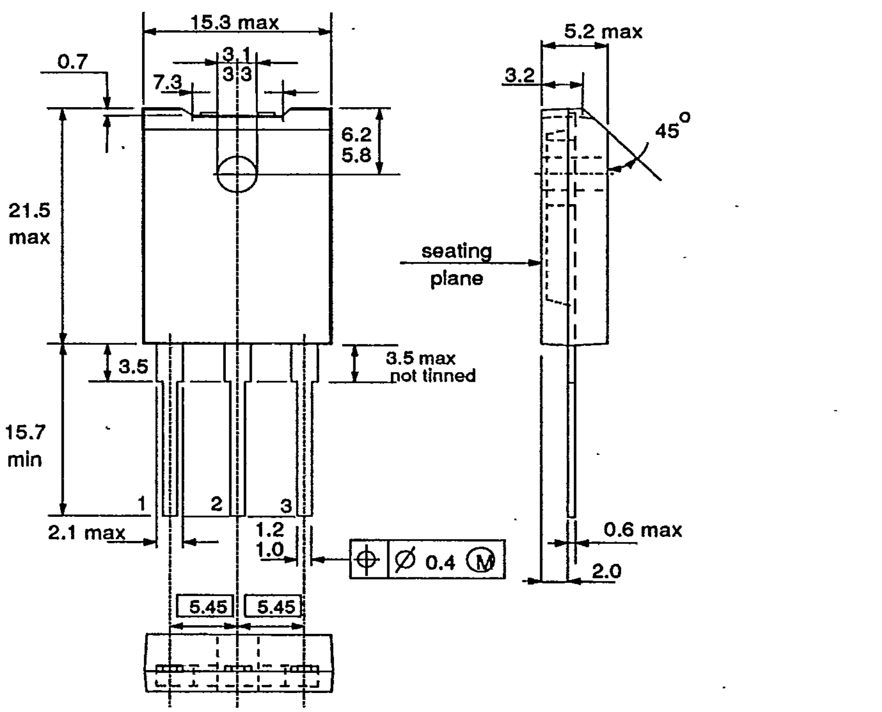


Fig.1 SOT-199; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for F-pack envelopes.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	450	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	450	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	5.6	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	3.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	22	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	45	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

From junction to heatsink	with heatsink compound	$R_{th\,j\text{-}hs}$ = 2.8 K/W
From junction to ambient	-	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	450	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 450 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 450 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6.5 A	-	0.6	0.65	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6.5 A	5.0	8.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	1800	pF
C_{oss}	Output capacitance		-	170	270	pF
C_{rss}	Feedback capacitance		-	70	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.8 A;	-	20	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	200	250	ns
t_f	Turn-off fall time		-	75	90	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

ISOLATION

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65 % ; clean and dustfree	-	-	2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	22	-	pF

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-		-	-	5.6	A
I_{DRM}	Pulsed reverse drain current	-		-	-	22	A
V_{SD}	Diode forward voltage	I_F = 5.6 A;	V_{GS} = 0 V	-	1.1	1.5	V
t_{rr}	Reverse recovery time	I_F = 5.6 A;	T_j = 25 °C	-	180	250	ns
		$-dI_F/dt$ =	T_j = 125 °C	-	220	300	ns
Q_{rr}	Reverse recovery charge	100 A/µs;	T_j = 25 °C	-	0.65	1.2	µC
		V_{GS} = 0 V;	T_j = 125 °C	-	2.6	5.0	µC
I_{rrm}	Reverse recovery current	V_R = 100 V	T_j = 125 °C	-	15	-	A

AVALANCHE RATING

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A ; $V_{DD} \leq$ 250 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	500	mJ

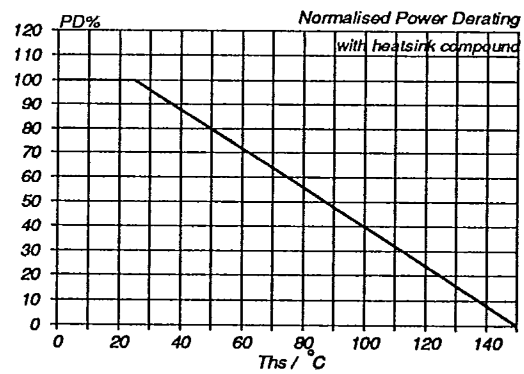

Fig.2. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\,25\,°C} = f(T_{hs})$

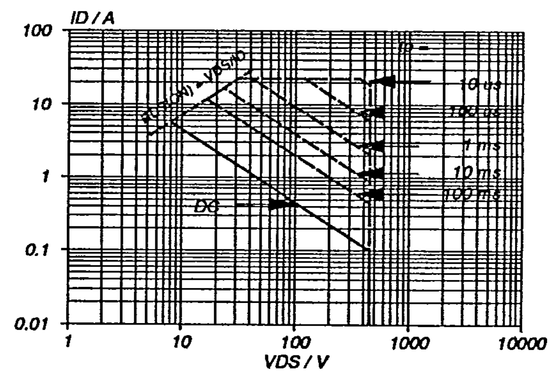

Fig.4. Safe operating area. T_{hs} = 25 °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

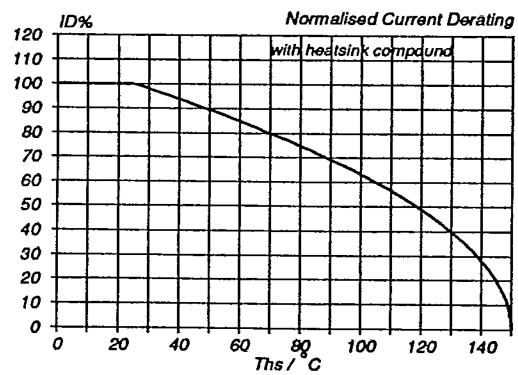

Fig.3. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\,25\,°C} = f(T_{hs})$; conditions: $V_{GS} \geq 10$ V

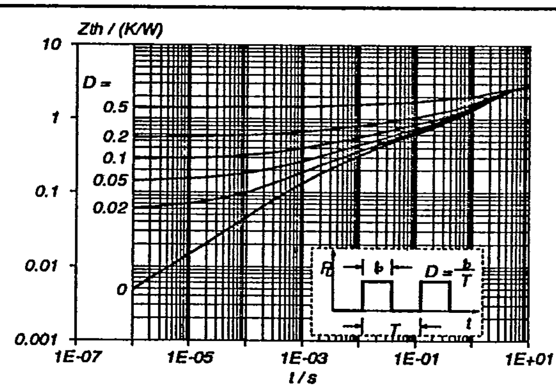

Fig.5. Transient thermal impedance.
$Z_{th\,j\text{-}hs} = f(t)$; parameter $D = t_p/T$

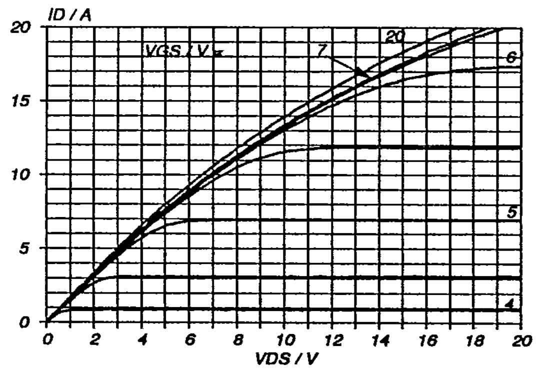

Fig.6. [1] Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

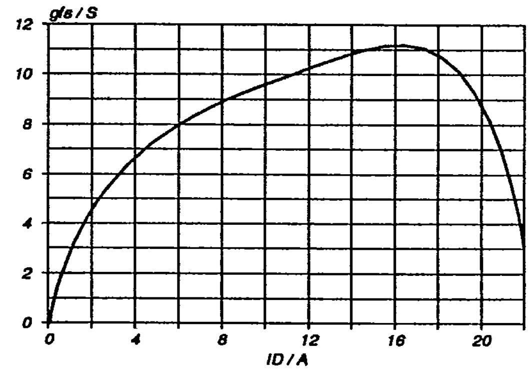

Fig.9. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

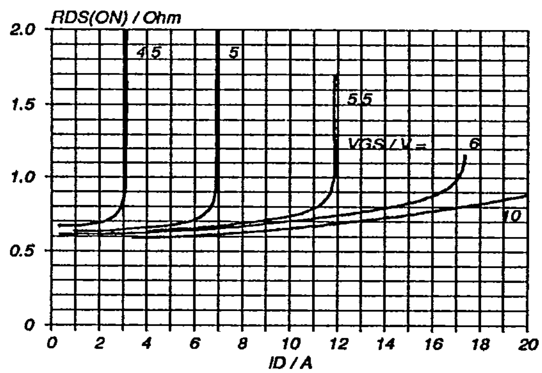

Fig.7. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

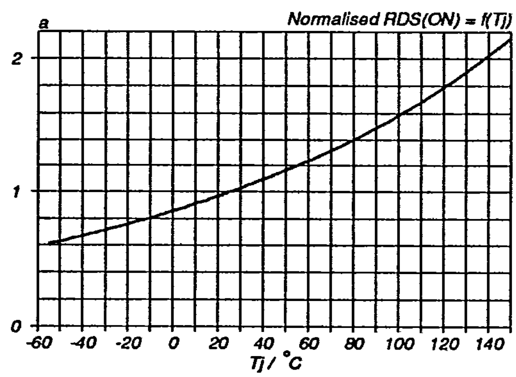

Fig.10. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 6.5$ A; $V_{GS} = 10$ V

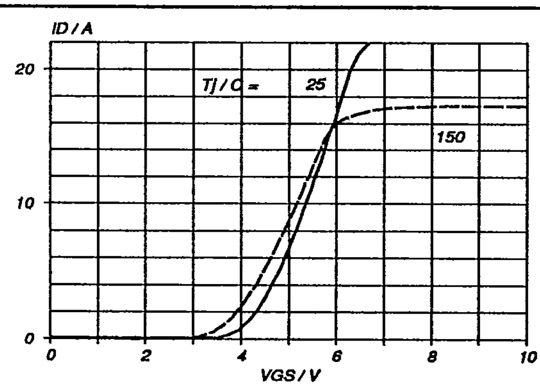

Fig.8. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

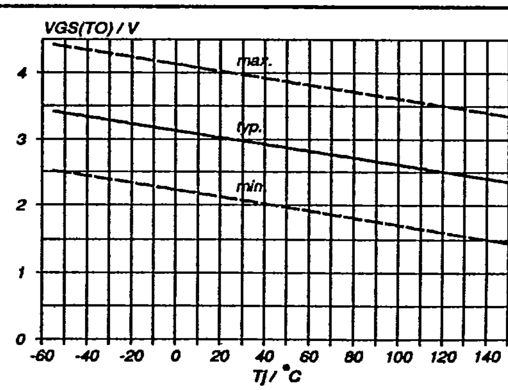

Fig.11. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

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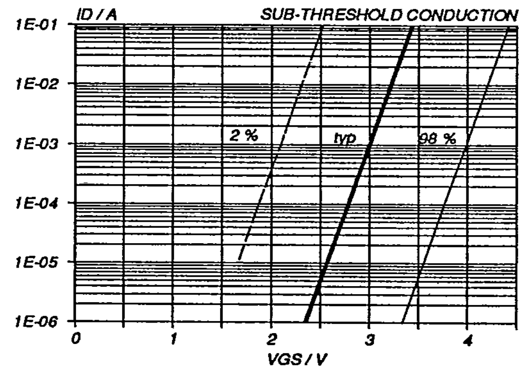

Fig.12. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

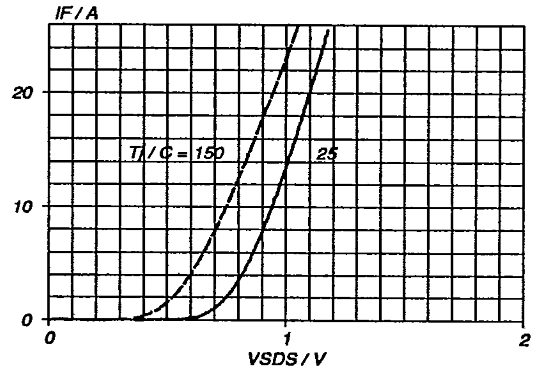

Fig.15. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

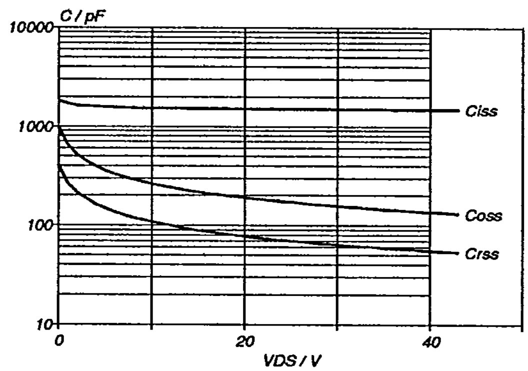

Fig.13. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

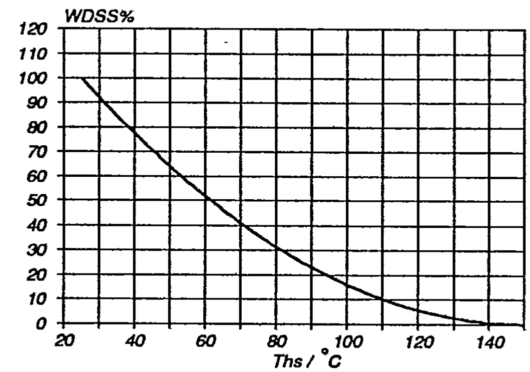

Fig.16. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 11$ A

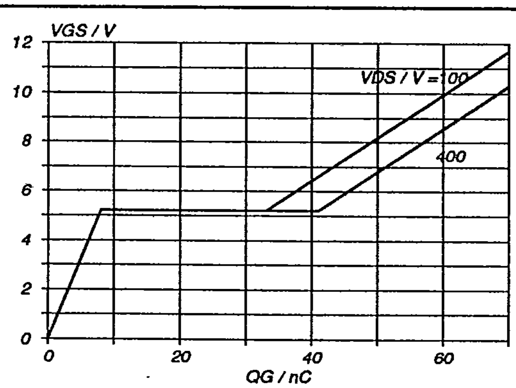

Fig.14. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 11$ A; parameter V_{DS}

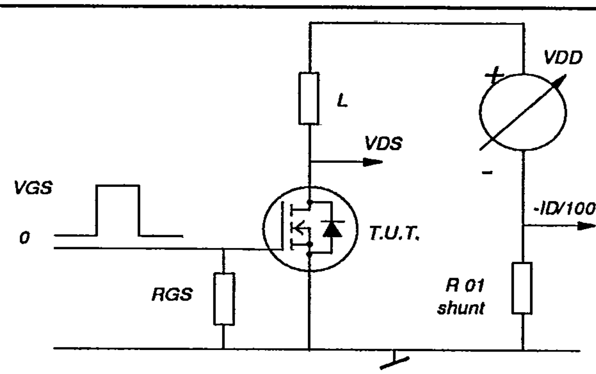

Fig.17. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$