

BUK7107-55ATE

TrenchPLUS standard level FET

Rev. 01 — 29 July 2002

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring both very low on-state resistance, and diode for temperature sensing.

Product availability:

BUK7107-55ATE in SOT426 (D²-PAK).

1.2 Features

- Integrated temperature sensor
- ESD protection
- Q101 compliant
- Standard level compatible

1.3 Applications

- Variable Valve Timing for engines
- Automotive and power switching
- Electrical Power Assisted Steering
- Fan control

1.4 Quick reference data

- $V_{DS} = 55 \text{ V}$ (max)
- $I_D = 75 \text{ A}$ (max)
- $R_{DSon} = 5.8 \text{ m}\Omega$ (typ)
- $V_F = 658 \text{ mV}$ (typ)
- $S_F = -1.54 \text{ mV/K}$ (typ)
- $P_{tot} = 272 \text{ W}$

2. Pinning information

Table 1: Pinning - SOT426 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	anode (a)		
3	drain (d)		
4	cathode (k)		
5	source (s)		
mb	mounting base; connected to drain (d)	 Front view SOT426	 MBL317



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3. Limiting values

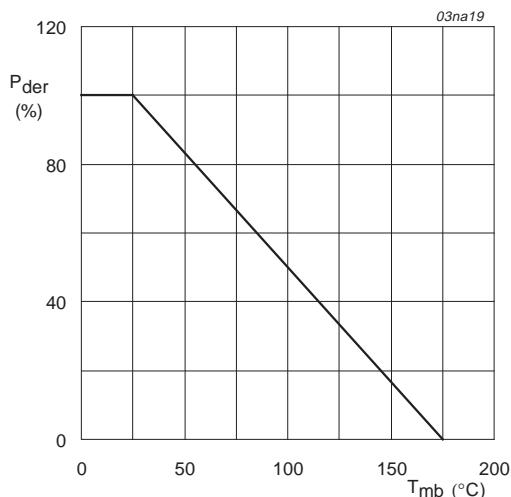
Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
V_{DGS}	drain-gate voltage (DC)	$I_{DG} = 250 \mu A$	-	55	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25^\circ C; V_{GS} = 10 V$; Figure 2 and 3	[1] -	140	A
			[2] -	75	A
		$T_{mb} = 100^\circ C; V_{GS} = 10 V$; Figure 2	[2] -	75	A
I_{DM}	peak drain current	$T_{mb} = 25^\circ C$; pulsed; $t_p \leq 10 \mu s$; Figure 3	-	560	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ C$; Figure 1	-	272	W
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA
		$t_p = 5 ms; \delta = 0.01$	-	50	mA
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	± 100	V
T_{stg}	storage temperature		-55	+175	$^\circ C$
T_j	junction temperature		-55	+175	$^\circ C$
Source-drain diode					
I_{DR}	reverse drain current	$T_{mb} = 25^\circ C$	[1] -	140	A
			[2] -	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25^\circ C$; pulsed; $t_p \leq 10 \mu s$	-	560	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 68 A$; $V_{DS} \leq 55 V$; $V_{GS} = 10 V$; $R_{GS} = 50 \Omega$; starting $T_j = 25^\circ C$	-	460	mJ
Electrostatic Discharge					
V_{esd}	electrostatic discharge voltage; pins 1,3,5	Human Body Model; $C = 100 pF$; $R = 1.5 k\Omega$		6	kV

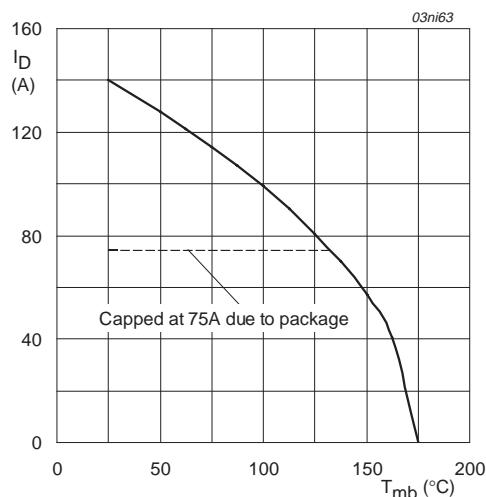
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



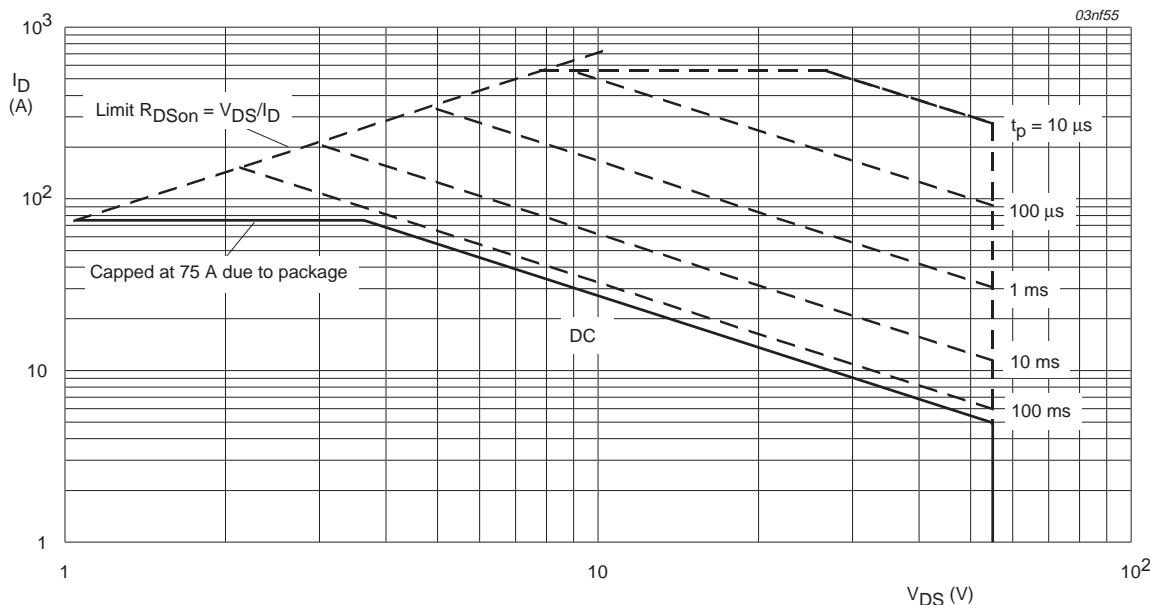
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ C)} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



V_{GS} ≥ 10 V

Fig 2. Continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient SOT426	minimum footprint; mounted on a PCB	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.55	K/W

4.1 Transient thermal impedance

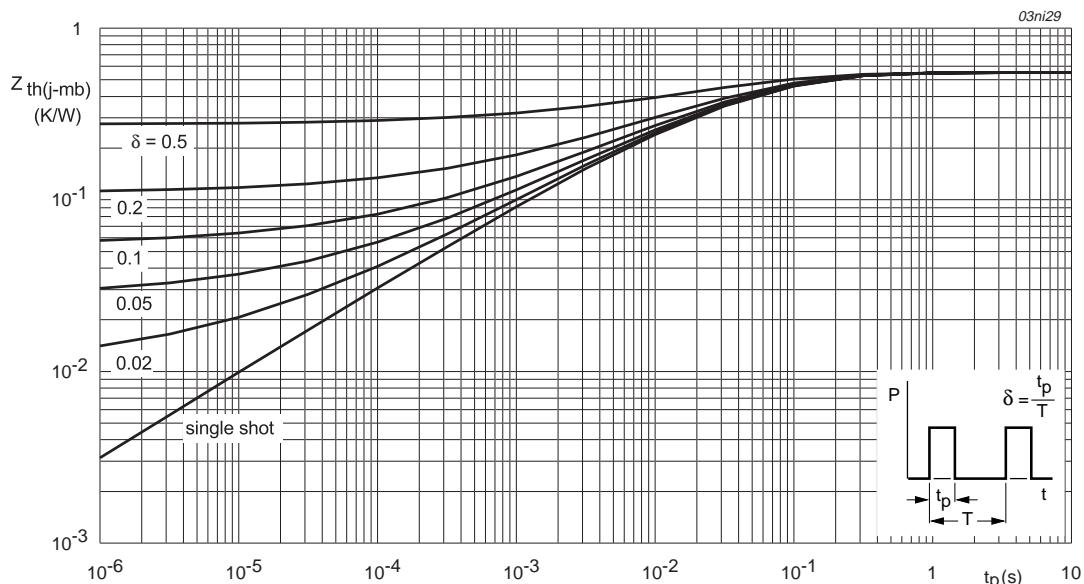


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

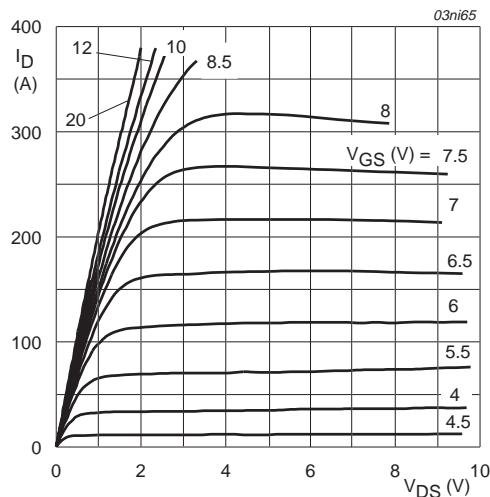
5. Characteristics

Table 4: Characteristics $T_j = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}$ $T_j = 25^\circ\text{C}$ $T_j = -55^\circ\text{C}$	55	-	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$; Figure 9 $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2	3	4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}$ $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$	-	0.1	10	μA
$V_{(\text{BR})\text{GSS}}$	gate-source breakdown voltage	$I_G = \pm 1 \text{ mA};$ $-55^\circ\text{C} < T_j < 175^\circ\text{C}$	20	22	-	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10 \text{ V}; V_{DS} = 0 \text{ V}$ $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$	-	22	1000	nA
$R_{DS\text{on}}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 50 \text{ A};$ Figure 7 and 8 $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$	-	5.8	7	$\text{m}\Omega$
V_F	forward voltage, temperature sense diode	$I_F = 250 \mu\text{A}$	648	658	668	mV
S_F	temperature coefficient temperature sense diode	$I_F = 250 \mu\text{A};$ $-55^\circ\text{C} < T_j < 175^\circ\text{C}$	-1.4	-1.54	-1.68	mV/K
V_{hys}	temperature sense diode forward voltage hysteresis	$125 \mu\text{A} < I_F < 250 \mu\text{A}$	25	32	50	mV
Dynamic characteristics						
$Q_{g(\text{tot})}$	total gate charge	$V_{GS} = 10 \text{ V}; V_{DS} = 44 \text{ V};$ $I_D = 25 \text{ A}$; Figure 14	-	116	-	nC
Q_{gs}	gate-source charge		-	19	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	50	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V};$	-	4500	-	pF
C_{oss}	output capacitance	$f = 1 \text{ MHz}$; Figure 12	-	960	-	pF
C_{rss}	reverse transfer capacitance		-	510	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DD} = 30 \text{ V}; R_L = 1.2 \Omega;$	-	36	-	ns
t_r	rise time	$V_{GS} = 10 \text{ V}; R_G = 10 \Omega$	-	115	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	159	-	ns
t_f	fall time		-	111	-	ns

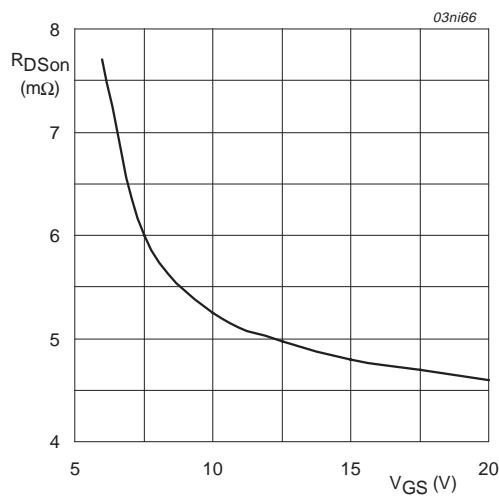
Table 4: Characteristics...continued $T_j = 25^\circ C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_d	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_s	internal source inductance	from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V};$ Figure 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}$	-	80	-	ns
Q_r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}$	-	200	-	nC



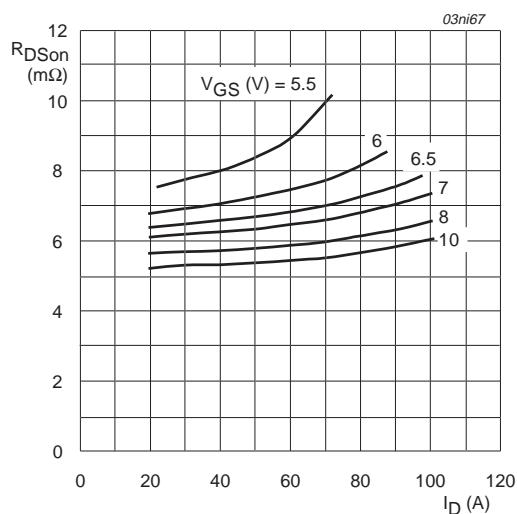
$T_j = 25^\circ\text{C}$; $t_p = 300 \mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



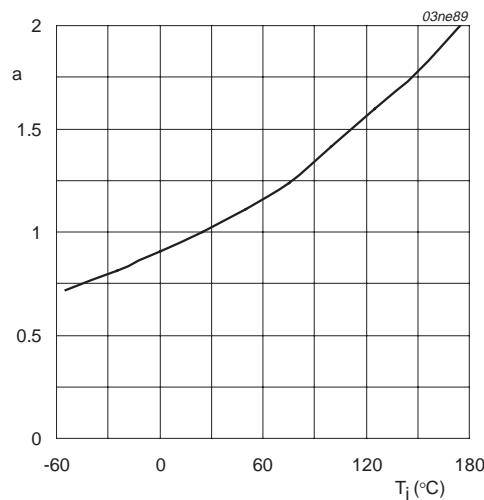
$T_j = 25^\circ\text{C}$; $I_D = 50 \text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



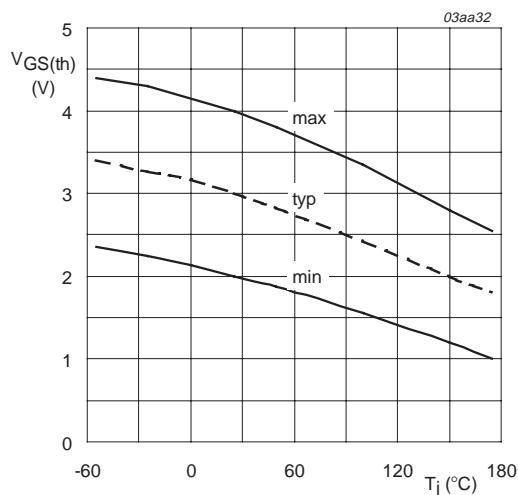
$T_j = 25^\circ\text{C}$; $t_p = 300 \mu\text{s}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



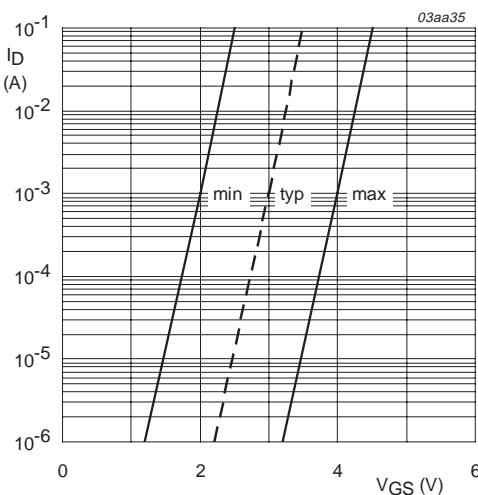
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



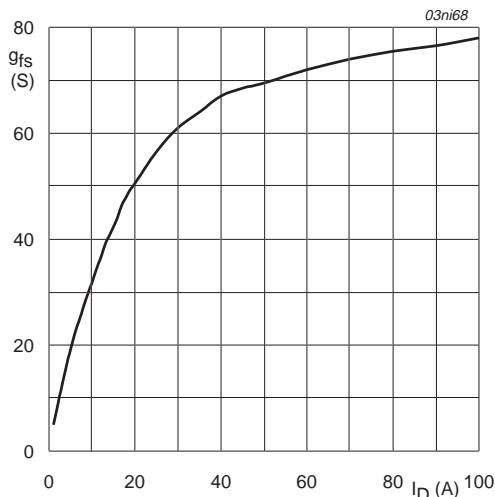
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



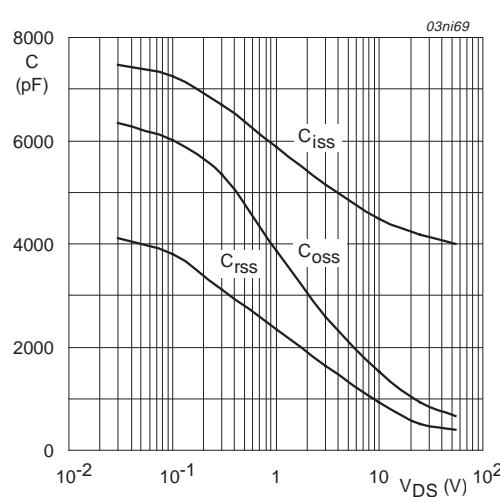
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



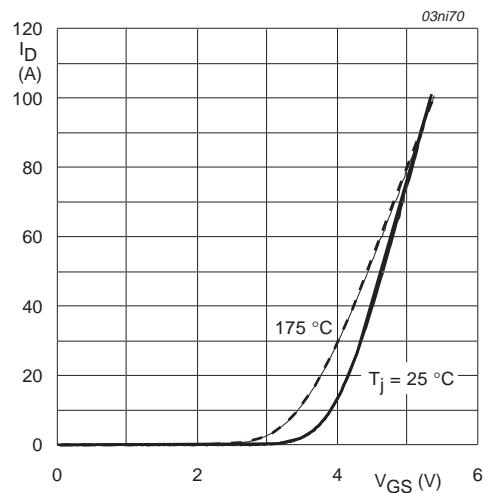
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



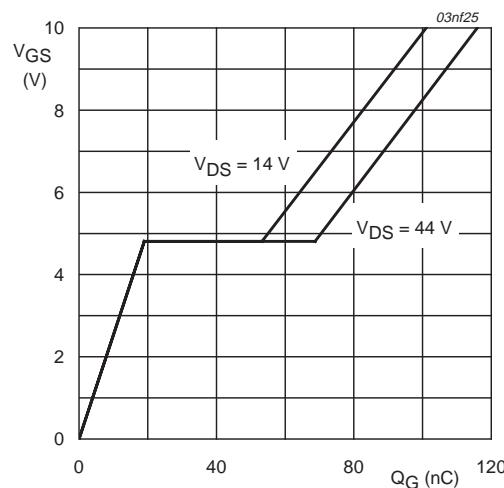
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



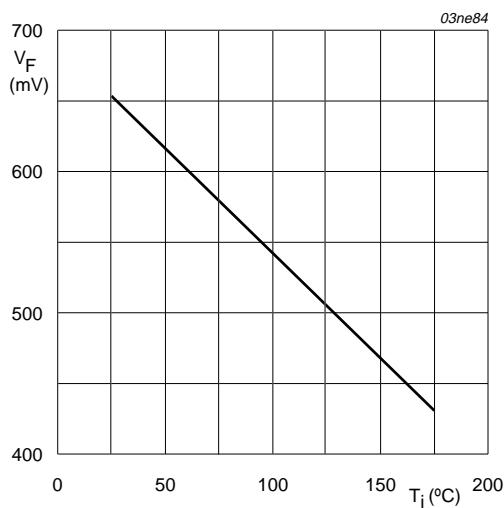
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



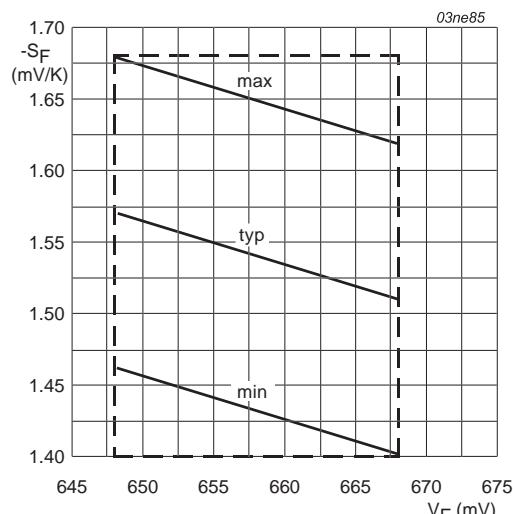
$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



$I_F = 250 \mu\text{A}$

Fig 15. Forward voltage of temperature sense diode as a function of junction temperature; typical values.



V_F at $T_j = 25 \text{ °C}; I_F = 250 \mu\text{A}$

Fig 16. Temperature coefficient of temperature sense diode as a function of forward voltage; typical values.

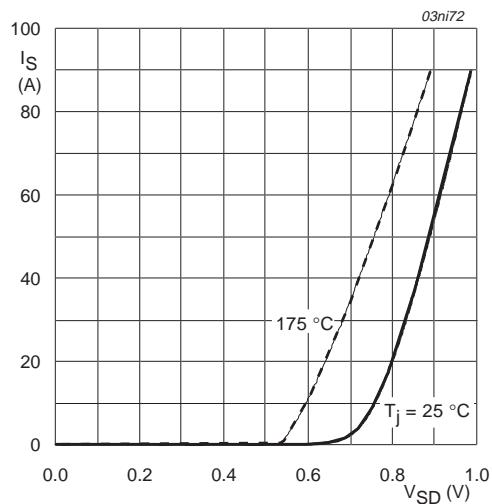
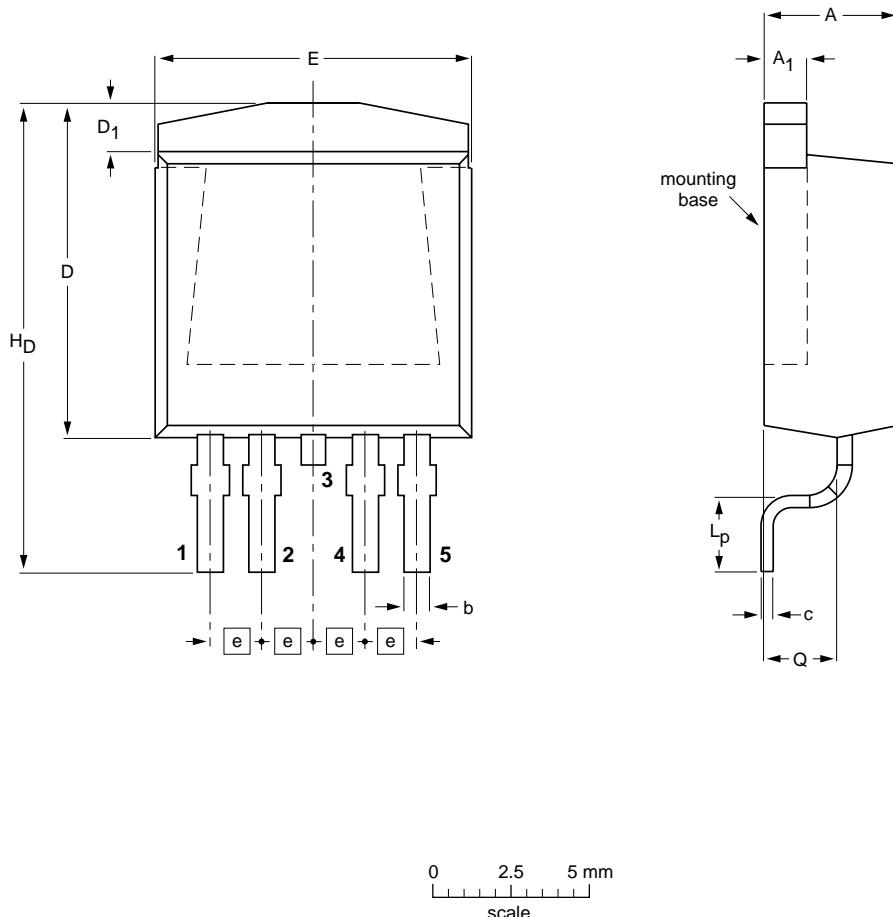
 $V_{GS} = 0 \text{ V}$

Fig 17. Reverse diode current as a function of reverse diode voltage; typical values.

6. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK); 5 leads
(one lead cropped)

SOT426



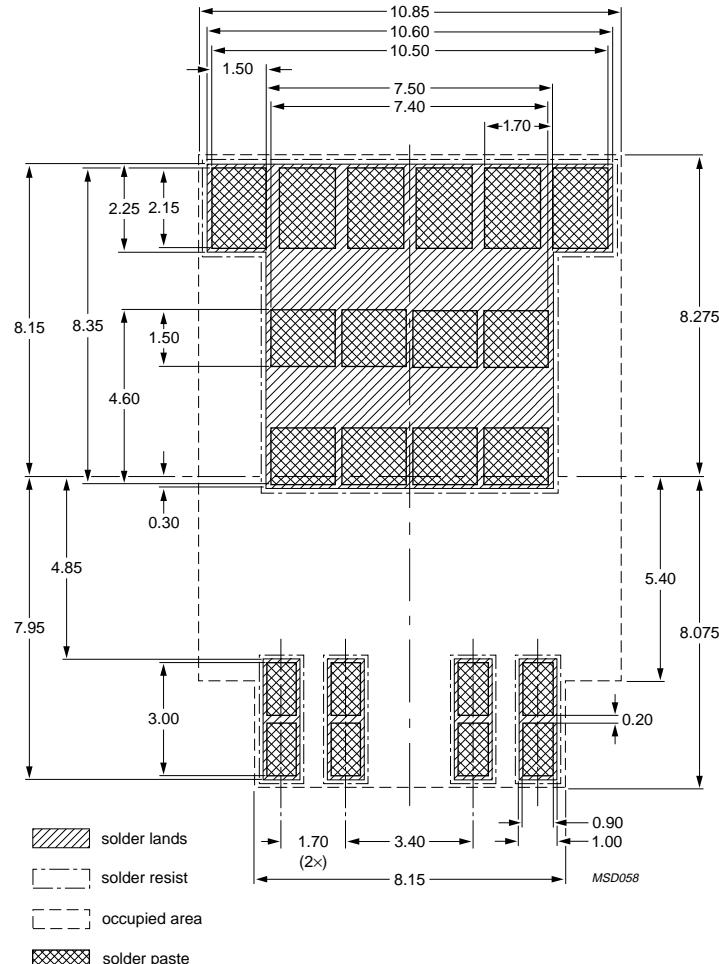
DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D max.	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	1.70	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT426						-98-12-14 99-06-25

Fig 18. SOT426 (D²-PAK).

7. Soldering



Dimensions in mm.

Fig 19. Reflow soldering footprint for SOT426.

8. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20020729	-	Product data; initial version

9. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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