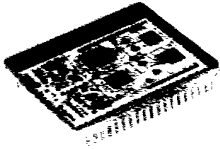




BUS-61555

MIL-STD-1553 ADVANCED INTEGRATED MUX (AIM) HYBRID



APPROX. 1/2
ACTUAL SIZE

**PLEASE REFERENCE BUS-61555
DATA SHEET FOR TIMING
SPECIFICATIONS**

FEATURES

- +5 VOLT ONLY
- VERY LOW POWER
- COMPLETE INTEGRATED MUX INCLUDING:
 - LOW POWER DUAL TRANSCEIVER
 - BC/RTU/MT PROTOCOL
 - 8K x 16 SHARED RAM
 - INTERRUPT LOGIC
- COMPATIBLE WITH MIL-STD-1750 AND OTHER STANDARD CPUs
- MINIMIZES CPU OVERHEAD
- PROVIDES MEMORY MAPPED 1553 INTERFACE
- ON-LINE AND OFF-LINE SELF-TEST
- IBM PC® DEVELOPMENT TOOLS AVAILABLE

DESCRIPTION

DDC's BUS-61555 Advanced Integrated Mux (AIM) Hybrid is a complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT) device requiring only a +5 volt power supply. Packaged in a single 78 pin DIP package, the BUS-61555 contains dual low-power transceivers, complete BC/RTU/MT protocol logic, a MIL-STD-1553-to-host interface unit and an 8K x 16 RAM.

Using an industry standard dual transceiver and standard status and control signals, the BUS-61555 simplifies system integration at both the MIL-STD-1553 and host processor interface levels.

The CPU controls all 1553 operations by

accessing the shared 8K x 16 RAM. To ensure maximum design flexibility, memory control lines are provided for attaching external RAM to the BUS-61555 Address and Data Buses and for disabling internal memory; the total combined memory space can be expanded to 64K x 16. All 1553 transfers are entirely memory-mapped; thus the CPU interface requires minimal hardware and/or software support.

The BUS-61555 operates over the full military -55°C to +125°C temperature range. Available screened to MIL-STD-883, the BUS-61555 is ideal for demanding military and industrial microprocessor to 1553 interface applications.

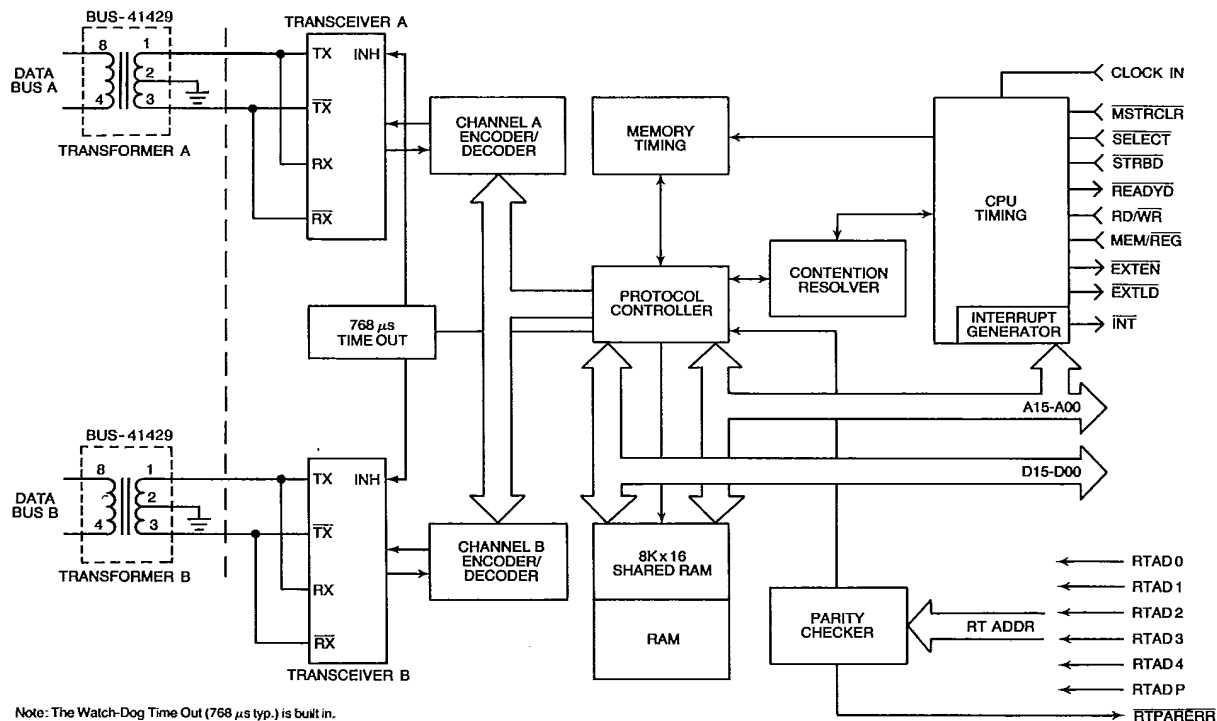


FIGURE 1. BUS-61555 BLOCK DIAGRAM

TABLE 1. BUS-61555 SPECIFICATIONS

Specifications at nominal power supply voltages.		
PARAMETER	VALUE	NOTES
RECEIVER		
Differential Input Voltage	V_{p-p}	40 max
Differential Input Impedance	K Ohms	7 min
CMRR	dB	40 min
TRANSMITTER (Direct Coupled)*		
Differential Output Voltage	V_{p-p}	6.0 min, 9.0 max
Output Rise and Fall Times	n sec	100 min, 300 max
Output Offset Voltage	mV	± 90 max
LOGIC		
V_{IH}	V	2.2 min
V_{IL}	V	0.8 max
CLOCK		
	MHz	16
POWER SUPPLIES		
+5V (Logic)	V	$\pm 5 \pm 10\%$
+5VA (Chan A)	V	$\pm 5 \pm 10\%$
+5VB (Chan B)	V	$\pm 5 \pm 10\%$
Current Drain (Total Package)		(Typ)/max
Idle	mA	(70)/160
25% Duty Cycle	mA	(205)/310
50% Duty Cycle	mA	(340)/460
100% Duty Cycle	mA	(610)/760
TEMPERATURE RANGE		
Operating (Case)	°C	-55 to +125
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size		
78 pin DIP	in (mm)	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)
82 pin Flatpack	in (mm)	2.19 x 1.6 x 1.7 (55.6 x 40.6 x 4.34)
Weight	oz (g)	1.0 (29)

*Given for direct coupled output across 35 ohms.

TABLE 2. BUS-61555 PIN OUTS

PIN	NAME	PIN	NAME
1	D00	40	TX/RX-A
2	D02	41	D01
3	D04	42	D03
4	D06	43	D05
5	D08	44	D07
6	D10	45	D09
7	D12	46	D11
8	D14	47	D13
9	RTAD1	48	D15
10	RTAD0	49	RTAD3
11	RTAD4	50	RTAD2
12	ILLCMD	51	RTADP
13	SA/MC-0	52	SA/MC-2
14	LOGIC +5V	53	SA/MC-4
15	SA/MC-1	54	SA/MC-3
16	BCSTRCV	55	THIS-RT
17	LMC	56	RTPARERR
18	NC	57	T/R
19	GNDB	58	+5VB
20	TX/RX-B	59	TX/RX-B
21	LOGIC GND	60	A00
22	A01	61	A02
23	A03	62	A04
24	A05	63	A06
25	A07	64	A08
26	A09	65	A10
27	A11	66	A12
28	A13	67	A14
29	A15	68	MEMWR
30	MEMOE	69	MEMENA-IN
31	MEMENA-OUT	70	INCMD
32	CLOCK IN	71	MSTRCLR
33	MEM/REG	72	INT
34	STRBD	73	IOEN
35	EXTEN	74	SELECT
36	RD/WR	75	READYD
37	EXTLD	76	TAGEN
38	GNDA	77	+5VA
39	NC	78	TX/RX-A

ORDERING INFORMATION

BUS-61555-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

Blank = 0° to 70° C

Note: Flatpack version available, contact factory for details.

Specifications are subject to change without notice.

DDC
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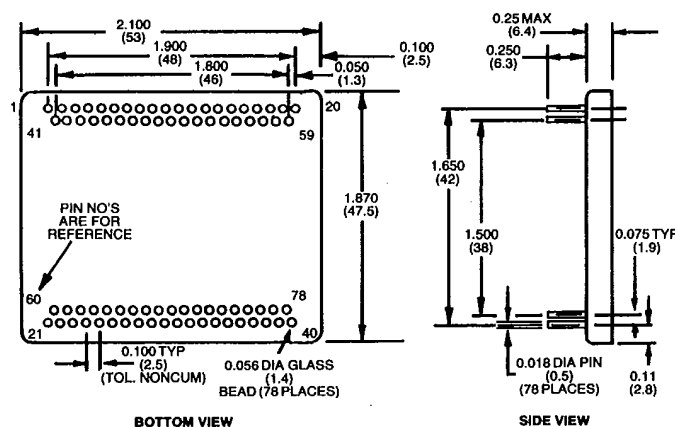
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Note: Dimensions are in inches (millimeters).

FIGURE 2. MECHANICAL OUTLINE (DDIP)