

The TQ9121 Low-Noise Amplifier is part of TriQuint's RFIC Downconverter Building Block family. Intended for use in the first stages of a Low-Noise Receiver front end, the TQ9121 provides high-performance operation from a standard +5 V power supply. Its low current consumption and small, plastic surface-mount package are well suited for low-cost hand-held and battery-powered applications. The amplifier has internal self-bias circuitry for easy system integration. An external matching network at the input of the amplifier yields optimum noise performance. Output match to 50 Ω is provided internally. The input pin is internally DC-blocked.

Electrical Specifications

Test Conditions: $V_{DD} = +5\text{ V}$, $T_A = 25^\circ\text{C}$, Frequency 1575 MHz

Parameter ⁽¹⁾	Min.	Typ.	Max.	Units
Frequency of Operation	1200		1600	MHz
Gain	14	16		dB
Noise Figure		1.25	1.5	dB
DC Supply Current		17	24	mA

Note: 1. Min/Max values listed are production tested.

TQ9121

Low-Noise Amplifier

Features

- Single + 5 V supply
- SO-8 plastic package
- Low noise figure 1.25 dB, typ.
- 1200 – 1600 MHz operation
- Output matched to 50 Ω

Applications

- GPS (Global Positioning Systems)
- Satellite Terminals

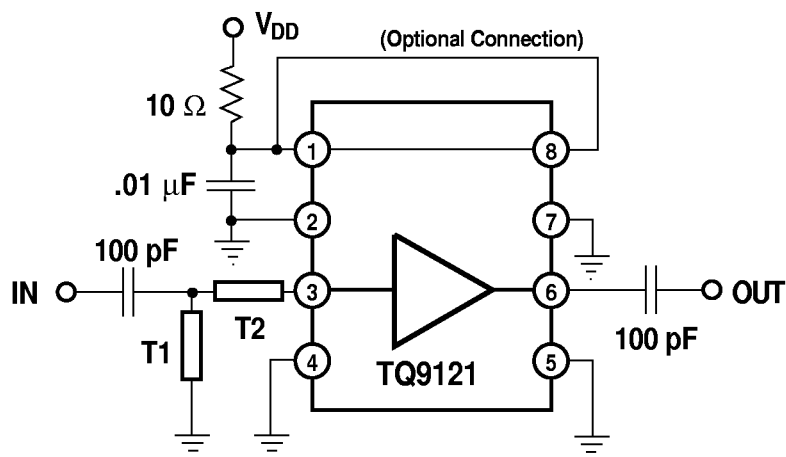
TQ9121

Electrical Specifications

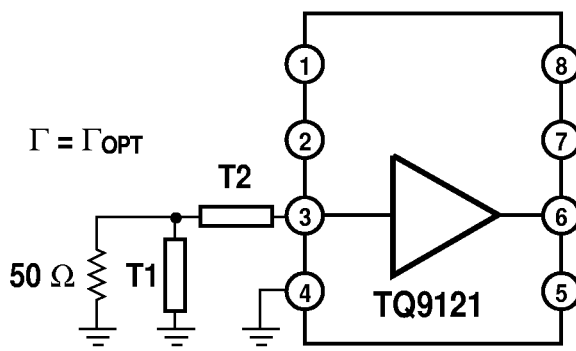
Test Conditions: $V_{DD} = +5\text{ V}$, $T_A = 25^\circ\text{C}$, Frequency = 1575 MHz

Parameter	Conditions	Min.	Typ.	Max.	Units
Gain		14	16		dB
Noise Figure			1.25	1.5	dB
Output 3rd. Order Intercept			+11		dBm
Output 1 dB Gain Compression			-2		dBm
Supply Voltage		4.5	5.0	5.5	V
Supply Current			17	24	mA

Test Circuit



Typical Noise-Matching Circuit



Note: T1 and T2 – Electrical length of 75 ohm transmission line is given in the Noise Parameters table.

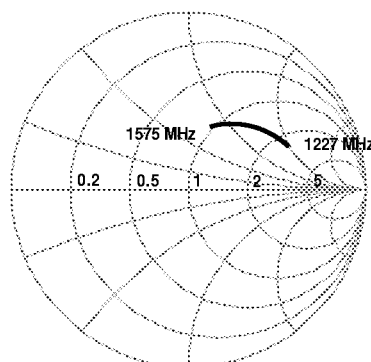
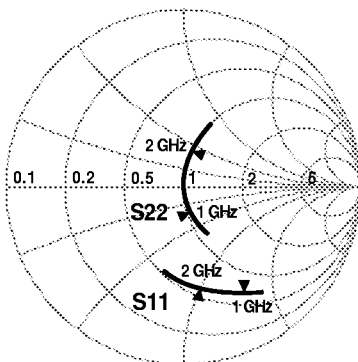
S-Parameters (typical) – SO-8 Package with no matching networksTest Conditions: $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$. (Reference plane at package pins)

Freq (MHz)	S11	$\angle S11$	S21	$\angle S21$	S12	$\angle S12$	S22	$\angle S22$	Gain (dB)
1.000	0.749	-57	12.2	-104	0.006	122	0.249	-68	21.7
1.100	0.727	-61	11.5	-115	0.007	114	0.183	-82	21.2
1.200	0.702	-67	10.8	-125	0.007	110	0.114	-86	20.6
1.227	0.697	-68	10.6	-128	0.007	108	0.079	-100	20.5
1.300	0.684	-71	10.0	-135	0.008	104	0.029	-145	20.0
1.400	0.666	-76	9.3	-145	0.009	101	0.068	135	19.4
1.500	0.654	-81	8.6	-155	0.010	94	0.126	104	18.7
1.575	0.645	-85	8.1	-162	0.010	96	0.183	98	18.2
1.600	0.642	-86	8.0	-164	0.010	96	0.200	96	18.0
1.700	0.629	-91	7.3	-173	0.011	89	0.254	84	17.2
1.800	0.620	-96	6.7	178	0.011	86	0.343	78	16.6
1.900	0.612	-102	6.1	169	0.012	84	0.393	78	15.7
2.000	0.603	-108	5.5	162	0.013	81	0.428	69	14.8

ICs

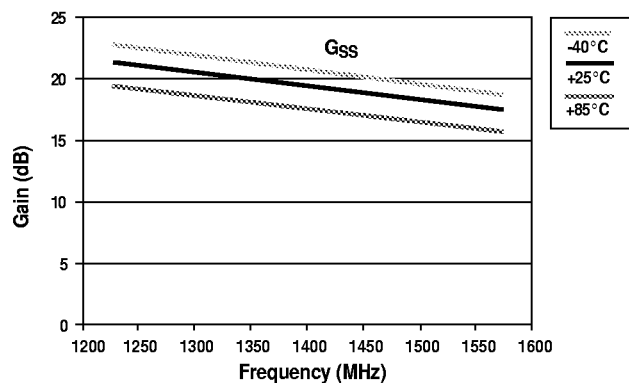
Noise Parameters (typical)

Frequency (MHz)	F_{MIN} dB	Gamma-Opt		Electrical Length ($Z_0 = 75\ \Omega$)		
		Mag.	Angle	R_Noise	T_1 (Degrees)	T_2 (Degrees)
1227	1.26	0.535	39.5	27.7	42.9	38.0
1575	1.26	0.433	60.1	25.0	47.6	23.3

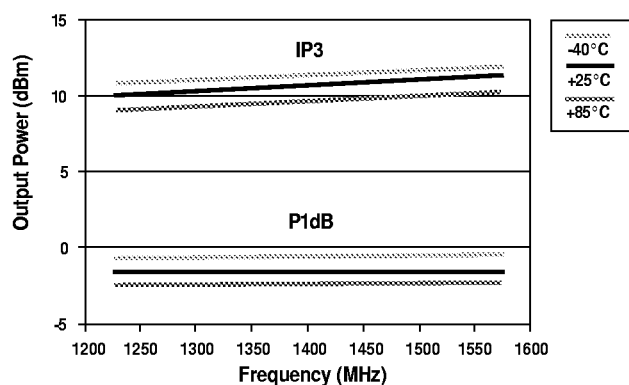
**Input and Output Impedance
(w/o external matching)****Gamma Optimum**

Typical Performance

Gain vs. Frequency vs. Temperature

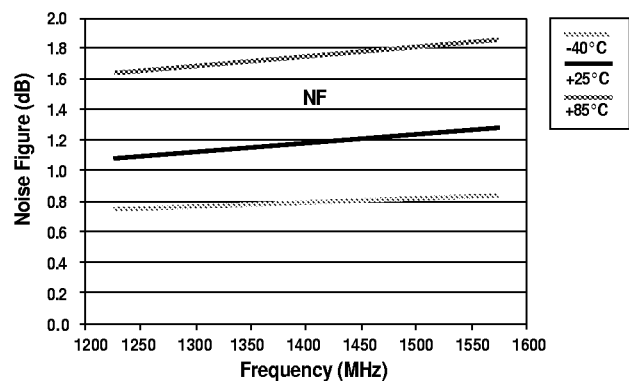


P1dB and IP3 vs. Frequency vs. Temperature



NF vs. Frequency vs. Temperature

(with external matching)

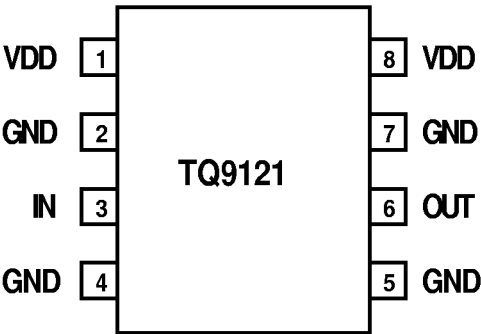


Pin Descriptions

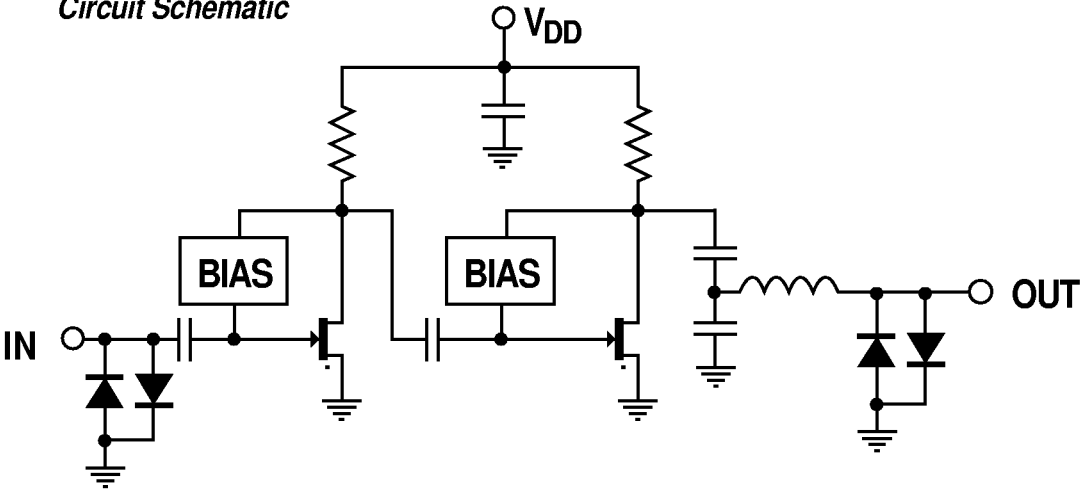
Name	Pin #	Description
V _{DD}	1, 8	+5 V Power Supply. Decoupled on chip with 50 pF capacitor. If additional decoupling is required, decouple with 0.01 uF within 0.25 inch of package. Pins 1 and 8 are connected internally.
IN	3	Input has ESD-protection diodes internal to the die. Internal DC bias is isolated from the input port. An external DC block may therefore be required for some circuit applications where DC voltages are present, to stop current flow into the ESD diodes from the external circuit. Optimum noise figure requires an external matching network.
OUT	6	Output also has ESD protection diodes internal to the die. (See the note above regarding bias isolation and external DC block requirements.)
GND	2,4,5,7	Ground connection. Keep physically short for stability and performance. Pins are internally connected.

Note: Refer to block diagram for pin location

TQ9121 Pinout



Circuit Schematic



ICs

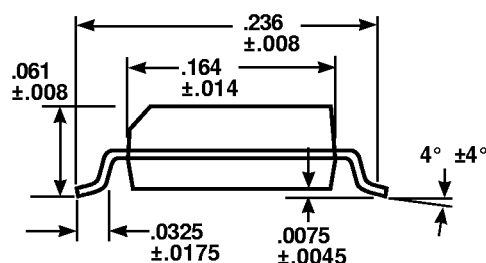
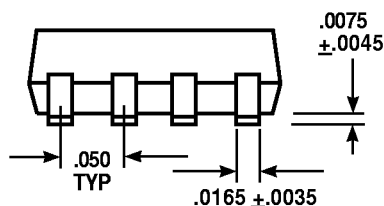
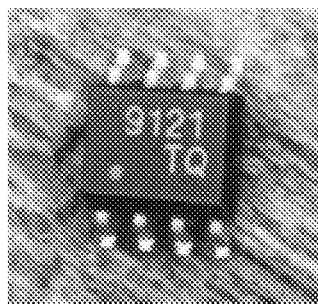
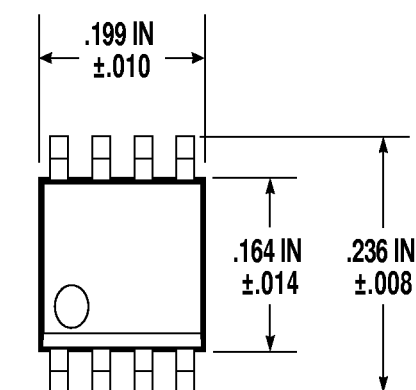
TQ9121

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
DC Power Supply			7	V
Power Dissipation			140	mW
Input Power			+10	dBm
Storage Temperature	-55		+150	°C
Operating Temperature	-40		+85	°C

Note: ESD-sensitive device - Class 1

SO-8 Plastic Package



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