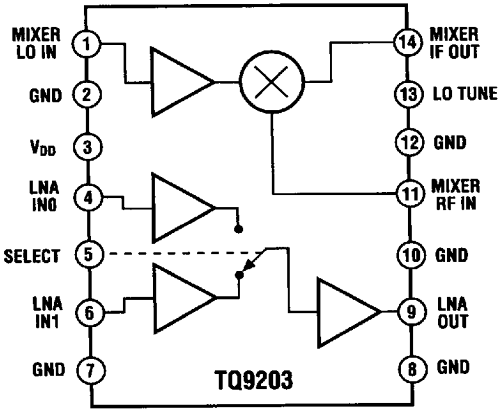
TQ9203

Low-Current Cellular-Band Downconverter IC



The TQ9203 RFIC Downconverter is a multifunction RF front end designed for the high dynamic range cellular communications standards. The design of the TQ9203 provides a 2.5 dB system noise figure for excellent sensitivity, and a good signal range with -10 dBm input IP3. Its low current consumption, single +5 V operation and small, plastic surface-mount package are ideally suited for cost-competitive, space-limited and portable applications. In addition, two selectable RF inputs simplify implementation of "antenna diversity" in applications such as CDPD. The TQ9203 is specified over an RF frequency range of 800 to 1000 MHz, and therefore may be used for any of the cellular and cordless telephony standards.

Features

- + 5 V single supply
- Internal buffer amplifier on mixer LO port
- On-chip matching to 50 Ω
- Two selectable RF inputs
- Low-cost SO-14 plastic package
- 21 dB system gain
- -10 dBm typical input intercept point
- 2.5 dB typ. system noise figure
- 10.5 mA typ. operating current

Applications

- Cellular Communications
- Spread-Spectrum Receivers
- Cordless Phones

Electrical Specifications

Test Conditions: V_{DD} = 5 V, T_A = 25°C, RF = 881 MHz, LO = 966 MHz

Parameter (1)	Min.	Typ.	Max.	Units
Conversion Gain	18	21		dB
Noise Figure (2)		2.5	3.0	dB
Input 3rd Order Intercept (3)		-10		dBm
Supply Voltage	4.5	5.0	5.5	V
Supply Current		10.5	12.0	mA

Notes: 1. Min/Max values listed are production tested
2. Specified with external noise-matching circuit elements, with image-stripping BPF; IL = 3 dB.
3. Frequency separation of the two signals is 500 KHz; BPF IL = 3 dB.

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Electrical Specifications – Downconverter

Test Conditions: V_{DD} = 5 V, T_A = 25 °C, RF = 881 MHz, LO = 966 MHz, BPF Filter IL = 2 dB

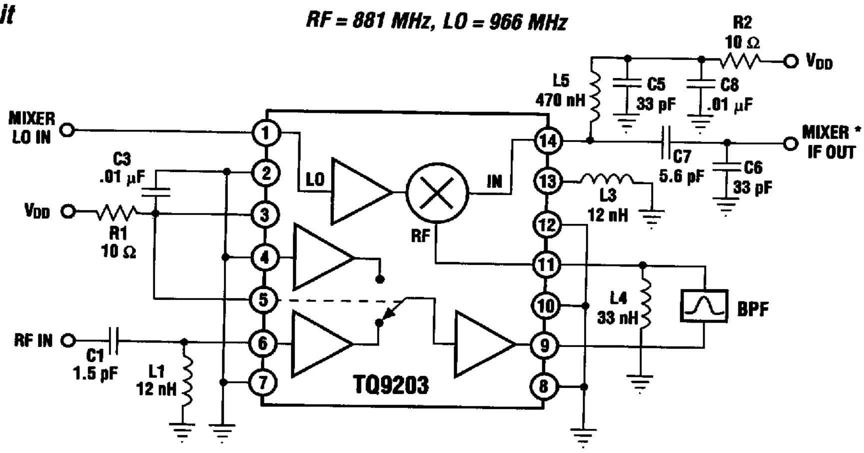
Parameter	Conditions	Min	Typ	Max	Units
RF Frequency		800		1000	MHz
LO Frequency		700		1300	MHz
IF Frequency		30		300	MHz

Parameter	Conditions	Min	Typ	Max	Units
Conversion Gain (1)	LO = -6 dBm, RF = -35 dBm	18	21		dB
Noise Figure (2)	LNA IN0 Pin; SSB		2.8	3.3	dB
Noise Figure (2)	LNA IN1 Pin; SSB		2.5	3.0	dB
Input 3rd Order Intercept	Frequency Sep. = 500 KHz		-10		dBm
MIXER RF Return Loss			10		dB
MIXER LO Return Loss			10		dB
LNA OUT Return Loss			20		dB
LO Input Power			-6		dB
Supply Voltage		4.5	5.0	5.5	V
Supply Current @ 5 V			10.5		mA

Notes: 1. Conversion gain, noise figure, and IP3 assume an image stripping band-pass filter between the LNA section and the Mixer section with a 3 dB insertion loss.
2. With optimum noise match, which results in approximately 12 dB return loss at the input port. G_{OPT} : |G| = 0.7, <G = 31°.

Test Circuit

RF = 881 MHz, LO = 966 MHz



** Component values for L5, C6, and C7 depend upon the IF frequency and the IF filter impedance. R1 and R2 are optional. Here they are chosen for an 85 MHz IF and 50W load.*

Electrical Specifications – LNA Section

Test Conditions: V_{DD} = 5 V, T_A = 25 °C, RF = 881 MHz

Parameter	Conditions	Min.	Typ.	Max.	Units
Gain	RF = -40 dBm		18		dB
Noise Figure (1)	LNA_0 Active		2.1		dB
Noise Figure (1)	LNA_1 Active		1.8		dB
Output 3rd Order Intercept	Separation: 500 KHz		+13		dBm
Output Gain Compression			1.5		dBm
Reverse Isolation			38		dB
Off Isolation, LNA In1/Out	Select = 0 V, LNA_0 On		-7		dB
Off Isolation, LNA In0/Out	Select = 5 V, LNA_1 On		-5		dB
Supply Voltage		4.5	5.0	5.5	V
Supply Current	Mixer Off (2) Powered down		8.8		mA

Notes: 1. With optimum noise match, which results in approximately 12 dB return loss at the input port. Γ_{OPT} : $|\Gamma|$ = 0.7, $<\Gamma$ = 31°.
2. V_{DD} pin supplies current to both the LNA and the LO buffer amps. Mixer cannot operate without V_{DD} connection.
Mixer V_{DD} through the IF pin connects only to the mixer FET.

Electrical Specifications – Mixer Section

Test Conditions: V_{DD} = 5 V, T_A = 25 °C, LO Power Level = -6 dBm, IF = 85 MHz, RF = 881 MHz, LO = 966 MHz (Includes Image Filter)

Parameter	Conditions	Min.	Typ.	Max.	Units
Conversion Gain	RF Power = -20 dBm		4.0		dB
Noise Figure			11.0		dB
3rd Order Intercept – Input	Separation = 500 KHz		+8.5		dBm
Isolation RF/IF			43		dB
Isolation LO/IF	Matching elements used in the test circuit		41		dB
Isolation LO/RF			5.0		dB
Supply Voltage		4.5	5.0	5.5	V
Supply Current @ 5 V	LNA Off (1) Powered down		1.6		mA

Notes: 1. V_{DD} pin supplies current to both the LNA and the LO buffer amps. Mixer cannot operate without V_{DD} connection.

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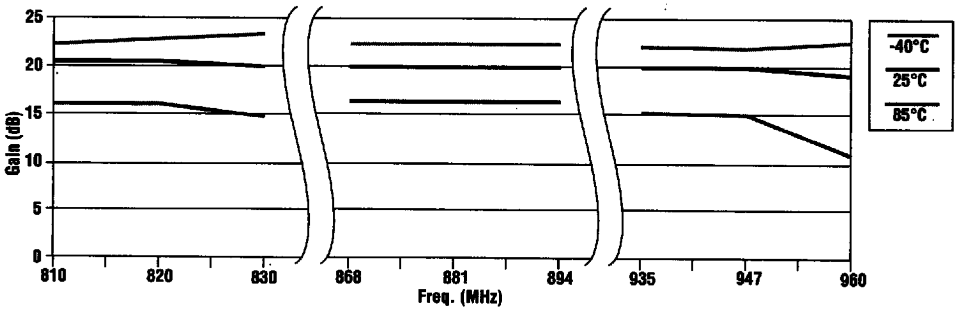
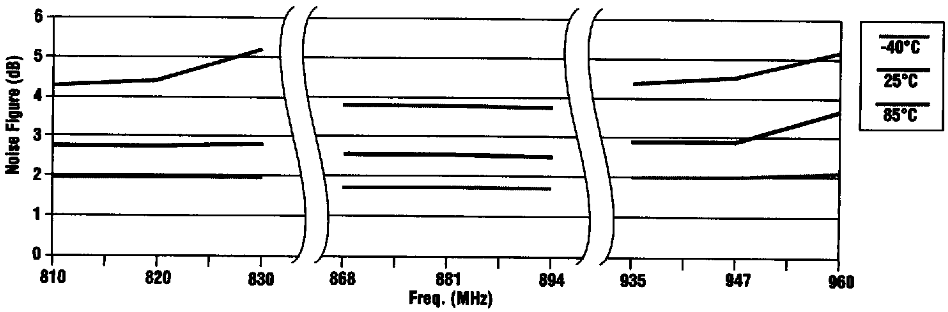
Typical Performance – Downconverter

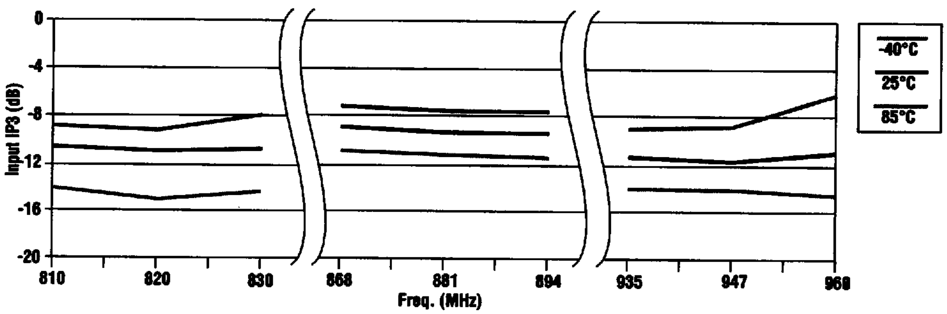
Conversion Gain vs. Frequency vs. Temperature



NF vs. Frequency vs. Temperature



Input IP_3 vs. Frequency vs. Temperature



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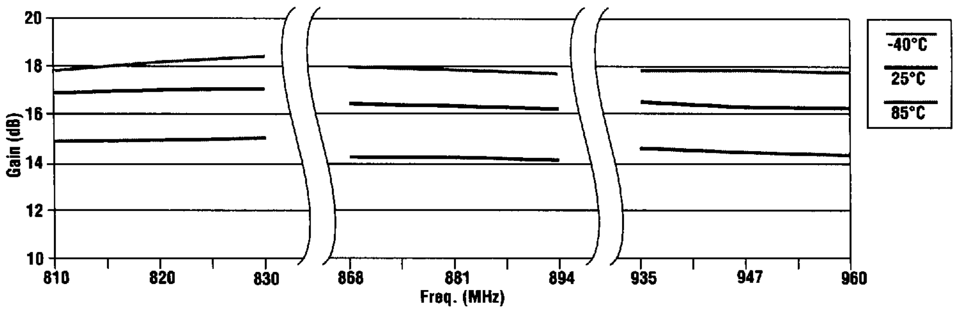
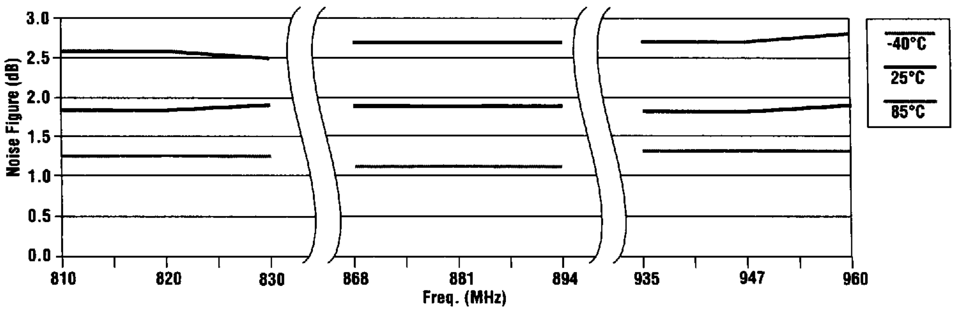
Typical Performance – LNA

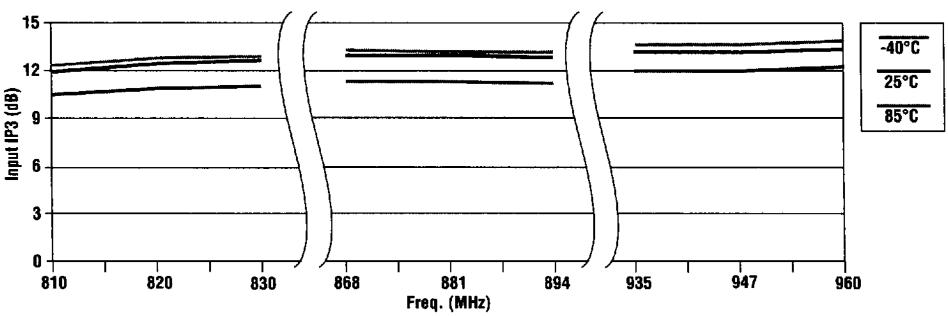
Gain vs. Frequency vs. Temperature



NF vs. Frequency vs. Temperature



IP_3 vs. Frequency vs. Temperature



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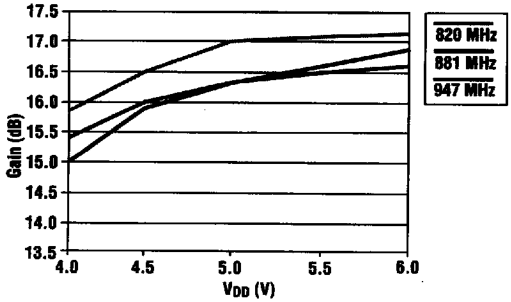
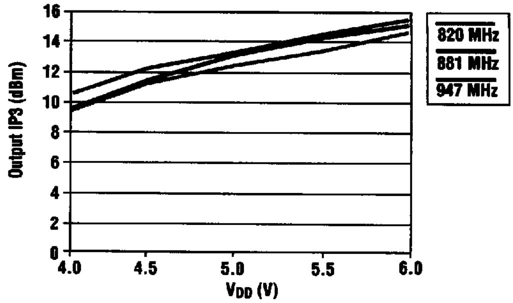
Typical Performance – LNA

Gain vs. V_{DD} vs. Frequency

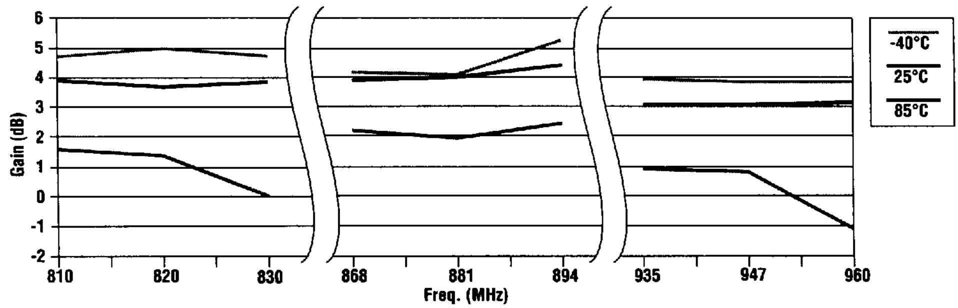


IP_3 vs. V_{DD} vs. Frequency

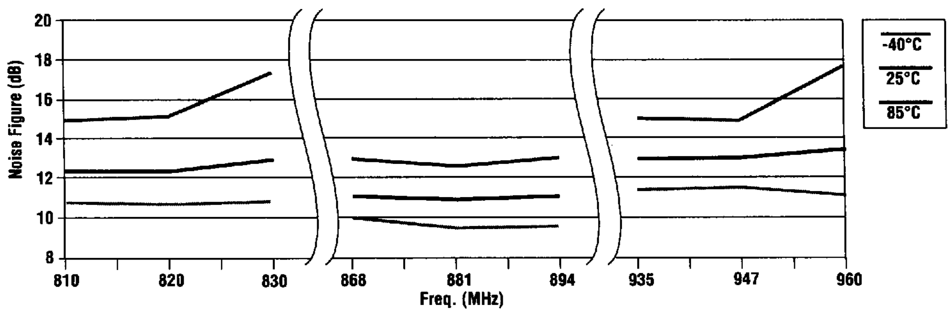


Typical Performance – Mixer

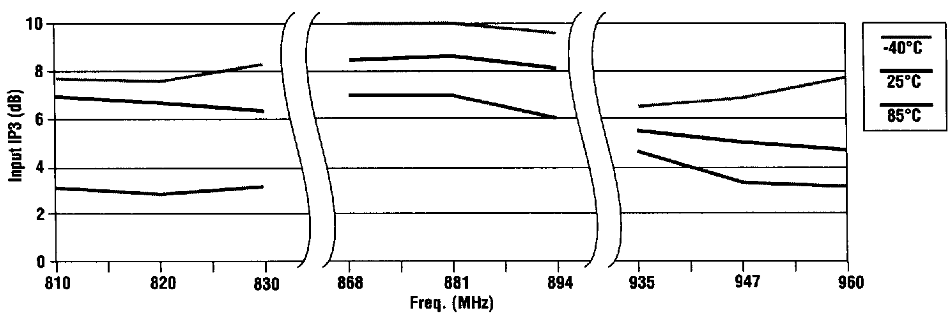
Gain vs. Frequency vs. Temperature



NF vs. Frequency vs. Temperature



IP_3 vs. Frequency vs. Temperature



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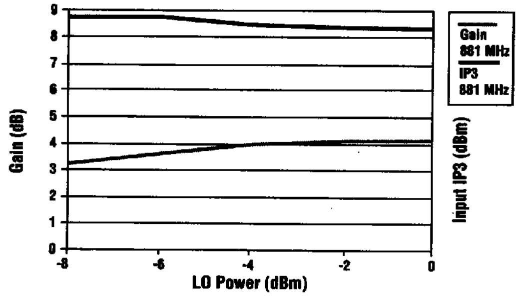
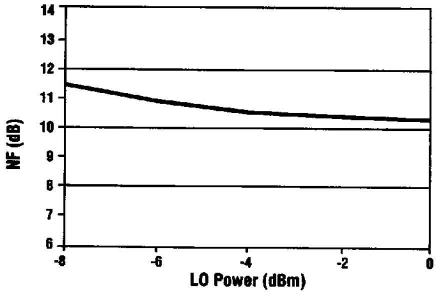
Typical Performance – Mixer

Gain and Input IP3 vs. LO Power



NF vs. LO Power



LNA_0 S-Parameters (typical)

Freq (MHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
800	0.76	-39	4.30	4	0.0033	-161	0.25	-110
825	0.75	-40	4.42	-2	0.0034	-158	0.16	-120
850	0.74	-41	4.50	-8	0.0038	-160	0.10	-138
875	0.73	-42	4.54	-13	0.0044	-164	0.05	167
900	0.72	-43	4.58	-22	0.0047	-170	0.07	93
925	0.71	-43	4.57	-28	0.0051	-174	0.12	75
950	0.71	-44	4.53	-34	0.0054	-178	0.18	60
975	0.70	-46	4.50	-38	0.0056	178	0.23	52
1000	0.70	-47	4.43	-45	0.0062	174	0.29	47

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LNA_1 S-Parameters (typical)

Freq (MHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
800	0.82	-40	4.55	17	0.0058	171	0.30	-94
825	0.82	-41	4.70	10	0.0061	166	0.23	-98
850	0.82	-42	4.82	4	0.0067	161	0.16	-100
875	0.81	-43	4.92	-2	0.0069	156	0.09	-99
900	0.81	-45	4.97	-8	0.0075	151	0.03	-69
925	0.80	-46	5.00	-13	0.0078	150	0.05	24
950	0.80	-47	4.99	-19	0.0079	145	0.11	37
975	0.79	-48	4.97	-24	0.0078	142	0.16	37
1000	0.79	-49	4.94	-29	0.0085	142	0.21	36

LNA_0 Noise Parameters (typical)

Frequency (MHz)	F_{MIN} (dB)	Γ_{OPT} (Mag)	Γ_{OPT} (Ang)	R_{NOISE} (Ω)
820	1.51	0.65	26.5	40.1
881	1.54	0.65	29.0	40.0
915	1.57	0.64	30.5	39.9
947	1.60	0.64	32.0	39.9

LNA_1 Noise Parameters (typical)

Frequency (MHz)	F_{MIN} (dB)	Γ_{OPT} (Mag)	Γ_{OPT} (Ang)	R_{NOISE} (Ω)
820	1.30	0.67	27.4	38.9
881	1.33	0.66	30.4	39.9
915	1.36	0.66	31.5	39.9
947	1.39	0.66	32.7	38.7

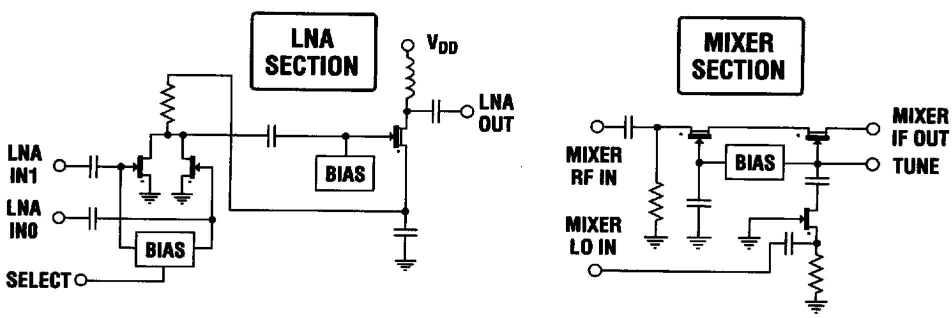
Mixer S-Parameters (typical)

Freq	Mixer RF IN /S11/	Mixer RF IN <S11	Mixer LO IN /S11/	Mixer LO IN <S11
700	0.36	-42	0.21	-48
750	0.36	-45	0.19	-44
800	0.35	-45	0.17	-40
850	0.34	-46	0.15	-33
900	0.33	-47	0.13	-14
950	0.34	-45	0.17	6
1000	0.40	-47	0.26	0
1050	0.39	-56	0.33	-23
1100	0.39	-60	0.31	-37

Mixer S-Parameters (typical)

Freq	IF OUT /S11/	IF OUT <S11
50	0.993	-2
75	0.991	-2
100	0.991	-2
125	0.994	-3
150	0.995	-4
175	0.995	-4
200	0.994	-5
225	0.994	-5
250	0.994	-6

Simplified Circuit Schematic

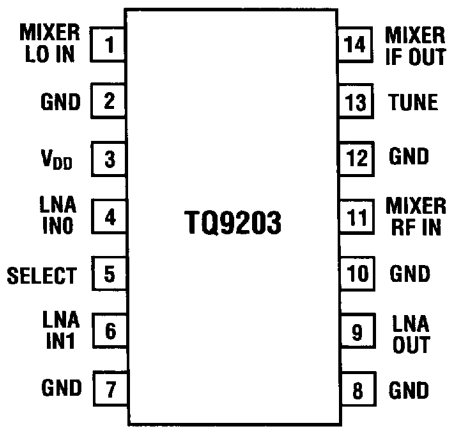


Pin Descriptions

Pin Name	Pin #	Description
LNA IN1	6	LNA IN1 is the primary input port. Best performance is achieved with external noise-matching network. Internally DC blocked.
SELECT	5	Input port selection switch. CMOS-compatible drive, switches input ports from LNA IN1 to LNA IN0. Low = IN0, High = IN1.
LNA IN0	4	LNA IN0 is an auxiliary input and has characteristics similar to the LNA IN1 input port. Best performance is achieved with external noise-matching network. Internally DC blocked.
LNA OUT	9	Output port from switched LNA section. Internally matched to 50 Ω. Internally DC blocked.
MIXER RF IN	11	Mixer RF signal input port. Image stripping band pass filtering before Mixer section improves noise and spurious performance. No return to ground is required. Shunt L recommended for IF suppression.
MIXER IF OUT	14	Mixer IF signal output port. Open "collector-" type output requires impedance matching to desired load impedance, connected to VDD supply.
MIXER LO IN	1	Buffered LO port. There is an internal DC block on this port, which is matched to 50 Ω.
VDD	3	Supply voltage for bias circuitry and LNA. This pin draws 8 mA, typically. Decouple with 0.01 μF within 0.25 inch of package.
GND	2, 7, 8, 10, 12	Ground connection. Keep physically short for stability and performance. Several via holes to ground plane.
TUNE	13	LO Buffer tuning, inductor to ground.

Note: Refer to block diagram for pin location

TQ9203 Pinout



General Description

The TQ9203 efficiently integrates a low-noise amplifier and high-intercept mixer, with performance equal to a discrete implementation, through use of circuit techniques from monolithic and discrete design practices. The LNA consists of two cascaded common-source amplifier stages, using a "DC-stacked" topology, in which the same DC current flows through both stages. An external noise match is used to achieve optimum noise figure. Matching is performed with PC board microstrip lines or lumped-element surface-mount components, using simple, well understood networks. The output on-chip impedance is matched to 50 ohms.

The mixer is implemented as a "cascode" stage operating like a dual-gate FET mixer. A common-gate LO buffer provides the necessary gain to drive the mixer FET gate and establishes a good input match. The on-chip buffer amplifier allows for direct connection to a commercial VCO at drive levels down to -6 dBm. An "open collector" IF output allows for flexibility, matching to various IFs and filter types.

The two topologies efficiently use the supply current for low-power operation, approximately 10 mA with a 5 V supply. The overall circuit provides a distinct performance edge over silicon monolithic designs in terms of input intercept, noise figure and gain. Specifically, the circuit was intended for use in the following applications: cellular (AMPS, NADC, GSM, JDC, ETACS, etc.) and ISM band (902 - 928 MHz).

In addition, two selectable LNA inputs are available. They are implemented through the use of two independent first stages, each connected to the second-stage input. A SELECT pin controls which input is active by steering the current through the selected input stage and cutting it off from the other. This provides the optional functionality of a diversity switch in front of the LNA, but without the insertion loss and noise figure penalty from the switch.

Power Supply Connection

The TQ9203 was designed to operate within specifications over the power supply range of 4.5 to 5.5 V, although it will function over a range of 4.0 to 6.0 V. The internal biasing maintains stable operating points with varying supply voltage. However, the electrical parameters do vary slightly with supply voltage.

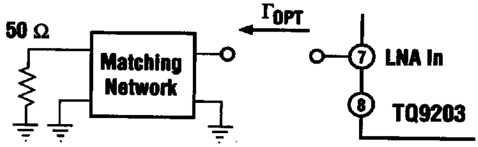
Internally, the downconverter has 50 pF of capacitance from V_{DD} to ground for RF decoupling of the supply line. This should be augmented with additional decoupling capacitance: 1000 pF connected externally within 5 mm of the package pin. A 10-ohm series resistor in the V_{DD} line may also be added (optionally) to provide some filtering of supply line noise. Connections to ground should go directly to a low-impedance ground plane. Therefore, it is recommended that multiple via holes to the ground plane occur within 2 mm on the inside of the package pins .

LNA Input Interfacing

The TQ9203 LNA was designed for low-noise operation. It makes use of an optimum noise-matching network at the input, not a conjugate match, as would be used for maximum power transfer (although gamma optimum is near the conjugate match). Gamma optimum is referenced from the LNA input into the noise-match network in series with 50 ohms. The gamma optimum and the noise parameters for selected frequencies are shown in the LNA Noise Parameters table.

There are several options for the physical realization of gamma optimum: a series-shunt microstrip transmission line network, a series capacitor/shunt inductor, and a series inductor. Ideal values for these components are included in the Noise Parameters table. The microstrip transmission lines can easily be constructed on FR-4 or G-10 circuit boards, using standard design techniques. The lumped-element components are surface-mount elements designed for RF use. Slight adjustments in the actual values of the elements are likely, due to the effects of component parasitics. It is important that the board-level circuit establishes an impedance of gamma optimum, measured at the solder pad of pin 6. Proper board design for gamma optimum eliminates the need for tuning adjustments and produces a low-noise circuit which is tolerant of component variations.

LNA Impedance Matching



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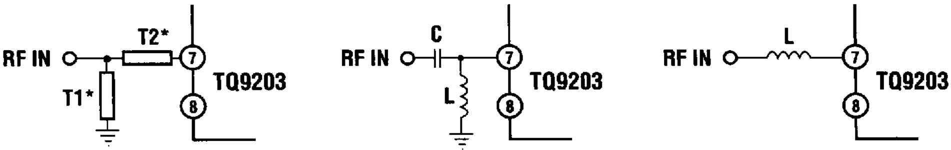
Possible Matching Networks



LNA Output

The LNA output is internally matched to 50 ohms over the 800 to 1000 MHz frequency band and it is internally DC-blocked. Therefore, direct connections may be made to pin 9.

Mixer RF Input

The mixer RF input is matched close to 50 ohms and is internally DC-blocked. Pin 11 may be directly connected to the filter output. The filter must be as close as possible to the mixer RF input to maintain the proper termination impedance at the LO frequency. Include a shunt inductor of 22 nH at the mixer RF input to improve the mixer noise performance by providing a short to ground at the IF frequency. This provides a secondary benefit of slightly improved input match.

Mixer LO Input

The mixer LO input is matched close to 50 ohms and is internally DC-blocked. Pin 1 may be directly connected to the LO input signal. A level greater than -6 dBm is recommended. Standard VCO outputs of -2 dBm work well.

LO Tuning (Pin 13)

A shunt L on pin 13 resonates with some internal capacitance to produce a bandpass frequency response of the LO buffer amplifier. This attenuates noise at $\pm$ one IF frequency away from the LO frequency. The approximate value of L is determined by the following equation:

$$L = \frac{1}{C(2\pi f)^2}\text{, where } C = 2.2\text{ pF}$$

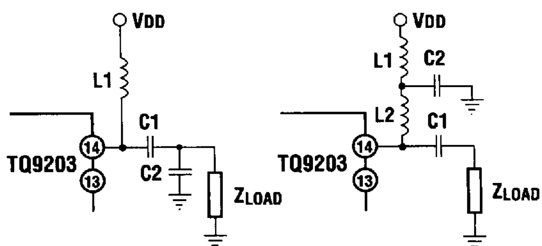
In practice, the value (and/or placement) of L should be empirically determined for a particular layout, since stray capacitance on the PCB layout can move the resident frequency from the expected ideal. The actual value of L should be adjusted until the buffer response (pin 1 -> pin 13) produces a peak at the LO frequency. A measurement of the response may be accomplished with a simple coaxial probe "sniffer," in which the end is positioned 50 -100 mils from the inductor at pin 13. The frequency response of the LO buffer amplifier (pin 13) is directly measured on a network analyzer as the LO input (pin 1) is swept in frequency. The LO drive level should be set at approximately the operating level (-6 to -3 dBm) for this measurement. This "tuning" needs to be done only in design, not in production.

Mixer IF Interfacing

The mixer IF port is a high-impedance, open-drain output. The impedance is a few K ohms in parallel with less than 1 pF capacitance. The IF port S-parameters (S11) are listed in the table over the frequency range of 45 MHz to 250 MHz. It is possible to use IFs above and below this range; however, at low frequencies the noise increases, and at high frequencies the LO/IF, RF/IF isolation decreases.

The open-drain output permits matching to any chosen filter impedance. In general, a conjugate impedance match is recommended on this port to achieve best power gain, noise figure and output 3rd-order intercept. It is also important to properly center the tuned circuit at the desired IF. This maximizes circuit robustness to component tolerances. For proper mixer operation, pin 14, the open-drain output, must also be biased to V_{DD}. Two practical matching networks which include biasing are shown below:

Mixer IF Interfaces



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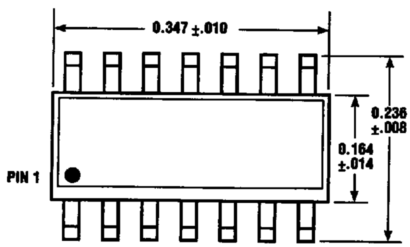
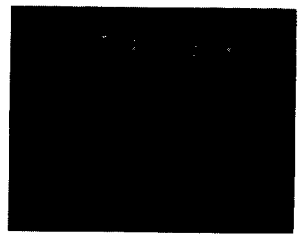
Absolute Maximum Ratings

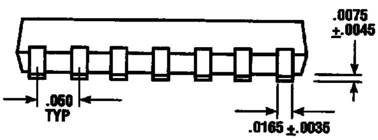
Parameter	Min.	Typ.	Max.	Units
DC Power Supply			8	V
Power Dissipation			120	mW
Input Power (All Ports)			+10	dBm
Storage Temperature	-55		+150	°C
Operating Temperature	-40		+ 85	°C

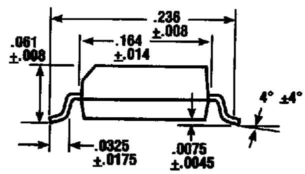
ESD-sensitive device - Class 1

SO-14 Plastic Package
(J Suffix)









TriQuint SEMICONDUCTOR

Revision E.2, July 12, 1997

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