TriTech Microelectronics

TR88200CG

ADPCM CODEC

General Description

The TriTech TR88200 ADPCM CODEC is a low power, full duplex telephony CODEC with integrated ADPCM compression and decompression. A tone generator and voice/silence detection circuit are also integrated.

The TR88200 includes three compression algorithms for 32, 24 and 16kbps. Voice data may also be coded as 64kbps μ or A-law PCM samples. Several master clock options are provided to offer compatibility with DECT, PHS and other systems

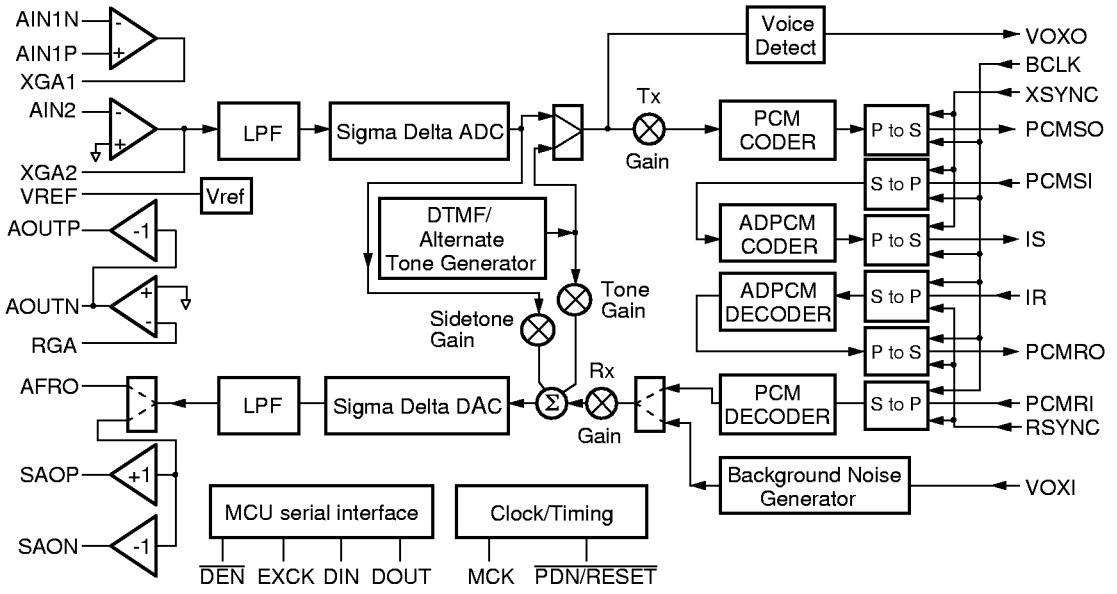
Applications

- Digital Cordless Phones
- Voice Recorders
- Digital Corded Phones
- PABXs
- Pair-Gain Applications

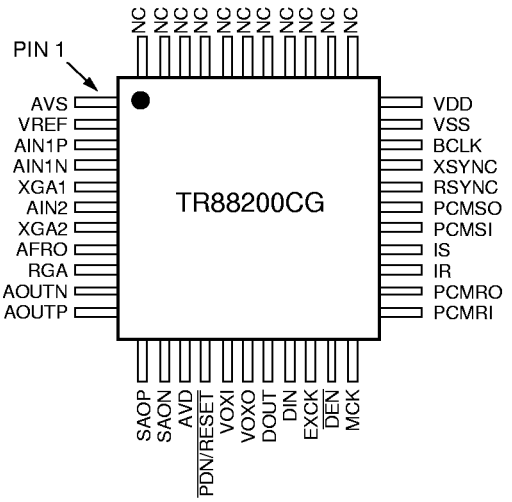
Features

- Single 2.7V to 3.6V power supply
- ADPCM Algorithms – G.721 (32kbps), G.723 (24kbps) G.726 (16kbps). G.711-PCM
- Master Clock Frequencies – 10.368, 12.288 or 19.200 MHz selectable
- Built in DTMF transmitter with various single tone options
- Built in VOX control, voice detect and background noise generation
- Built in microphone amplifier and sounder driver
- Programmable transmit, receive and sidetone gain controls
- Low power CMOS
- 44-pin LQFP package

Block Diagram



Pin Configuration



44-pin LQFP (top view)

Pin Descriptions

Pin	Name	I/O	Function
1	AVS	–	Analog ground
2	VREF	AO	On chip signal ground. Connect 10μF and 0.1μF in parallel to AVS.
3	AIN1P	AI	Differential amplifier non-inverting input
4	AIN1N	AI	Differential amplifier inverting input
5	XGA1	AO	Differential amplifier gain control
6	AIN2	AI	Single ended input amplifier inverting input.
7	XGA2	AO	Single ended amplifier gain control
8	AFRO	AO	Receive filter output
9	RGA	AI	Receive gain adjustment
10	AOUTN	AO	Differential analog output negative
11	AOUTP	AO	Differential analog output positive
12	SAOP	AO	Sounder differential output positive
13	SAON	AO	Sounder differential output negative
14	AVD	–	Analog supply voltage
15	$\overline{\text{PDN/RESET}}$	DI	Power down and reset. Control registers are reset to initial states. The power down state is controlled as a logical OR with control bit CR0-B5.
16	VOXI	DI	Logic control for receive voice detection. A “0” at this pin will generate background noise into the receive path if control bit CR6-B3 is set to “0”. The background noise amplitude is set by CR6.
17	VOXO	DO	Voice detection logic output signal. The “1” and “0” levels indicate the presence, or absence, of the transmit voice signal. The detection threshold is set by CR6-B6,B5.

Pin Descriptions (continued)

Pin	Name	I/O	Function
18	DOUT	DO	Serial data output
19	DIN	DI	Serial data input
20	EXCK	DI	Data shift clock input
21	$\overline{\text{DEN}}$	DI	Data enable signal input
22	MCK	DI	Master Clock. Three clock frequencies (10.368, 12.288, 19.200MHz) are selectable from CR0.
23	PCMRI	DI	PCM serial data receive input. PCM is shifted on the rising edge of BCLK, MSB first.
24	PCMRO	DO	PCM serial data receive output after ADPCM processing. The data is MSB first, synchronised to RSYNC and the rising edge of BCLK.
25	IR	DI	Receive ADPCM signal input. The data is MSB first, synchronised to RSYNC and the rising edge of BCLK.
26	IS	DO	Transmit ADPCM signal output. Post ADPCM encoded data, MSB first, synchronised to XSYNC and the rising edge of BCLK.
27	PCMSI	DI	Transmit PCM serial input. Normally connected to PCMSO.
28	PCMSO	DO	Transmit PCM serial output. PCM coded serial data, MSB first synchronized with XSYNC and rising edge of BCLK.
29	RSYNC	DI	Receive PCM and ADPCM data synchronous serial input. Indicates the MSB of the receive PCM or ADPCM stream.
30	XSYNC	DI	Transmit PCM and ADPCM data 8kHz synchronous signal input. Indicates the MSB of the transmit PCM or ADPCM stream.
31	BCLK	DI	Shift clock input for the PCM data (PCMSO, PCMSI, PCMRO, PCMRI) and ADPCM (IS, IR) data. The frequency can be in the 64kHz to 2048kHz range.
32	VSS	–	Digital ground
33	VDD	–	Digital Power supply
34-44	NC	–	Do not connect.

Circuit Description

The analog inputs and outputs of the TR88200 are designed to provide flexibility for use with different telecom systems. Figure 1 below shows the typical connections and calculations required to adapt the circuit to other applications.

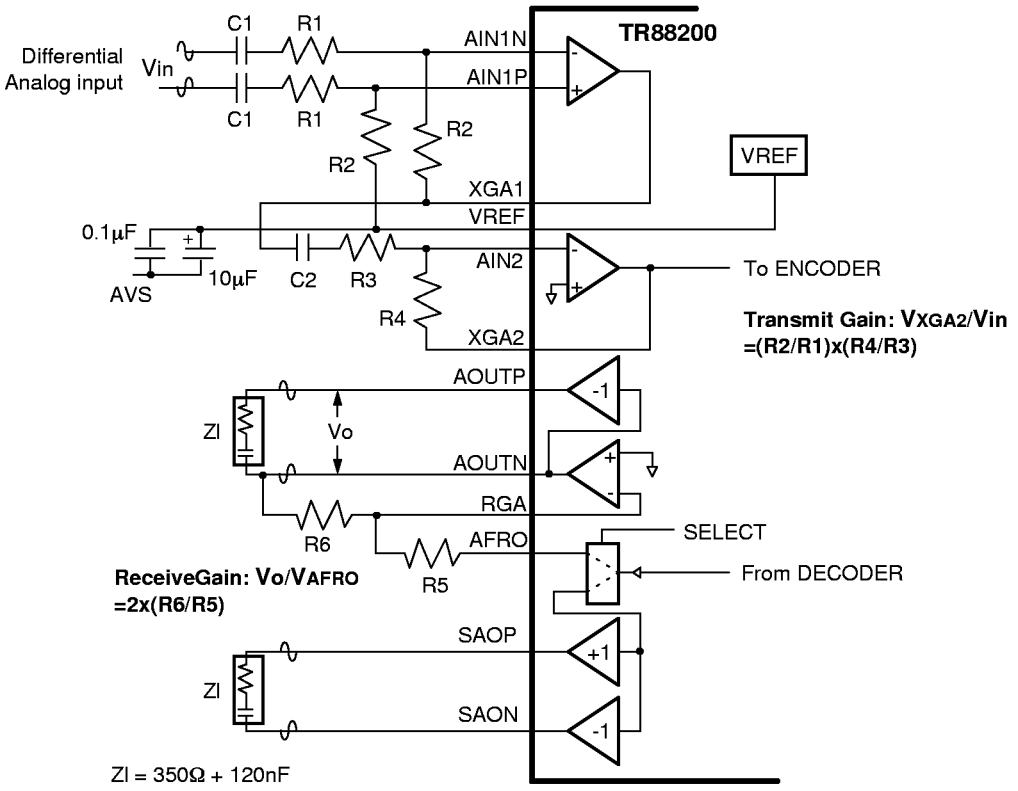


Figure 1 • *Analog inputs and outputs*

Note: Throughout this data sheet, transmit path refers to the upper portion of block diagram (with the ADC) and the Receive path refers to the lower position (with DAC).

MCU Serial Interface

Figure 2 shows the timing for the serial MCU interface to the eight control registers in the TR88200.

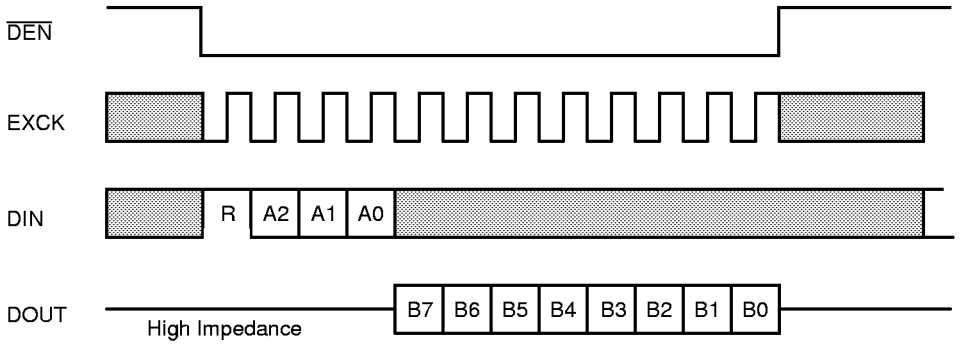


Figure 2 • *MCU read interface*

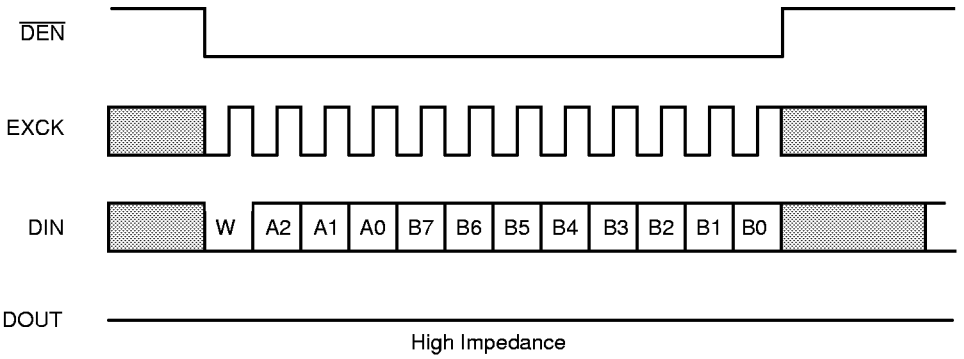


Figure 3 • *MCU write interface*

Control Registers

The control registers are defined below. All control registers are set to their default state upon a hardware reset (PDN/RESET). Initial values after reset are all zero's except for some bits of CR2. Reserved or unused bits of Control registers should be set to 0.

Table 1. *Control Register Index*

	ADDRESS			CONTROL AND DETECT DATA								
Name	**A2**	**A1**	**A0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**R/W**
CR0	0	0	0	A/μ SEL	MCK SEL0	PDN ALL	PDN TX	PDN RX	MCK SEL1	–	PDN SAO/ AOUT	R/W
CR1	0	0	1	MODE1	MODE0	RESET	–	–	–	–	RX PAD	R/W
CR2	0	1	0	TX ON/ OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/ OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ ALT SEL	TONE SEND	SAO/ AFRO	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR5	1	0	1	-	PCM RX MUTE	PCM TX MUTE	Factory Test modes					R/W
CR6	1	1	0	VOX ON/ OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LVL SEL	RX NOISE LVL1	RX NOISE LVL0	R/W
CR7	1	1	1	–	–	–	Factory Test modes					R

Control Register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A/μ SEL	MCK SEL0	PDN ALL	PDN TX	PDN RX	MCK SEL1	–	PDN SAO/ AOUT

CR0-B0 1 = Power down for sound amplifier outputs or receiver amplifiers depending on state of CR4-B5. (0 = power on).

CR0-B0	CR4-B5	
0	0	SA Mute, RA active
0	1	SA active, RA mute
1	0	SA powerdown, RA active
1	1	SA active, RA powerdown

SA – Sounder amplifier
RA – Receive amplifier

CR0-B1 Reserved. Normally zero.
CR0-B2,B6 Master clock frequency selection

MCK sel1	MCK sel0	Frequency
0	0	12.288MHz
0	1	19.200MHz
1	X	10.368MHz

CR0-B3 1 = Power down for receive only. 0= power on.
CR0-B4 1 = Power down for transmit only. 0= power on.
CR0-B5 1 = Power down for whole system. 0= power on. When using this data for power down controll set $\overline{\text{PDN/RESET}}$=1. The control registers are not reset by CR0-B5.
CR0-B7 PCM mode select. 1=A-law, 0=μ-law.

Control Register 1 (ADPCM Coder/Decoder Settings)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MODE1	MODE0	RESET	–	–	–	–	RX PAD

CR1-B0 1= Analog O/P attenuated by 12dB.
CR1-B1 Reserved
CR1-B2 Reserved
CR1-B3 Reserved
CR1-B4 Reserved
CR1-B5 1=ADPCM reset
CR1-B6,B7 ADPCM algorithm selection

MODE1	MODE0	Algorithm
0	0	32kbps (G.721)
0	1	64kbps (G.711)
1	0	24kbps (G.723)
1	1	16kbps (G.726)

Control Register 2 PCM Block & Tx-Rx Gain Control Settings

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
0	0	1	1	0	0	1	1

NOTE: Last row above, shows bit values after reset.

CR2-B0-B2 Receive gain adjustment see table below.
CR2-B3 1=Disable PCM decoder (receive PCM idle pattern). 0= enable.
CR2-B4-B6 Transmit gain adjustment see table below.
CR2-B7 1=Disable PCM coder (transmit PCM idle pattern). 0= enable.

B6	B5	B4	Transmit gain	B2	B1	B0	Receive gain
0	0	0	-6dB	0	0	0	-6dB
0	0	1	-4dB	0	0	1	-4dB
0	1	0	-2dB	0	1	0	-2dB
0	1	1	0dB	0	1	1	0dB
1	0	0	+2dB	1	0	0	+2dB
1	0	1	+4dB	1	0	1	+4dB
1	1	0	+6dB	1	1	0	+6dB
1	1	1	+8dB	1	1	1	+8dB

The output of the DTMF tone generator is -16dBmO for low group tones and -14dBmO for the high group and alternative tones. The gain shown above must be added to these levels to calculate the amplitude of the final output signal. For example if the +4dB setting is selected, the DTMF output at PCMSO will be equivalent to -12dBmO for the low group and -10dBmO for the high group. This applies to transmitted tones.

Control Register 3 (Side Tone and Tone Generator Controls)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/ OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0

CR3-B0-B3 Tone generator gain adjustment for receive side. See table below.

B3	B2	B1	B0	Tone generator RX gain	B3	B2	B1	B0	Tone generator RX gain
0	0	0	0	-36dB	1	0	0	0	-20dB
0	0	0	1	-34dB	1	0	0	1	--18dB
0	0	1	0	-32dB	1	0	1	0	-16dB
0	0	1	1	-30dB	1	0	1	1	-14dB
0	1	0	0	-28dB	1	1	0	0	-12dB
0	1	0	1	-26dB	1	1	0	1	-10dB
0	1	1	0	-24dB	1	1	1	0	-8dB
0	1	1	1	-22dB	1	1	1	1	-6dB

The output of the DTMF tone generator is -2dBmO for low group tones and 0dBmO for the high group and alternative tones. The gain shown above must be added to these levels to calculate the amplitude of the final output signal. For example if the -14dB setting is selected, the DTMF output at SAOP/SAON or AFRO will be -14dBmO for the high group and -16dBmO for the low group.

CR3-B4 1=Tone generator enable. 0=disable.
CR3-B5-B7 Side tone gain setting. See table below.

B7	B6	B5	Side tone path gain
0	0	0	off
0	0	1	-21dB
0	1	0	-19dB
0	1	1	-17dB
1	0	0	-15dB
1	0	1	-13dB
1	1	0	-11dB
1	1	1	-9dB

Control Register 4

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTMF/ALT SEL	TONE SEND	SAO/AFRO	TONE4	TONE3	TONE2	TONE1	TONE0

CR4-B0-B4 Tone frequency setting. See table below.
CR4-B5 Tone output pin select (receive side). 0= AFRO, 1=SAOP/SAON.
CR4-B6 Tone output pin select (transmit side). 0= Voice signal (transmit), 1=Tone signal.
CR4-B7 DTMF or alternative tones select. 1=DTMF, 0=Alternate.

(a) B7=1 DTMF Tones

B3	B2	B1	B0	TONES			B3	B2	B1	B0	TONES		
MSB			LSB	Low Group Hz	High Group Hz	Digit	MSB			LSB	Low Group Hz	High Group Hz	Digit
0	0	0	0	697	1209	1	1	0	1	0	852	1477	9
0	0	0	1	697	1336	2	1	1	0	1	941	1336	0
0	0	1	0	697	1477	3	1	1	0	0	941	1209	*
0	1	0	0	770	1209	4	1	1	1	0	941	1477	#
0	1	0	1	770	1336	5	0	0	1	1	697	1633	A
0	1	1	0	770	1477	6	0	1	1	1	770	1633	B
1	0	0	0	852	1209	7	1	0	1	1	852	1633	C
1	0	0	1	852	1336	8	1	1	1	1	941	1633	D

(b) B7=0 Alternative Tones

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	1k/1333Hz, 16Hz mod.	1	0	0	0	0	2500Hz
0	0	0	0	1	800/1kHz, 16Hz mod	1	0	0	0	1	2600Hz
0	0	0	1	0	800/1k Hz, 8 Hz mod	1	0	0	1	0	2670Hz
0	0	0	1	1	400Hz, 16Hz mod	1	0	0	1	1	2700Hz
0	0	1	0	0	2700Hz, 16 Hz mod	1	0	1	0	0	2800Hz
0	0	1	0	1	400Hz	1	0	1	0	1	2910Hz
0	0	1	1	0	800Hz	1	0	1	1	0	3000Hz
0	0	1	1	1	1kHz	1	0	1	1	1	3110Hz
0	1	0	0	0	1333Hz	1	1	0	0	0	3200Hz
0	1	0	0	1	1440Hz	1	1	0	0	1	—
0	1	0	1	0	1900Hz	1	1	0	1	0	—
0	1	0	1	1	2000Hz	1	1	0	1	1	—
0	1	1	0	0	2100Hz	1	1	1	0	0	—
0	1	1	0	1	2180Hz	1	1	1	0	1	—
0	1	1	1	0	2300Hz	1	1	1	1	0	—
0	1	1	1	1	2400Hz	1	1	1	1	1	—

Control Register 5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	PCM RX MUTE	PCM TX MUTE	Factory Test				

CR5-B0-B4 Test Control pins Must be zero for normal operation.
CR5-B5 1=Mute RX PCM signal at PCM decoder.
CR5-B6 1=Mute TX PCM signal at PCM coder.
CR5-B7 Reserved.

Control Register 6

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VOX ON/ OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LVL SEL	RX NOISE LVL1	RX NOISE LVL0

CR6-B1-B0 Background noise amplitude setting. See table below.

Rx Noise LVL1	Rx Noise LVL0	Rx Noise Power
0	0	No Noise
0	1	-55dBmO
1	0	-45dBmO
1	1	-35dBmO

CR6-B2 Rx Background noise amplitude setting.1=programmable using B1, B0. Do not clear this bit.
CR6-B3 Receive VOX function. 0=background noise transmit, 1=voice signal transmit. To use this data, set VOXI to zero.
CR6-B4 Hang over time. 1=320ms, 0=160ms. (T_{VXOFF}, Fig 5.)
CR6-B5,B6 Select Transmit signal energy detect (transmit VOX) threshold. See table below.

ON LVL1	ON LVL0	Tx VOX Threshold
0	0	-30dBmO
0	1	-35dBmO
1	0	-40dBmO
1	1	-45dBmO

CR6-B7 VOX function enable. 0=Disable, 1=Enable.

Control Register 7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VOXO	–	–	Factory Test				

CR7-B0-B4 Factory test control pins. Must be zero for normal operation.
CR7-B5-B6 Reserved.
CR7-B7 Transmit VOX (VOXO) status bit. Same as VOXO pin.
NOTE: 0dBmO = -7.7dBm(600Ω)

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V	AVDD, DVDD Supply Voltage	-0.5	5.5	V
Vi	Input Voltage	-0.3	5.8	V
Vo	Output Voltage	-0.3	5.8	V
Ts	Storage Temperature	-40	125	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
AVDD	Supply Voltage	2.7	3.0	3.6	V
DVDD	Supply Voltage	2.7	3.0	3.6	V
Ta	Ambient Temperature	0		70	°C
MCLK	Master Clock Frequency MCK SEL<1:0>=0,0 MCK SEL<1:0>=0,1 MCK SEL<1:0>=1,X	-0.01%	 12.288 19.200 10.368	+0.01%	MHz
FBCLK	Bit clock frequency	64		2048	kHz
FSYNC	Synchronous clock frequency, XSYNC, RSYNC		8		kHz
Dc	Clock duty cycle, MCK, BCLK, EXCK	30	50	70	%
Tir	Digital input rise time			50	ns
Tif	Digital input fall time			50	ns
txs, tsx	Tx sync pulse settling time, rising or falling	100			ns
tsr, trs	Rx sync pulse settling time, rising or falling	100			ns
tws	Sync pulse width	1 BCLK		100	µs
tds, tdh	PCM, ADPCM Set and hold time	100			ns
Csg	Bypass cap for VREF	10//0.1			µF

General Specifications

DC Characteristics (AVDD=VDD=2.7V to 3.6V, Ta=25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
IDD1	Supply Current @3.0V	Operating mode		8	14	mA
IDDPD	Supply Current @3.0V	Power down mode			0.5	µA
Iil	Input Leakage Current		-10		10	µA
Vil	Low Level Input Voltage				0.16xVDD	V
Vih	High Level Input Voltage		0.45xVDD			V
Vol	Low Level Output Voltage	|Iol|<4mA			0.4	V

Transmit Analog Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Rinx	Input Resistance	AIN1P, AIN1N, AIN2	10			MΩ
Rlgx	Output Load	XGA1, XGA2	20			kΩ
Clgx	Output Capacitance	XGA1, XGA2			100	pF
Vogx	Output Amplitude	XGA1, XGA2, Rl =20kΩ			1.30	Vpp
Vofgx	Offset voltage	pre op-amps	-20		20	mV

NOTE: -7.7dBm (600Ω) = 0dBm0, +3.14dBm0=1.30Vpp

Receive Analog Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Rinpw	Input Resistance	RGA	10			MΩ
Rlvf	Output Load	AFRO	20			kΩ
Rlao	Output Load	AOUTP, AOUTN, SAOP, SAON	1.2			kΩ
Clvf	Output Capacitance	AFRO			100	pF
Clao	Output Capacitance	AOUTP, AOUTN, SAOP, SAON			100	pF
Vo	Output Amplitude	AFRO, AOUTP, AOUTN, SAOP, SAON (all at above specified loads)			1.30	Vpp
Vofro	Offset voltage	AFRO	-100		100	mV
Vofao	Offset voltage	AOUTP, AOUTN, SAOP, SAON	-20		20	mV
Gdb	Open loop gain	Power amps only, as shown in fig 1.	40			dB

NOTE: -7.7dBm (600Ω) = 0dBm0, +3.14dBm0=1.30Vpp

AC Characteristics

Parameter	Condition		Min	Typ	Max	Units
	Freq (Hz)	Level (dBm0)				
Transmit Frequency Response	0 to 60Hz	0	25			dB
	300 to 3000Hz		-0.15		0.2	dB
	1020		reference			dB
	3300		-0.15		0.8	dB
	3400		0		0.8	dB
	3968.75		13			dB

AC Characteristics (continued)

Parameter	Condition		Min	Typ	Max	Units
	Freq (Hz)	Level (dBm0)				
Receive Frequency Response	0 to 3000Hz	0	-0.15		0.2	dB
	1020		reference			dB
	3300		-0.15		0.8	dB
	3400		0		0.8	dB
	3968.75		13			dB
Transmit Signal to distortion ratio C-message weighted	1020	3	35			dB
		0	35			dB
		-30	35			dB
		-40	28			dB
		-45	23			dB
Receive Signal to distortion ratio C-message weighted	1020	3	35			dB
		0	35			dB
		-30	35			dB
		-40	28			dB
		-45	23			dB
Transmit gain tracking	1020	3	-0.2		0.2	dB
		-10	Reference			dB
		-40	-0.2		0.2	dB
		-50	-0.5		0.5	dB
		-55	-1.2		1.2	dB
Receive gain tracking	1020	3	-0.2		0.2	dB
		-10	Reference			dB
		-40	-0.2		0.2	dB
		-50	-0.5		0.5	dB
		-55	-1.2		1.2	dB
Idle channel noise	Tx C-message	AIN=VREF			-68	dBm0p
	Idle Rx C-message	code 11010101 (A-law)			-72	
	Idle Rx C-message	code 11111111 (μ-law)			-72	
Absolute signal amplitude, XGA2, AFRO	1020	0	0.285	0.320	0.359	Vrms
Power Supply Noise rejection	Noise BW 0-50kHz	Noise Level 50mVpp	30			dB

Tone Generator AC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Dft	Frequency difference	All tones	-7		+7	Hz
Vtl	Transmit low reference level	DTMF low and alternate	-18	-16	-14	dBm0
Vth	Transmit high reference level	DTMF high group	-16	-14	-12	dBm0
Vrl	Receive low reference level	DTMF low and alternate	-4	-2	0	dBm0
Vrh	Receive high reference level	DTMF high group	-2	0	+2	dBm0
Vtwist	Relative levels of DTMF	Vth/Vtl, Vrh/Vrl	+1	+2	+3	dBm0

Programmable Gain Stages AC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Dg	Gain Accuracy		-1	0	+1	dB

VOX system AC Characteristics (see figures 4 and 5)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Tvxon	Transmit VOX detect time	off -> on		5		ms
Tvxof		on -> off		160/320		ms
Dvx	VOX detect level accuracy	CR6-B6,B5	-2.5	0	+2.5	dB

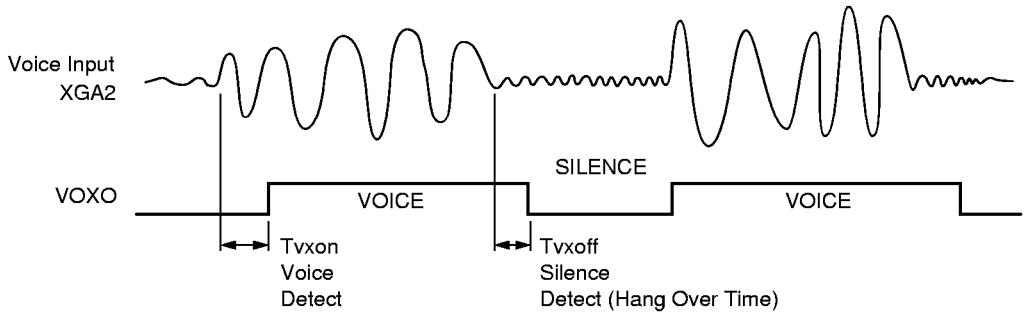


Figure 4 • *Transmit VOX function timing*

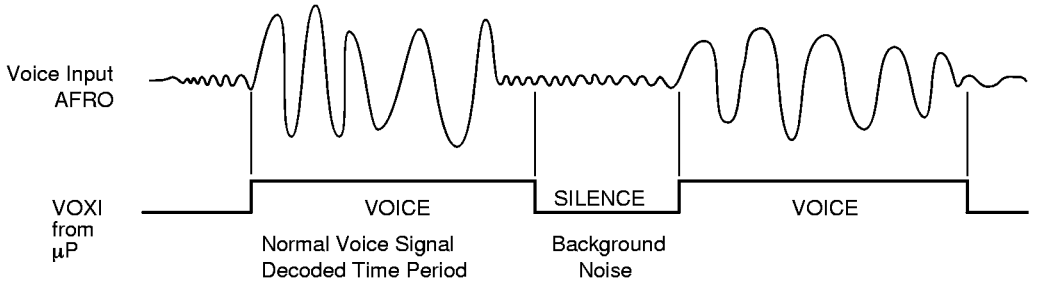


Figure 5 • *Receive VOX function timing (CR6-B3=0)*

Digital Interface AC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
tsdx, txd1, txd2, txd3	Digital output delay time, PCM & ADPCM transmit interface	1 LS TTL load + 100pF	0		200	ns
tsdr, trd1, trd2, trd3	Digital output delay time, PCM & ADPCM receive interface	1 LS TTL load + 100pF	0		200	ns
tm1-4	Serial output settling time	Cl=100pF	50			ns
tm5			100			ns
tm6,7 & tm9,10			50			ns
tm8,11			0		50	ns
F_{EXCK}	Shift clock frequency		0		10	MHz

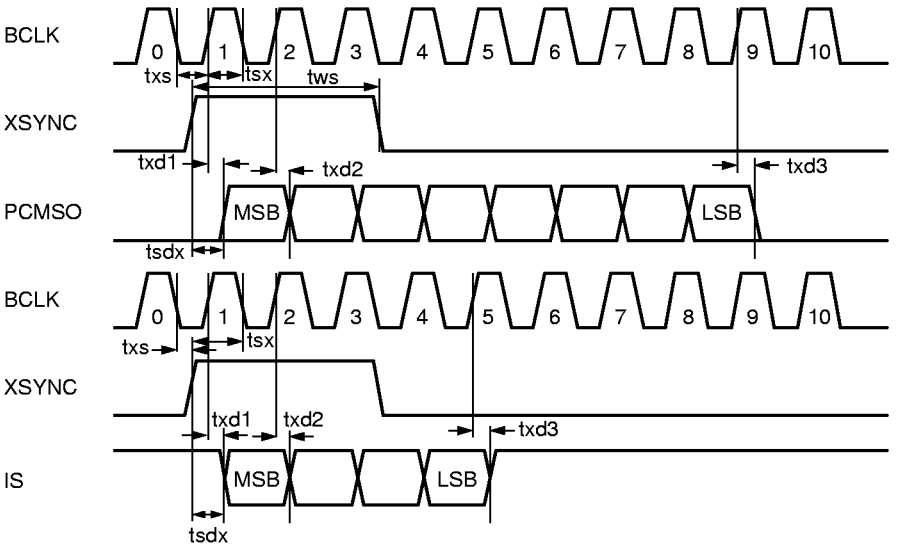


Figure 6 • *Transmit PCM/ADPCM serial interface*

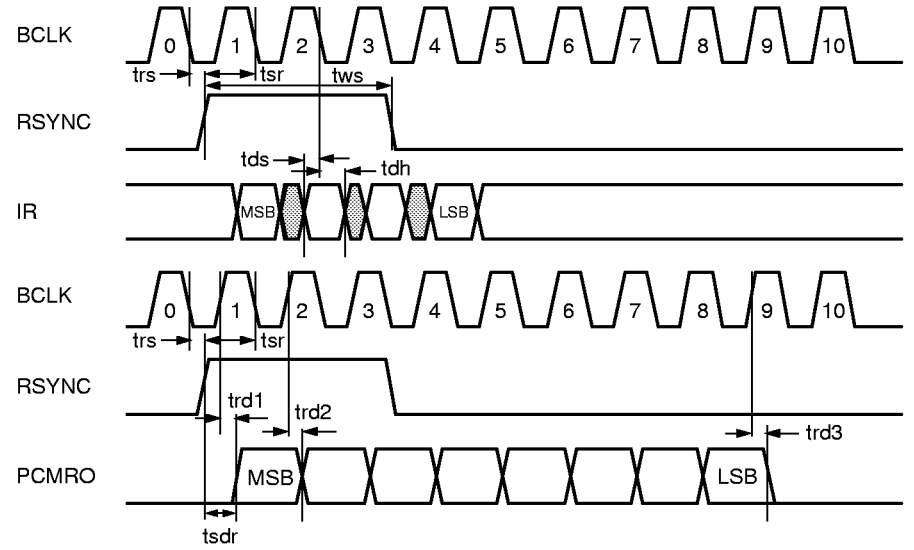


Figure 7 • *Receive PCM/ADPCM serial interface*

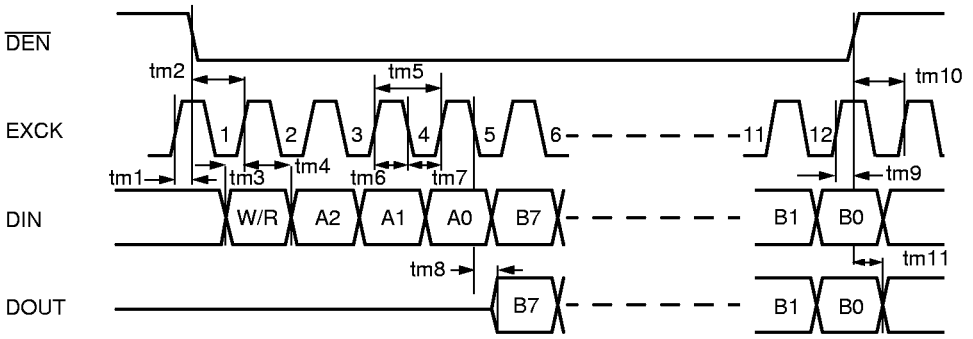
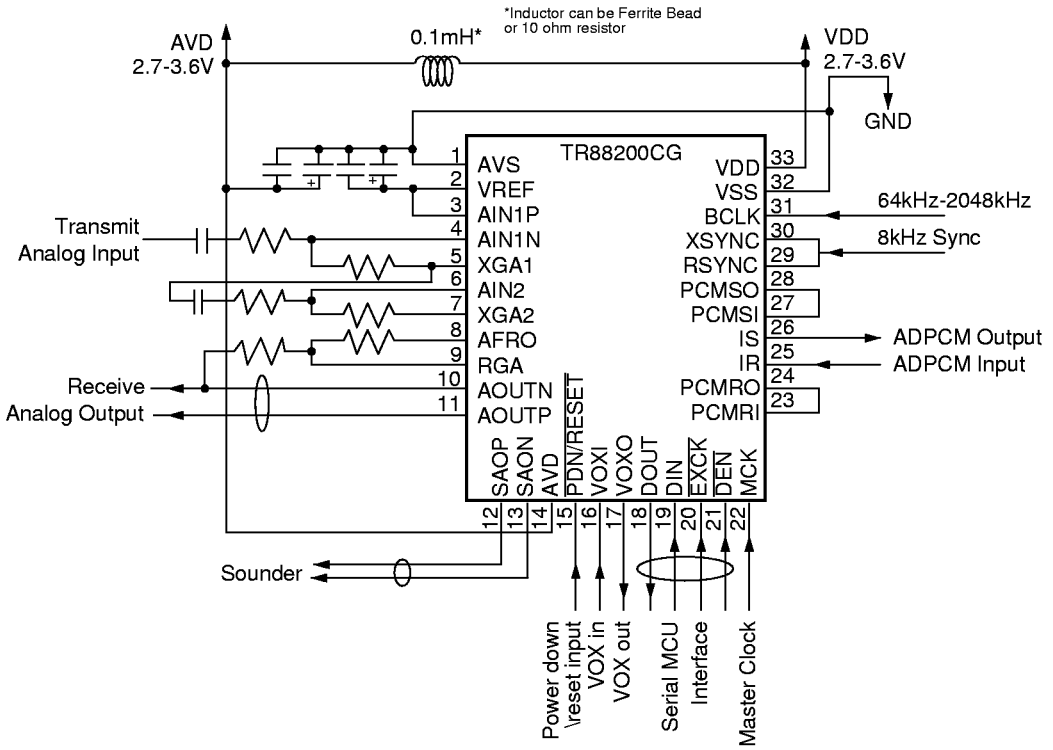


Figure 8 • *MCU serial interface*

Application Schematic

(single ended input))



Mechanical Dimensions

44 Pin LQFP

Dimensions in inches (mm)