TriTech Microelectronics

TR88L803/804

Pen-input Processor

Features

- Fully integrated pen input processor
- 2 multiplexed A/D input channels
- No user programming
- 10-Bit A/D for high resolution
- Low current consumption
- 2.7V to 5.5V operation
- Pen detection circuitry with auto Power Save
- 8-bit Parallel Interface option (TR88L804)
- Serial Interface option (TR88L803)
- On-chip oscillator circuit
- Data Averaging Mode

Applications

- Personal digital assistants
- Touch screens
- Electronic organizers / terminals
- Feature phones
- Digitizer tablets

General Description

The TR88L803/804 contain all the circuitry required to provide touch and pen-input capability to a variety of applications through an easy interface to low-cost resistive digitizers. The TR88L803/804 use 10-bit ADCs to resolve 1024 levels. This translates to a resolution of 204 dpi when used with a typical PDA sized digitizer pad. The TR88L803/804 is designed to simplify pen interfacing by integrating all pen-input tasks required to present X,Y-position data to the main application at 200 coordinate pairs per second.

Two additional ADC input channels are available under multiplex mode. These can be used to enable additional functions like battery gauge, ambient light or temperature.

The application interface is either through an interrupt-driven parallel bus or through a serial connection. The TR88L803/804 are fully self-contained

BLOCK DIAGRAM

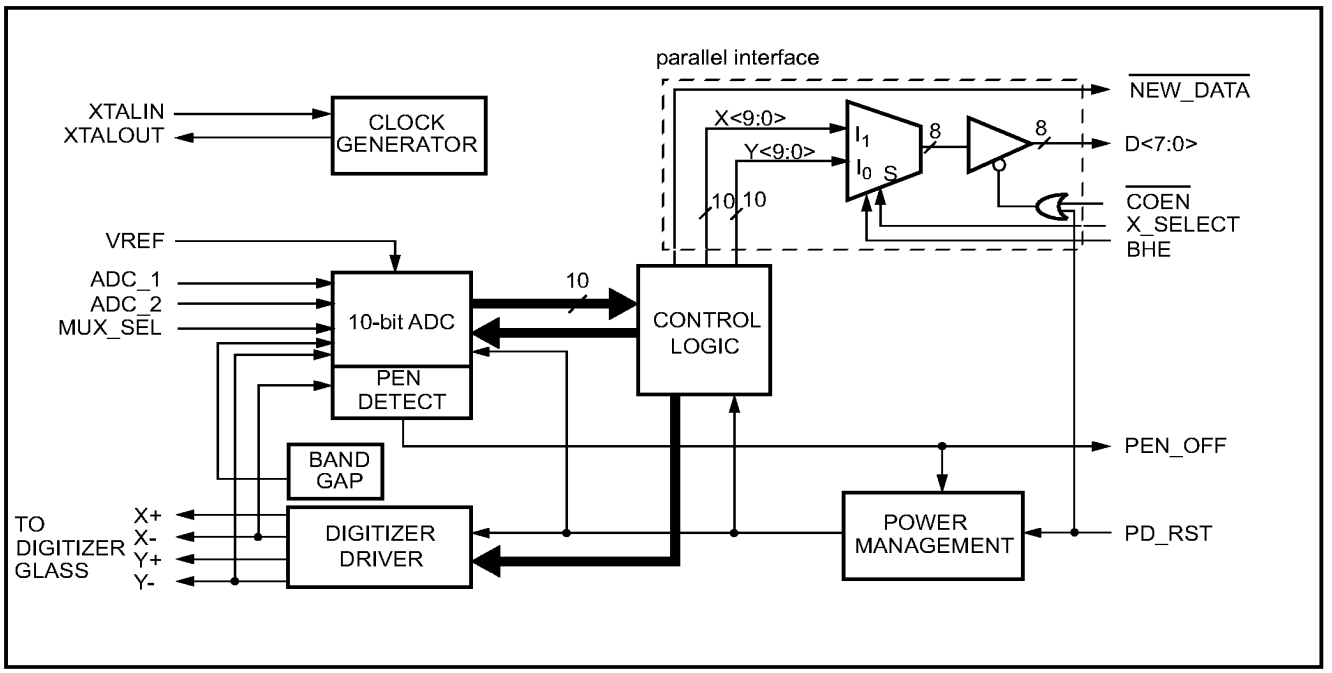


Figure 1 • *TR88L804 Block Diagram*

General Description (cont.)

and require no user programming. Pen detection status is signalled to the application for use in handwriting recognition and verification. Its low power consump-tion makes the device suitable for use with hand-held or battery-operated devices.

BLOCK DIAGRAM

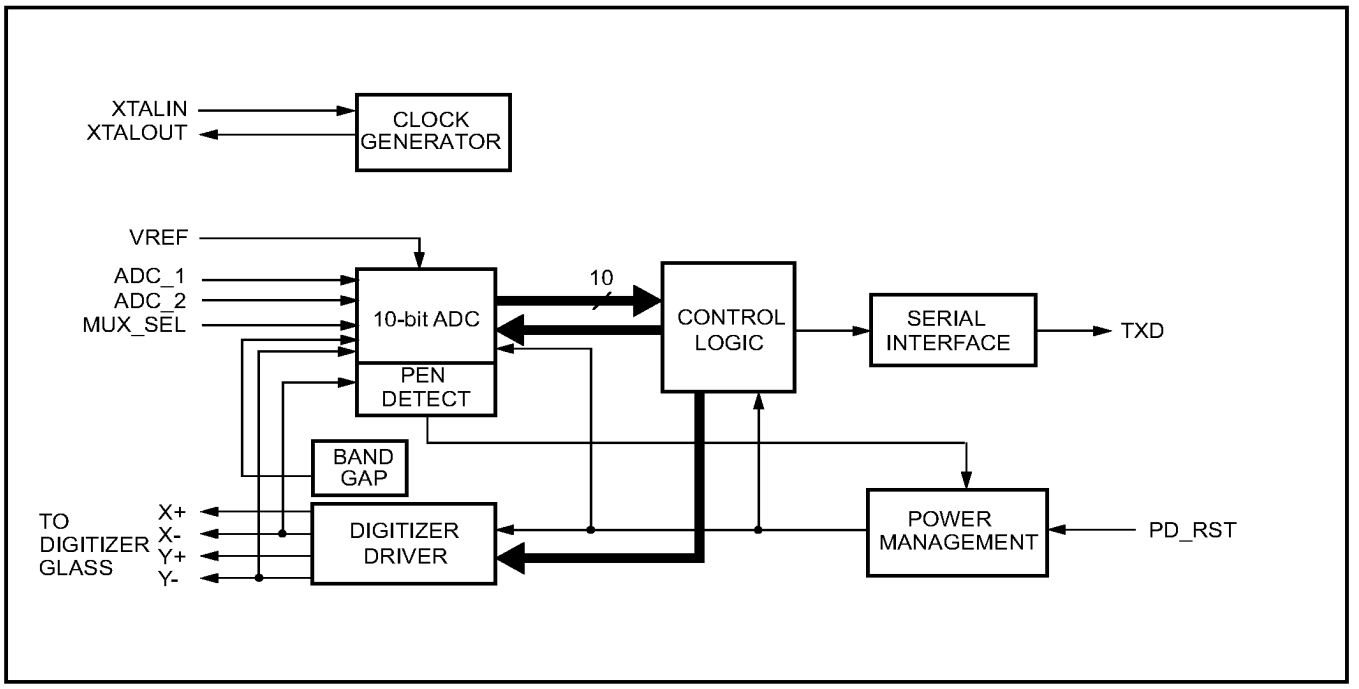
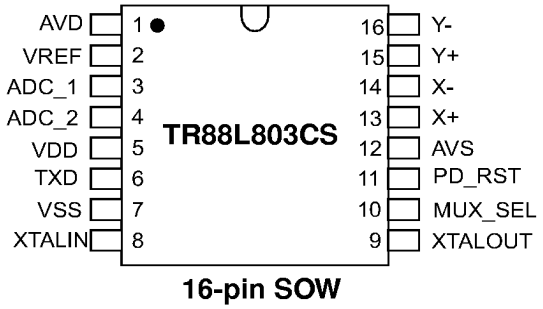
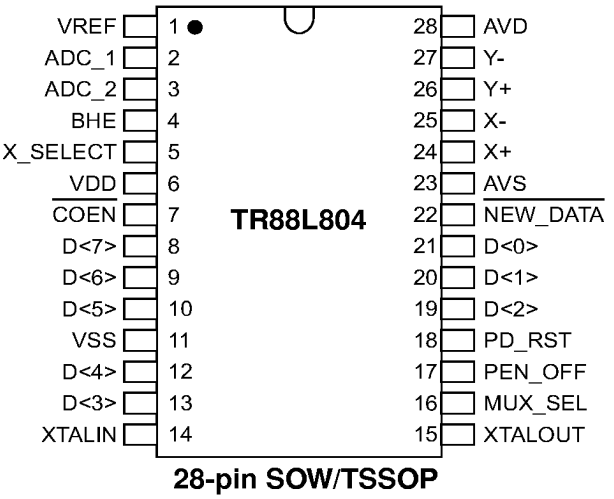


Figure 2 • *TR88L803 Block Diagram*

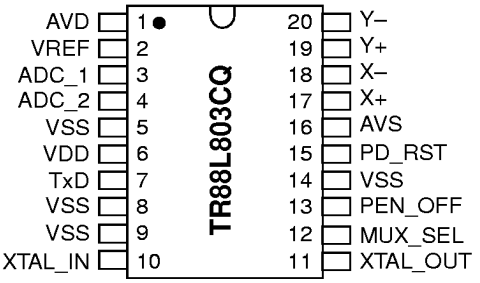
Pin Configuration





Package Top Views

Pin Configuration (continued)



Package Top View

Pin Descriptions TR88L803

CS (SOW-16) Pin	CQ (TSSOP-20) Pin	Pin Name	I/O	Description
1	1	AVD	Power	Analog Positive Supply. May be connected to digital positive supply (VDD) via a ferrite bead.
2	2	VREF	Analog Input	Internal 2.5V reference. Connect a 1 μF capacitor between this pin and analog ground pin (AVS).
3	3	ADC_1	Analog Input	ADC Input. Used when MUX_SEL is Logic 1. Should be connected to analog ground (AVS).
4	4	ADC_2	Analog Input	ADC Input. Used when MUX_SEL is Logic 1. Should be connected to analog ground (AVS).
n/a	5	VSS	Ground	Digital Ground
5	6	VDD	Power	Digital Power Supply
6	7	TXD	TTL Output	Serial Data Out. With a 1.8432MHz input clock, data is 19.2 kbps NRZ format (1 start bit; 1 stop bit).
7	8, 9	VSS	Ground	Digital Ground
8	10	XTAL_IN	CMOS Input	Crystal Oscillator input pin. Normally connected to 1.8432MHz CMOS input clock.
9	11	XTAL_OUT	CMOS Output	Used when connected to crystal as shown in Figure 7. Should be left floating if clock input is applied at XTAL_IN.
10	12	MUX_SEL	TTL Schmitt Input	ADC Multiplexor Select. Logic 1 for external ADC input mode. ADC input signals are applied at ADC_1 and ADC_2. Logic 0 for pen input mode.
n/a	13	PEN_OFF	TTL Output	Indicates pen not detected. Logic 1 if pen is not detected.
n/a	14	VSS	Ground	Digital Ground
11	15	PD_RST	TTL Schmitt Input	Active-High Power down/Reset input. Assert Logic 1 for ≥ 10ns to reset. Hold at Logic 1 for power-down mode.

Pin Descriptions TR88L803 (continued)

CS (SOW-16) Pin	CQ (TSSOP-20) Pin	Pin Name	I/O	Description
12	16	AVS	Ground	Analog Ground
13	17	X+	Analog I/O	Resistive tablet X- plane driver. Connect to x-terminal of resistive tablet.
14	18	X–	Analog I/O	
15	19	Y+	Analog I/O	Resistive tablet Y- plane driver. Connect to Y-terminal of resistive tablet.
16	20	Y–	Analog I/O	

Pin Descriptions TR88L804CQ/CS

SOW/ TSSOP-28 Pin	Pin Name	Type	Description
1	VREF	Analog Input	Internal reference filter point. Connect a 1μF ceramic capacitor between this pin and analog ground pin (AVS).
2	ADC_1	Analog Input	ADC input. Used only when MUX_SEL is Logic **1**. Should be connected to analog ground (AVS) if unused.
3	ADC_2	Analog Input	ADC input. Used only when MUX_SEL is Logic **1**. Should be connected to analog ground (AVS) if unused.
4	BHE	TTL Schmitt Input	Bus High Enable (TR88L804 only) Logic **1** to select D<9:2>. Logic **0** to select D<1:0> as MSBs. The lower 6 bits will all be zeros
5	X_SELECT	TTL Schmitt Input	X-Y data select. (TR88L804only) Logic **1** to select X-data output. Selects ADC_1 data if in ADC mux mode. Logic **0** to select Y-data output. Selects ADC_2 data if in ADC mux mode.
6	VDD	Power	Digital Positive Supply.
7	$\overline{\text{COEN}}$	TTL Schmitt Input	Chip Output Enable (TR88L804 only) Logic **1** to Hi-Z D<7:0>. Logic **0** to enable X/Y date to be read on D<7:0>
8-10	D<7:5>	TTL Output	X or Y coordinate output. (TR88L804 only)
11	VSS	Power	Digital Ground.
12,13	D<4:3>	TTL Output	X or Y coordinate output. (TR88L804 only)
14	XTALIN	CMOS Input	Crystal oscillator input pin. Normally connected to 1.8432MHz CMOS input clock.
15	XTALOUT	CMOS Output	Used when connected to crystal as shown in Figure 6. Should be left floating if clock input is applied at XTALIN.
16	MUX_SEL	TTL Schmitt Input	ADC Multiplexor Select Logic **1** for external ADC input mode. ADC input signals are applied at ADC_1 and ADC_2. Logic **0** for pen input mode.
17	PEN_OFF	TTL Output	Indicates pen not detected. (TR88L804 only) Logic **1** if pen is not detected. Independent of MUX_SEL.
18	PD_RST	TTL Schmitt Input	Active-Hi Power down/Reset input. Assert Logic **1** for ≥ 10ns to reset. Hold at Logic **1** for power-down mode.
19-21	D<2:0>	TTL Output	X or Y coordinate output. (TR88L804 only)
22	$\overline{\text{NEW\_DATA}}$	TTL Output	Indicates new data. (TR88L804 only). A Logic **0** pulse indicates that new data packet is available at D<7:0>.
23	AVS	Power	Analog Ground.
24	X+	Analog I/O	Resistive tablet X-plane driver. Connect across X-plane of resistive tablet.
25	X-	Analog I/O	
26	Y+	Analog I/O	Resistive tablet Y-plane driver. Connect across Y-plane of resistive tablet.
27	Y-	Analog I/O	
28	AVD	Power	Analog Positive Supply. May be connected to digital positive supply (VDD) via a ferrite bead.

Background Information

Digitizer Technologies

Pen-input appliances usually employ some form of digitizer tablet as a designated writing surface for capturing the position of the pen. The digitizer tablet often comes coupled with a display technology layer (for example LCD) so that the pen position on the digitizer tablet may be echoed on the display as "ink".

Resistive Digitizers

A resistive digitizer is made up of a multi-layer sandwich of resistive films and protective coatings all sitting on top of a flat-panel LCD.

Figure 3 shows a simplified blown-up picture of a typical resistive digitizer and its connections in a pen-input appliance.

The resistive digitizer works by direct contact of the pen flexing a pair of resistive films, hence any blunt pointing instrument may be used as the "pen". A protective hard coating is often added at the top of the resistive tablet to ensure durability of the resistive films and to prevent subsequent digitizing errors arising from the non-uniform wear and tear of an unprotected resistive film surface.

The simplicity of a resistive digitizer design and the use of a passive pen makes it an energy-efficient, lightweight and cost-effective solution to meet the needs of most pen-input appliances.

Digitizer Resolution

The resolution of a digitizer is typically measured in dots per inch (dpi) and is a function of the physical size of the digitizer tablet and the resolution of the ADC used in the conversion circuitry.

For example a 10-bit ADC is capable of resolving 2^{10} (or 1024) levels. When used in a 5 inch by 8 inch digitizer system, this results in a digitizer resolution of 128 dpi. When used in a smaller 3 inch by 5 inch system, the theoretical resolution becomes 204 dpi.

The effective digitizer resolution will be affected by things like the choice of digitizer technology, the choice of pen architecture (particularly the shape of the tip) and also by system noise.

In the case of resistive digitizers, the direct-contact nature of its operation and the pen thickness often imposes an upper limit on the effective system resolution that may be achieved, regardless of the resolution of the ADC itself.

Coordinate Data Report Rate

The coordinate data report rate is quantified in coordinate pairs per second(cpps) and refers to how many (x, y) coordinate positions of the pen were obtained from the tablet, digitized, and reported to the CPU every second. A higher coordinate rate enables closer tracking of the pen movement over the digitizer tablet surface and pre-

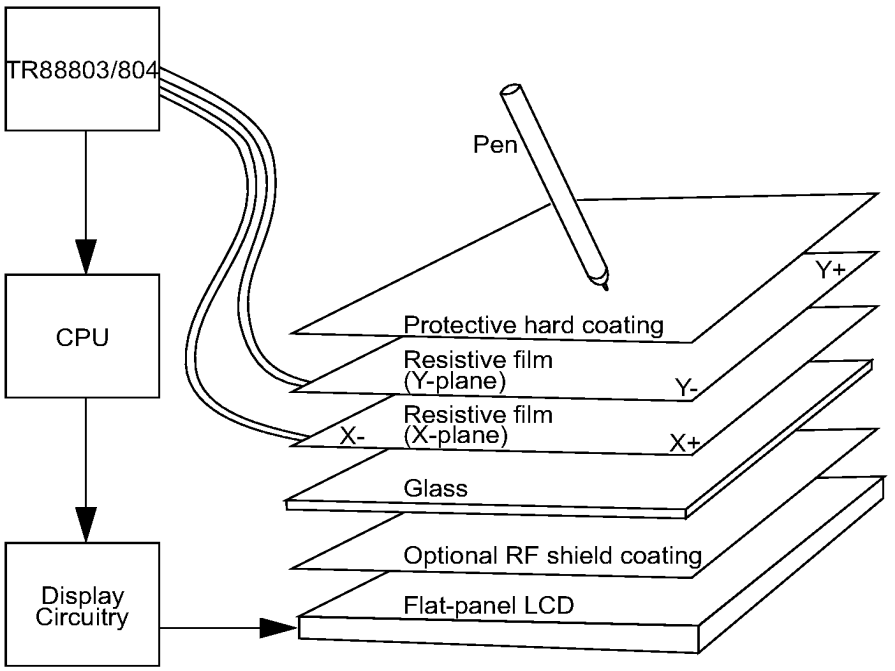


Figure 3 • *Typical Resistive Digitizer*

vents distortion of quick doodles or missed pen strokes in the entry of complex characters (e.g Chinese or Japanese script).

Functional Description

The TR88L803/804 when used in a pen-input appliance interfaces to a resistive digitizer and a micro-controller.

Resistive Digitizer Interface

The device interface to a typical resistive digitizer consists of four bi-directional (input/output) pins. These four pins (X+, X-, Y+, Y-) are connected across the X-plane resistive film and Y-plane resistive film of the digitizer respectively. On-chip buffers provide the necessary current drive to the resistive digitizer via these same four pins.

When a pen is in contact with the digitizer tablet, the pressure forces the X-plane and Y-plane resistive films to come into contact at the exact position where the pen is located (see Figure 4).

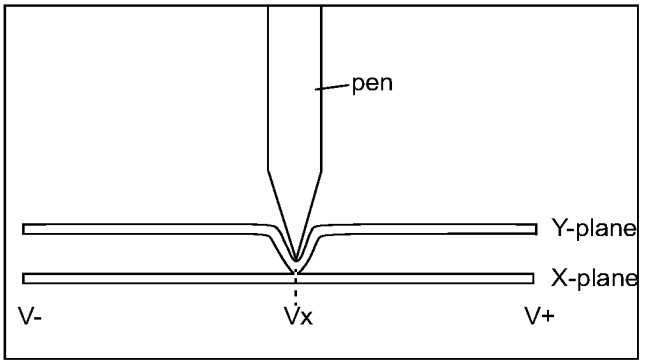


***Figure 4** • Locating the Pen Position*

To get the x-coordinate position, the TR88L803/804 will apply current drive to the X-plane resistive film (via X+, X-) and sense the voltages picked up by the Y-plane resistive film (via Y+, Y-). The current drive to the X-plane sets up a voltage gradient (V+, V-) across the resistive film. At the point of pen contact, the voltage at that point along the X-plane voltage gradient may be some value Vx, where V- ≤ Vx ≤ V+. Through direct contact, the Y-plane resistive film picks up the voltage Vx at the point of contact with the X-plane resistive film. This voltage is sensed by the TR88L803/804 and used to calculate the x-coordinate of the pen position.

Next, to get the y-coordinate position, the TR88L803/804 will apply the current drive at the Y-plane resistive film and sense the voltage picked up by the X-plane resistive film.

Pen Detection

On-chip circuitry detects if the pen is in contact with the digitizer tablet. No coordinate information will be made available at the parallel (TR88L804) or the serial (TR88L803) interfaces if no pen is detected to be in contact with the digitizer tablet.

In the TR88L804, the pen-detection status is flagged on a pin (PEN_OFF) and may be used by the system for signalling end-of-stroke for handwriting recognition software purposes. If no pen is detected, PEN_OFF will be pulled to Logic **1** and no coordinate data will be output. PEN_OFF at Logic **0** indicates that a pen is detected on the digitizer tablet and its coordinate position will be made available at the parallel interface.

Power Management

The TR88L803/804 is designed in advanced submicron CMOS process and consumes minimal power under normal operation. The system programmer can force the TR88L803/804 to enter power down mode by asserting and holding the PD_RST pin at Logic **1**. Normal operation (power up) will resume when PD_RST is returned to Logic **0**.

To further conserve power, the pen-detection circuitry will automatically switch the device to power down mode whenever there is no pen input detected for more than three seconds. Normal operation (power up) will automatically resume when any one of the following three events occur: pen down is detected; MUX_SEL is activated; or chip is reset (PD_RST pulled to Logic **1** and then returned to Logic **0**).

This auto power save feature is enabled only in the pen-input mode (MUX_SEL = Logic **0**) and not in the multiplexed ADC mode (MUX_SEL = Logic **1**).

Coordinate Calculation

The voltages picked up by the digitizer interface are first passed to a 10-bit Analog-to-Digital Converter (ADC) where they are digitized before further processing. The conversion speed of the ADC permits a data rate of 200 coordinate pairs per second when the crystal frequency (Fclk) is 1.8432 MHz. The Control Logic block calculates the (x, y) coordinate location of the pen and formats the data for output via the parallel (D<7:0>) and serial (TXD) interfaces. The x-coordinate and y-coordinate information are each 10-bit wide.

Data-Averaging

To provide better immunity against system noise, the TR88L803/804 offer built-in data-averaging. The coordinate data output at D<7:0> (TR88L804) or at TXD (TR88L803) is the output of an IIR filter which averages the previous and the current X-Y positions sampled by the ADC.

Multiplexed ADC Mode

Two independent ADC input channels are available in TR88L803 and TR88L804 under the ADC multiplex mode. A control pin (MUX_SEL) multiplexes the internal ADC between serving the digitizer inputs (X+, X-, Y+, Y-) and the 2 independent ADC input channels ADC_1 and ADC_2.

When a Logic **1** is asserted on MUX_SEL, the ADC_1 and ADC_2 inputs are enabled and any analog signals applied at ADC_1 and ADC_2 will be digitized by the ADC. In this mode, both ADC_1 and ADC_2 are cyclically sampled. ADC_1 data appears at the output instead of X coordinates and ADC_2 data appears instead of Y coordinates. We recommend that the user grounds (tie to AVS) any unused ADC input channel(s).

ADC reference voltage is ratio metric while reading the digitizer inputs. This filters supply noise from the digitizer. However, ADC_1 and ADC_2 inputs are referenced to the fixed band gap voltage and thus could be used as a battery guage. These inputs have a fixed full scale value of roughly 2.8 volts. Band gap reference is thus used only in the multiplexed ADC mode.

When a Logic **0** is asserted on MUX_SEL, the normal pen input mode at the digitizer input pins (X+, X-, Y+, Y-) is enabled.

Voltage on pins ADC_1 and ADC_2 can be measured only when a pen is on the digitizer surface.

Parallel Interface: TR88L804

A parallel interface is available on the TR88L804 in a 28-lead SOP package. The coordinate data is available at the data interface as D<7:0>. Three control pins ($\overline{\text{COEN}}$, X_SELECT, BHE) multiplex the x-coordinate and y-coordinate data onto D<7:0>. A Logic **0** on $\overline{\text{COEN}}$ will enable data onto the bus so that the TR88L804 may be used in parallel with other devices. When a Logic **1** is asserted on X_SELECT, the x-coordinate data is made available on D<7:0>. When a Logic **0** is asserted on X_SELECT, the y-coordinate data is selected. As the device offers 10-bit resolution, the pin BHE enables the data as D<9:2> (BHE = Logic **1**) and D<1:0> (+ six LSBs = Logic **0**) onto D<7:0>. A status pin ($\overline{\text{NEW\_DATA}}$) pulses low if a pen is detected to indicate when a new coordinate data pair is available. Parallel data format is shown in Figure 5.

		MSB							LSB
High byte	BHE=Logic 1	D9	D8	D7	D6	D5	D4	D3	D2
Low byte	BHE=Logic 0	D1	D0	0	0	0	0	0	0

Figure 5 • *Parallel data format*

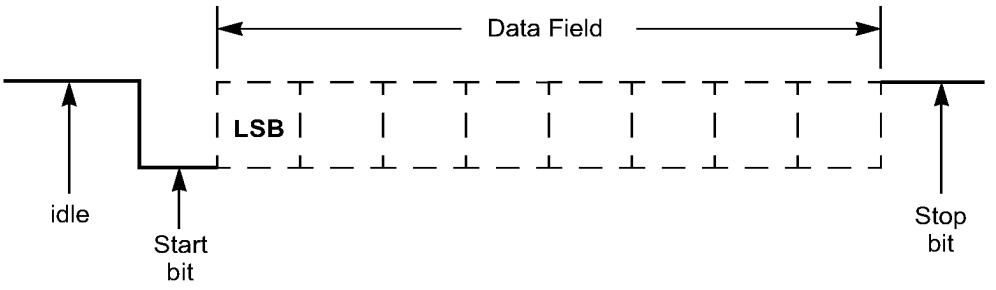


Figure 6 • *Serial data format*

Serial Interface: TR88L803

With the TR88L803 device, serial data is available at the TXD pin. With an input clock of 1.8432 MHz, the serial baud rate is 19200 bits per second. Table 1 shows the serial interface data format.

Table 1. *Serial Interface Data Format*

Parameter	Description
Data Output Voltage Levels	TTL
Serial output	1 start bit, 8 data bits, 1 stop bit, Non-return-to-zero (NRZ); No parity
Normal Frame [1] (5 bytes)	byte 1 = 0xFF byte 2 = Low byte of X byte 3 = High byte of X byte 4 = Low byte of Y byte 5 = High byte of Y
Pen off frame [2] (3 bytes)	byte 1 = 0xFF byte 2 = 0xFE byte 3 = 0xFE
Stream Format	Normal Frame Normal Frame . . . Normal Frame Pen-Off Frame
Transmission Rate	200 frames/sec at 19200 bps

***Notes**:*

1. *Normal frames sent when pen is detected on Digitizer. Refer to Fig 5. for bit pattern of these bytes.*
2. *TxD line goes idle after a Pen Off frame.*

Absolute Maximum Ratings

Beyond these limits damage may occur to the device

Symbol	Parameter	Min	Max	Units
V	Supply Voltage	-0.25	6.5	V
Ts	Storage Temperature	-40	125	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vdd	Supply Voltage	2.7	—	5.5	V
Avd	Analog Supply Voltage	2.7	—	5.5	V
Fclk	Crystal Frequency[1]	900KHz	1.8432	4.0	MHz

Note:

1. Min. and Max. guaranteed by design. All testing done at typical frequency.

General Specifications

Valid for 25°C ambient temperature and 3.3V supply voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{il}	TTL input LO	Vdd = 3.3V			0.4	V
V_{ih}	TTL input HI	Vdd = 3.3V	1.9			V
V_{+}	Schmitt input HI	Vdd = 3.3V		1.3		V
V_{-}	Schmitt input HI	Vdd = 3.3V		0.8		V
V_{hys}	Schmitt input Hysteresis	Vdd = 3.3V		0.5		V
I_{il}	Input leakage	V_i = Vdd or Vss	-10	0.1	10	µA
V_{ol}	Low Level Output	I_{ol} = 4mA, Vdd = 3.3V			0.4	V
V_{oh}	High Level Output	I_{oh} = -1mA, Vdd = 3.3V	2.4			V
I_{oz}	High Z leakage	V_o = Vdd or Vss	-10	0.4	10	µA

Valid for 25°C ambient temperature and 5V supply voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{il}	TTL input LO	Vdd = 5.0V			0.8	V
V_{ih}	TTL input HI	Vdd = 5.0V	2.0			V
V_{+}	Schmitt input HI	Vdd = 5.0V		1.8		V
V_{-}	Schmitt input HI	Vdd = 5.0V		1.2		V
V_{hys}	Schmitt input Hysteresis	Vdd = 5.0V		0.6		V
I_{il}	Input leakage	V_i = Vdd or Vss	-10	0.1	10	µA
V_{ol}	Low Level Output	I_{ol} = 4mA, Vdd = 5.0V			0.4	V
V_{oh}	High Level Output	I_{oh} = -1mA, Vdd = 5.0V	2.4			V
I_{oz}	High Z leakage	V_o = Vdd or Vss	-10	0.4	10	µA

Electrical Specifications

Valid for 25°C ambient temperature and 3.3V supply voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Digital Supply Current (using CMOS - level clock)	Power up PD_RST=Logic **0**		300	600	μA
I_{AVD}	Analog Supply Current	Power up PD_RST=Logic **0**		1.7	3	mA
I_{VDDPD}	Digital Supply Current	Power down PD_RST=Logic **1**		0.1	1	μA
I_{AVDPD}	Analog Supply Current	Power down PD_RST=Logic **1**		0.1	1	μA
R_{driver}	Parasitic Resistance of On-chip Driver			35	50	Ω
R_D	Resistance of Digitizer Film		250		10000	Ω
R_DC_D	Time Constant of Digitizer Film	Fclk=1.8432MHz			10	μS
BR	Serial Baud Rate	Fclk=1.8432MHz		19200		bps
CPPS	Coordinate Pairs Per Second	Fclk=1.8432MHz		200		cpps
T_{UP}	Power Up Time from PD_RST being deasserted to reliable coordinate data	(using 1μF capacitor at VREF)			200	ms
V_{ADC}	Input voltage on pins ADC_1, ADC_2		0		2 x V_{BG}	V
V_{BG}	Band Gap Reference Voltage		1.2	1.3	1.4	V

Valid for 25°C ambient temperature and 5.0V supply voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Digital Supply Current (using CMOS - level clock)	Power up PD_RST=Logic **0**		300	600	μA
I_{AVD}	Analog Supply Current	Power up PD_RST=Logic **0**		2.5	5.0	mA
I_{VDDPD}	Digital Supply Current	Power down PD_RST=Logic **1**		0.1	40	μA
I_{AVDPD}	Analog Supply Current	Power down PD_RST=Logic **1**		0.2	30	μA
R_{driver}	Parasitic Resistance of On-chip Driver			20	50	Ω
R_D	Resistance of Digitizer Film		300		10000	Ω
R_DC_D	Time Constant of Digitizer Film	Fclk=1.8432MHz			10	μS
BR	Serial Baud Rate	Fclk=1.8432MHz		19200		bps
CPPS	Coordinate Pairs Per Second	Fclk=1.8432MHz		200		cpps
T_{UP}	Power Up Time from PD_RST being deasserted to reliable coordinate data	(using 1μF capacitor at VREF)			200	ms
V_{ADC}	Input voltage on pins ADC_1, ADC_2		0		2 x V_{BG}	V
V_{BG}	Band Gap Reference Voltage		1.2	1.3	1.4	V

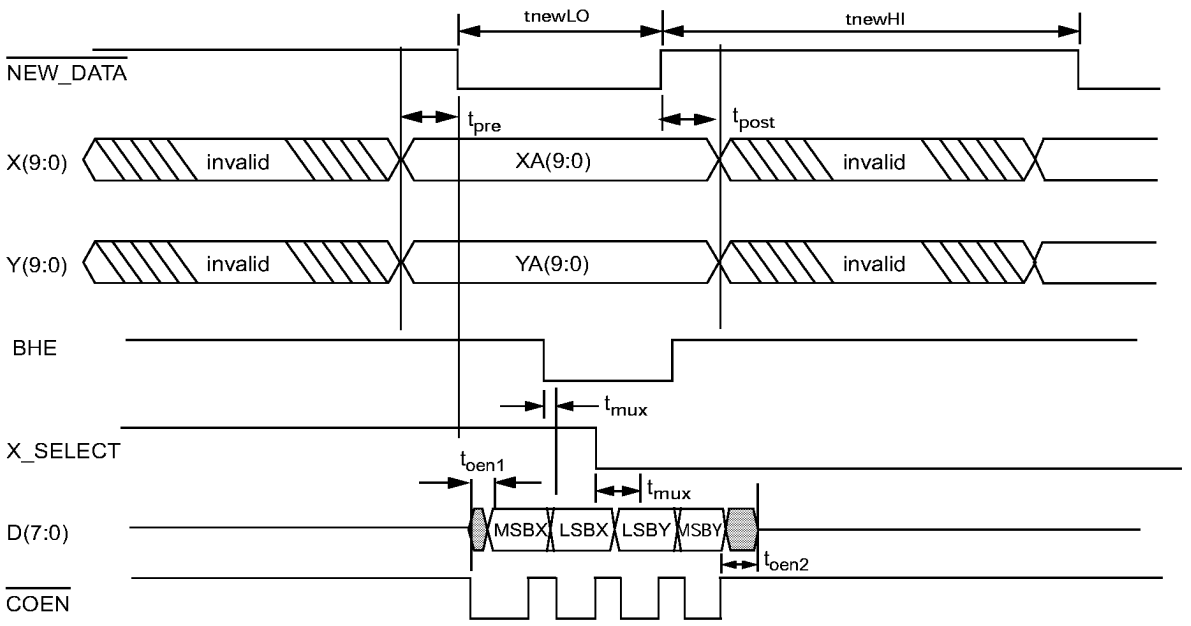
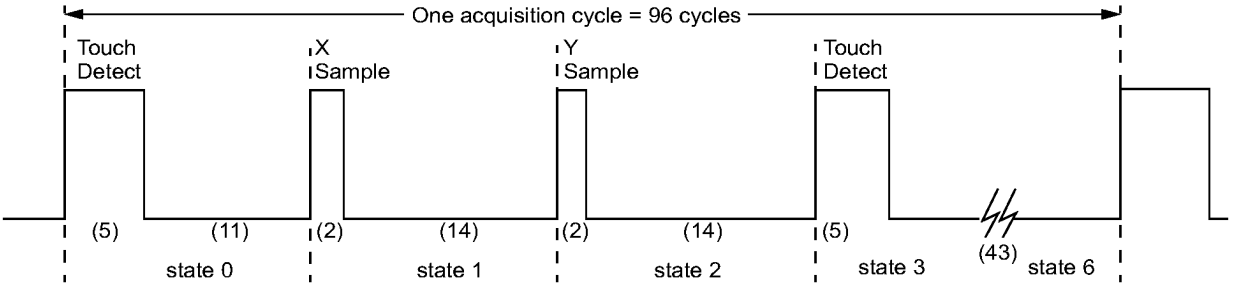


***Figure 7** • Parallel Interface Timing Diagram*

Parallel Interface Timing Fclk = 1.8432MHz

Symbol	Parameter	Min	Typ	Max	Units
tnewHI	NEW_DATA Logic 1 pulse width. Scales to Fclk		4.2		ms
tnewLO	NEW_DATA Logic 0 pulse width. Scales to Fclk		0.8		ms
tpre	Data setup before NEW_DATA falling edge	100			ns
tpost	Data setup before NEW_DATA rising edge	100			ns
tmux	Multiplexer selector path propagation delay		10	40	ns
toen1	COEN falling edge to data bus driven		10	40	ns
toen2	COEN rising edge to data bus Hi-Z		10	40	ns



- Figures in brackets are no. of clock cycles. There are 6 states in a cycle.
- Internal Clock frequency = Crystal freq / 96
- 16 clocks per state
- For example, with 1.8432 MHz crystal, X sample width is 104.166 micro seconds.
- Serial output data rate = Crystal clock frequency / 96 bits per sec.

***Figure 8** • Basic Timing Diagram*

Application Information

Figure 9 shows a typical application diagram for TR88L804. The clock input is derived by connecting a quartz crystal across XTALIN and XTALOUT.

Figure 10 shows a typical application diagram for TR88L803. The clock input is driven through pin XTALIN.

The TR88L803/804 4-wire digitizer interface connects easily to most resistive digitizer tablets available from various manufacturers including MicroTouch, Dynapro, Panasonic and Samsung.

On the board, the analog traces at X-, X+, Y-, Y+ should be kept short and routed away from other signal lines, especially clock-lines and high-activity lines. The traces from the TR88L803/804 to the capacitors should also be kept short. Use of a Ferrite bead between AVD and VDD is recommended.

Digitizer vendors often specify the resistance of the ITO Coating in Ohms per square. Lead to lead resistance along an axis may be obtained by multiplying this value with the aspect ratio of the digitizer.

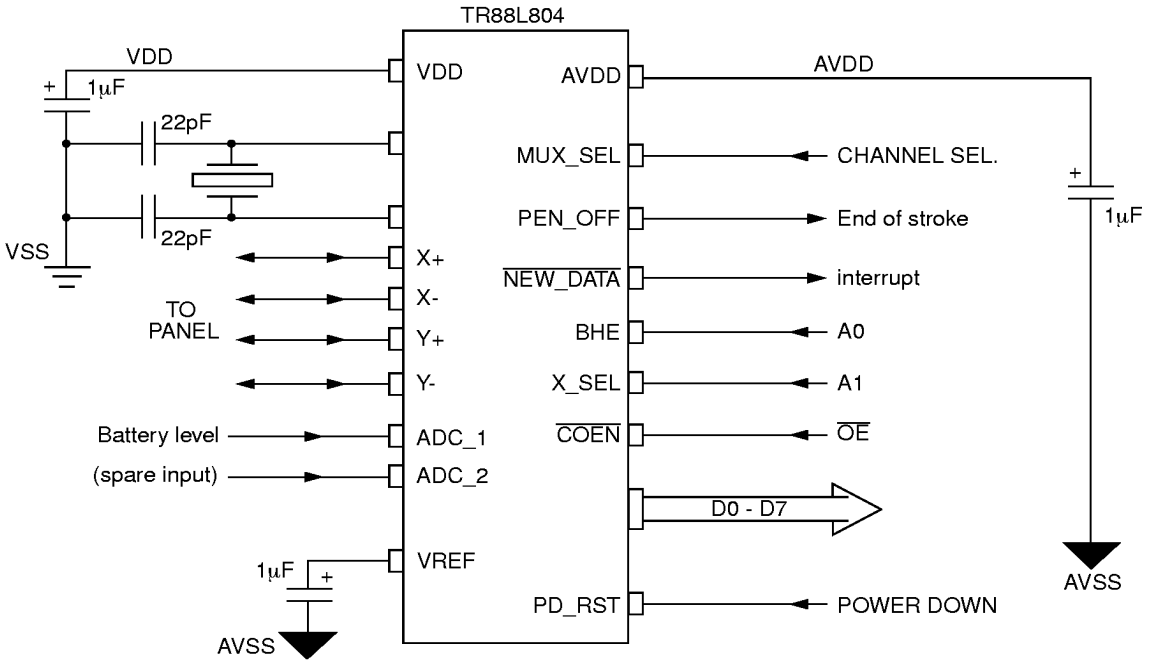


Figure 9 • *Typical Connection Diagram for TR88L804.*

Serial Interface Connections

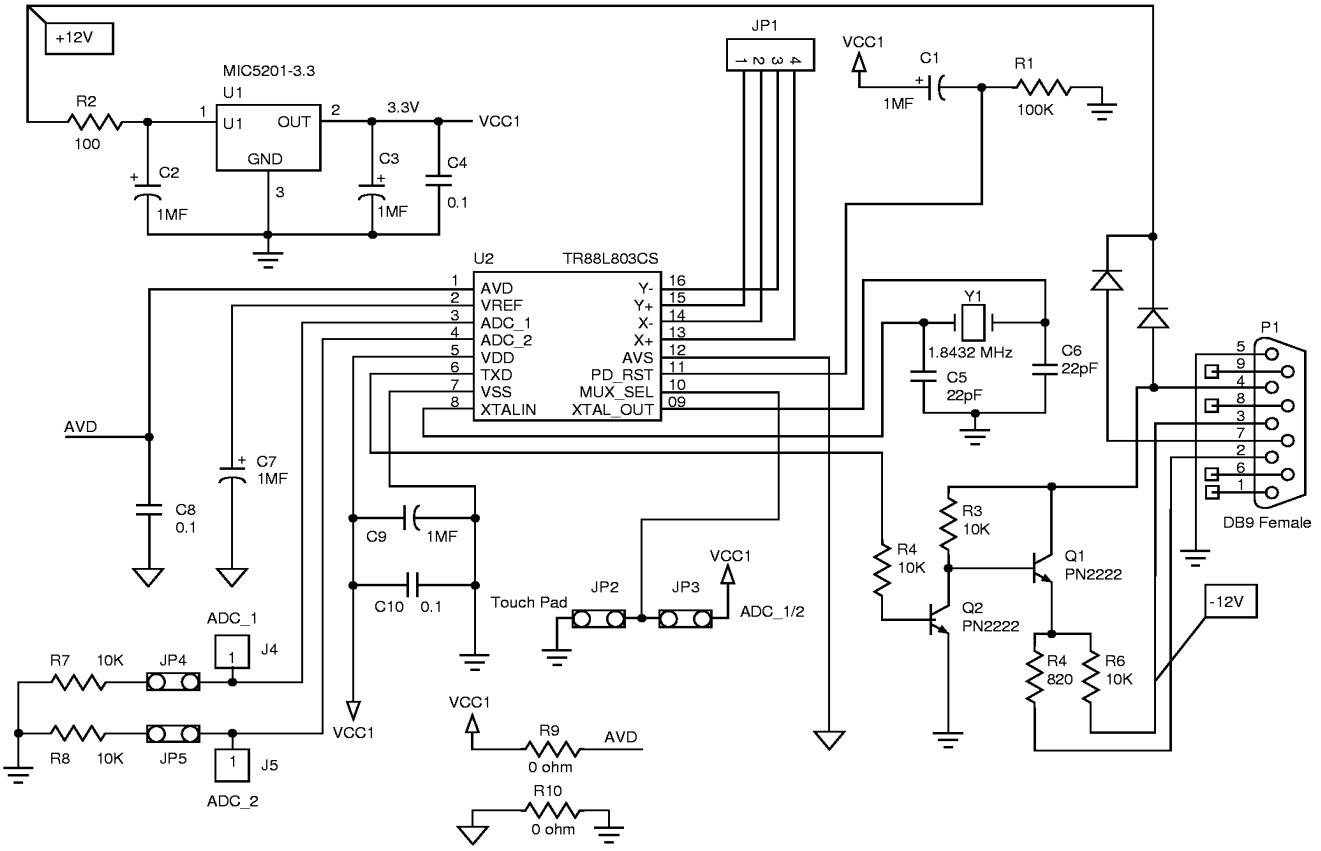


Figure 10 • *Typical Connection Diagram for TR88L803*

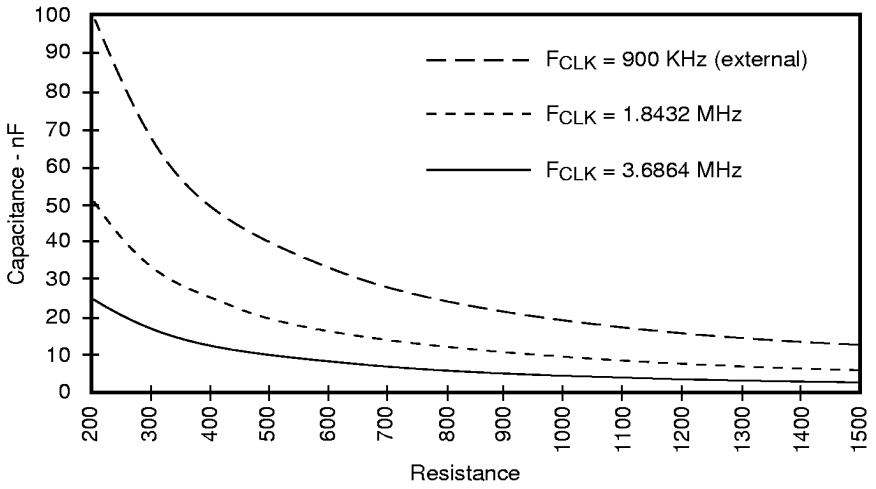


Figure 11 • *Typical limits for digitizer R-C parameters at different clock frequencies.*

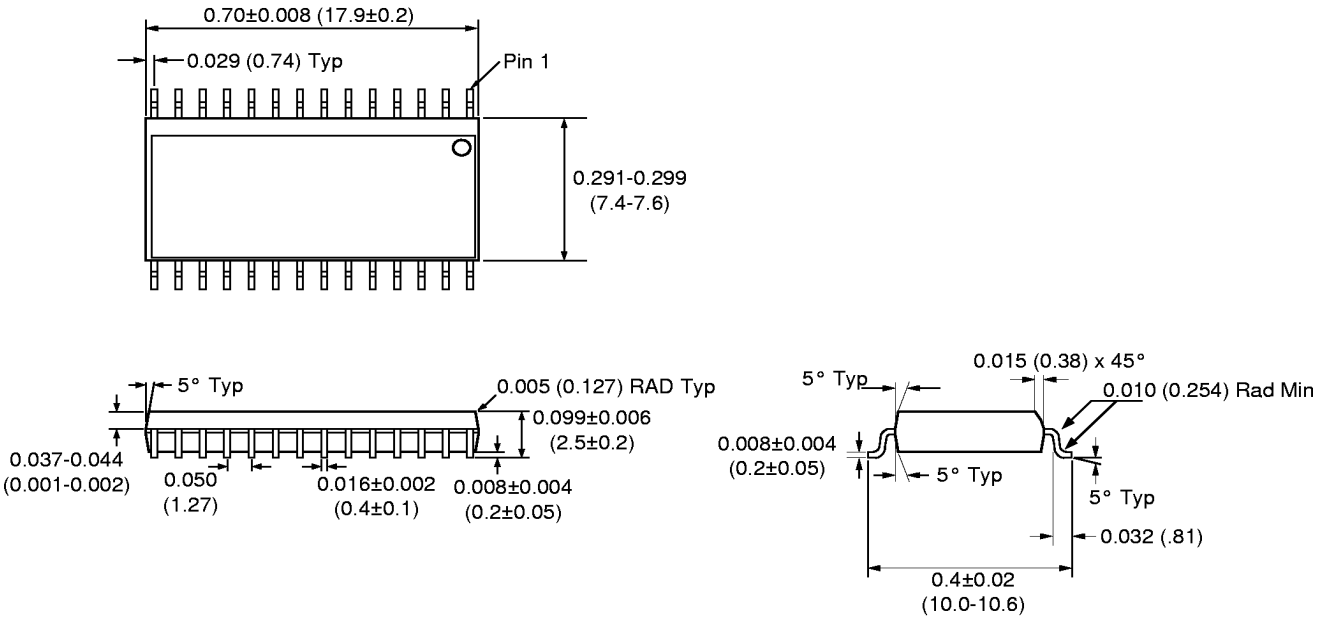
Notes:

1. *R-C limits shown are indicative only.*
2. *User should not expect to use all 1024 levels of the 10 bit ADC. Parasitic resistance of on-chip driver results in an internal voltage drop leading to reduced usable counts. This effect may be noticeable at lower values of digitizer resistance.*
3. *922KHz provides a baud rate of 9600baud.*

Mechanical Dimensions

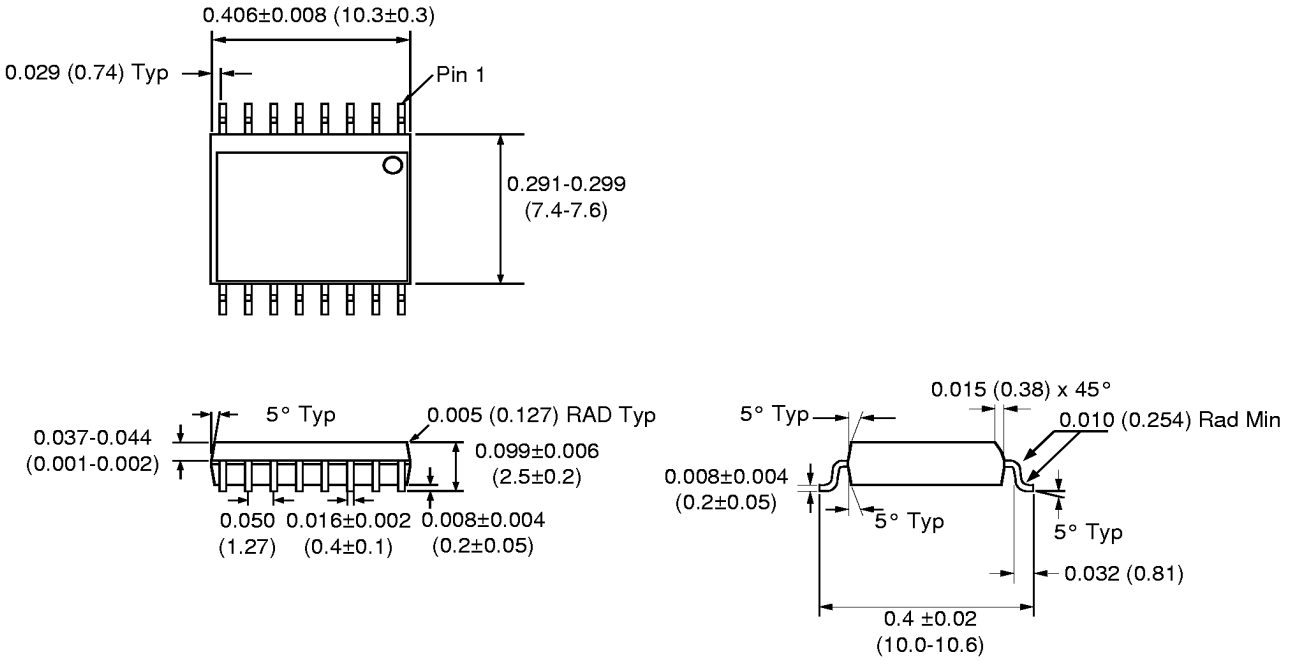
28-pin SOW

Dimensions in inches (mm)



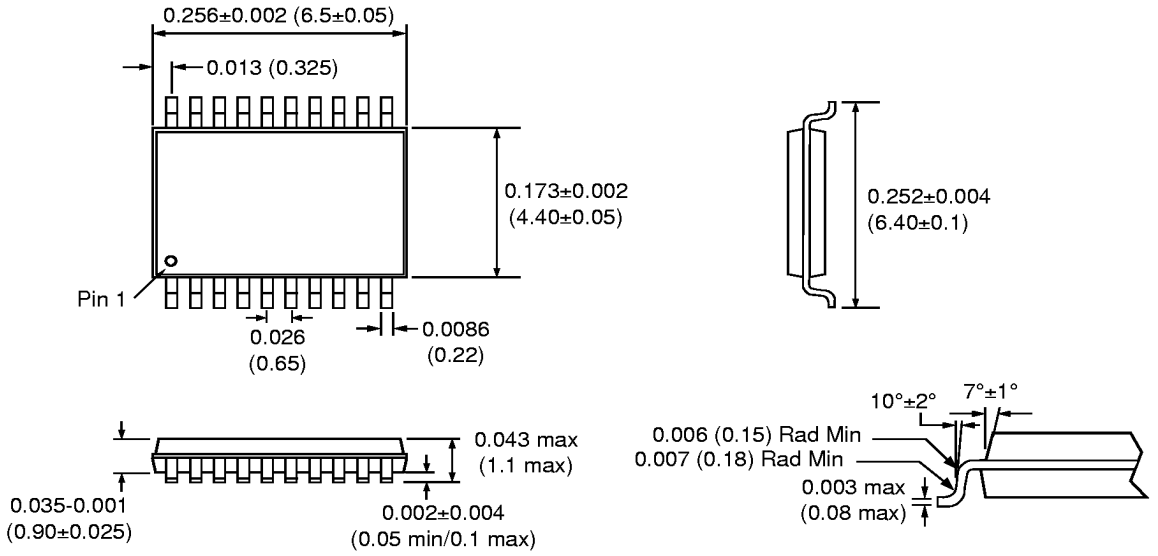
16-pin SOW

Dimensions in Inches (mm)

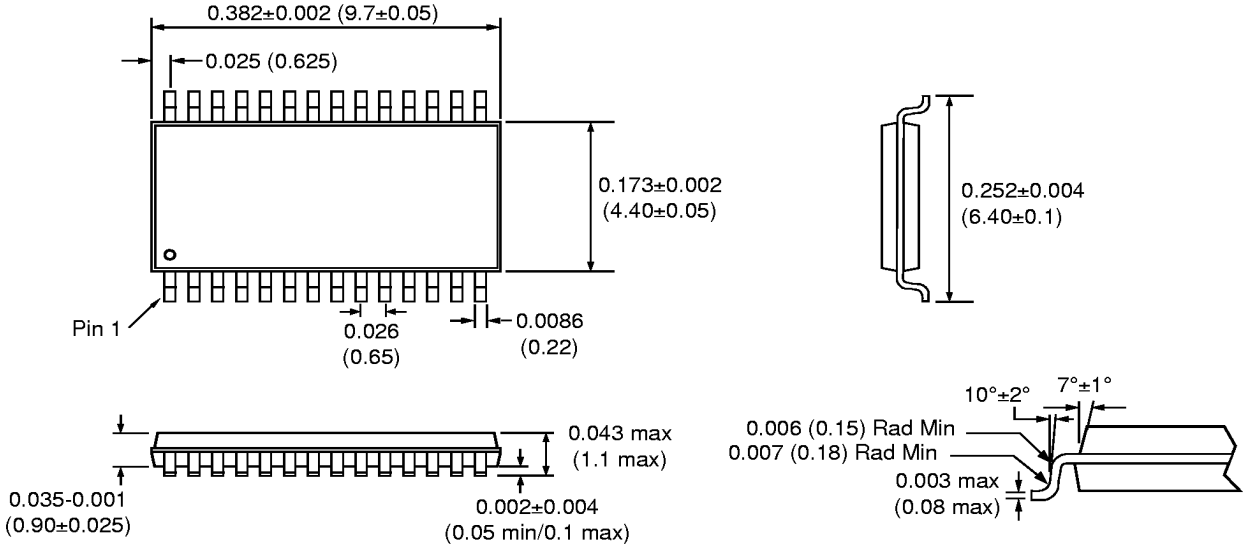


Mechanical Dimensions

20-pin TSSOP Dimensions in inches (mm)



28-pin TSSOP Dimensions in inches (mm)



Ordering Information

Part Number	Package Type
TR88L803CS	16-pin SOW
TR88L803CQ	20-pin TSSOP
TR88L804CS	28-pin SOW
TR88L804CQ	28-pin TSSOP