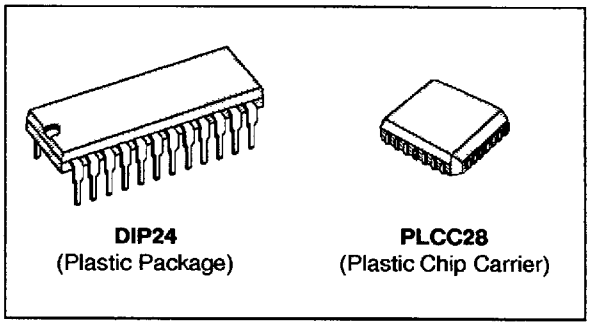
SGS-THOMSON MICROELECTRONICS

TS68950

MODEM TRANSMIT ANALOG INTERFACE

- TWO CHANNEL DIGITAL TO ANALOG CONVERTER FOR TRANSMISSION OF DIGITAL DATA TO THE TELEPHONE LINE AND ECHO CANCELLATION
- 6TH ORDER SWITCHED CAPACITOR LOW PASS FILTER FOR ADAPTATION TO THE TELEPHONE BANDWIDTH
- OUTPUT CONTINUOUS TIME SMOOTHING FILTER
- PROGRAMMABLE TRANSMIT OUTPUT ATTENUATION OVER A 22dB RANGE WITH 2dB STEPS
- DIRECT INTERFACE WITH DSP STANDARD MPU 8-BIT BUS
- LOW POWER CMOS TECHNOLOGY
- AVAILABLE IN DIL OR SURFACE MOUNT PACKAGE

The TS68950 copes with all the CCITT recommendations from V.21 to V.33 including full-duplex recommendations with echo-cancellation (V.32) thanks to its second transmit channel.
Used in conjunction with the TS68951 Receive (Rx) Analog Front-End circuit and the TS68952 clock generator*, it provides a very economic and efficient interface to digital signal processing functions in high speed modems or telephony applications.
* The interconnection between the 3 MAFE chips is detailed P. 9/14.



DIP24
(Plastic Package)

PLCC28
(Plastic Chip Carrier)

DESCRIPTION

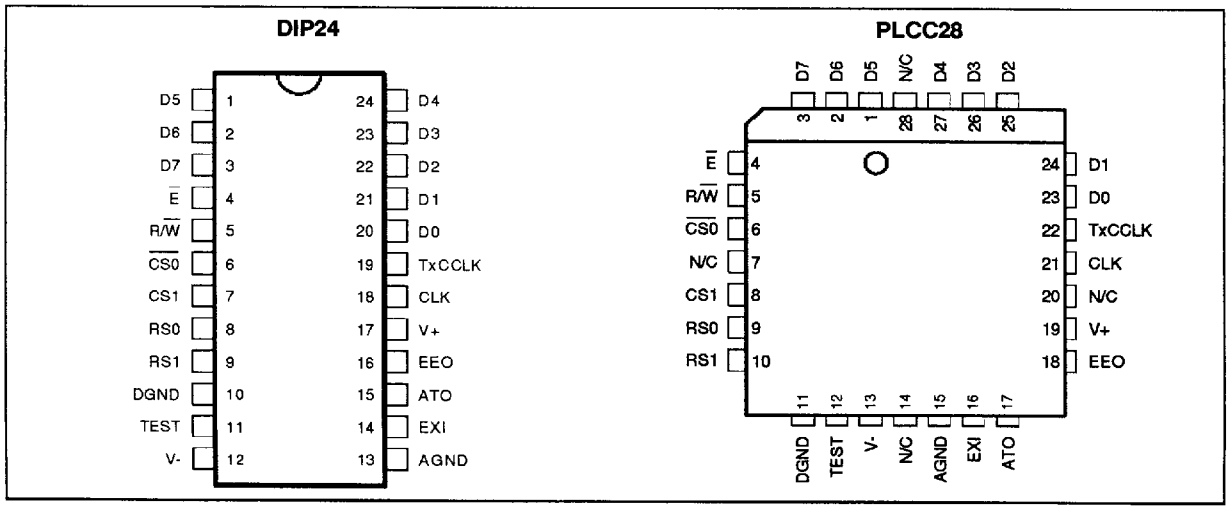
The TS68950 is a Transmit (Tx) Analog Front-End circuit designed to implement the filtering and digital to analog conversion required by high speed voice-band modems, telephony or speech coding applications using digital signal processing technology.

ORDER CODES

Part Number	Temperature Range	Package
TS68950CP	0 to +70°C	DIP 24
TS68950CFN	0 to +70°C	PLCC 28

68950-07.TBL

PIN CONNECTIONS



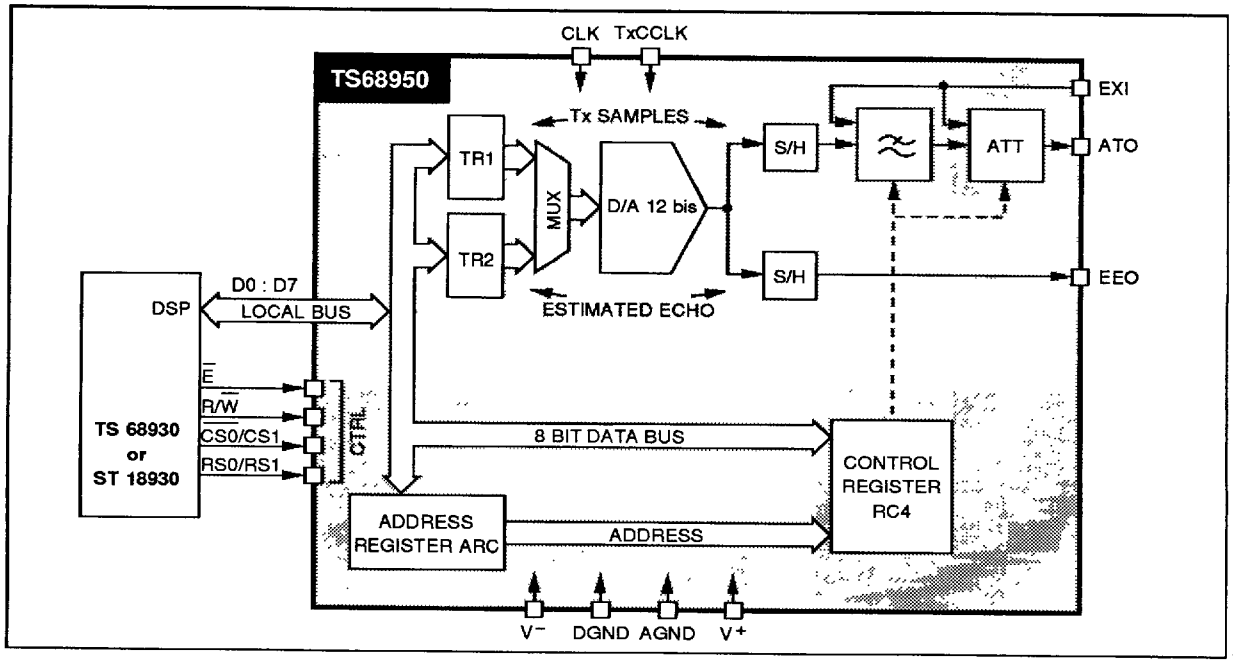
68950-01.EPS/68950-02.EPS

PIN DESCRIPTION

Name	Function
D5-D7	8 bit data bus inputs giving access to Tx, estimated echo, control and address registers
$\overline{E}$	Enable Input. Datas are strobed on the positive transitions of this input.
R/$\overline{W}$	Read/$\overline{Write}$ Selection Input. Internal registers can be written when R/$\overline{W}$ = 0. Read mode is not used.
$\overline{CS0}$-CS1	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1.
RS0-RS1	Register Select Inputs. Used to select D/A input registers or control/address registers in the write mode.
DGND	Digital Ground = 0 V. All digital signals are referenced to this pin.
TEST	Test Input. Used to reduce testing time. This Pin must be connected to DGND in all applications.
V^-	Negative Power Supply Voltage = -5V ±5%
AGND	Analog Ground = 0 V. Reference point for analog signals.
EXI	Programmable analog input tied to filter or attenuator input according to the RC4 register content.
ATO	Analog Transmit Output
EEO	Analog Echo Cancelling Output (estimated echo)
V^+	Positive Power Supply Voltage : +5V ±5%
CLK	1.44MHz Clock Input. Used for internal sequencing.
TxCCLK	Transmit Conversion Clock Input. Must be derived from CLK.
D0-D4	See pins D5-D7

68950-01.TBL

BLOCK DIAGRAM



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DEVICE OPERATION

The TS68950 is a transmit analog interface circuit dedicated to voice-grade MODEMs, telephony and speech applications. The TS68950, the TS68951 (receive analog front-end circuit) and the TS68952 (clock generator) constitute an analog front-end chip set useful for implementation of synchronous modems operating on two or four wires according to the CCITT V.26, V.26bis, V.27, V.27bis, V.27ter and V.29 recommandations or BELL 208 and 209 standards, or on two wires full-duplex according to CCITT V.22, V.22 bis or BELL 212A (split band) and CCITT V.26 ter and V.32 (echo cancelling). The chipset can also be used for asynchronous recommendations such as V.21, V.23, Bell 103.

By receiving digital samples from a DSP like the ST 8930/31, the TS68950 delivers two analog signals: the transmitted (Tx) signal that will be sent on the line and the estimated echo signal that will be subtracted from the received (Rx) signal on the TS68951 Rx chip.

The digital Tx and estimated echo samples are converted to analog during the low state and the high state of the TxCCLK clock, respectively.

Main Functions (see block diagram)

- 12-bit digital to analog converter multiplexed on two channels.
- Tx signal sample and hold running with Tx sampling frequency TxCCLK.
- Tx low-pass filter with continuous-time smoothing.
- Programmable attenuator from 0 to -22dB with 2dB steps.
- Estimated echo sample and hold running with Tx sampling frequency TxCCLK.

DSP Interface Signals

The TS68950 interfaces to the signal processor via an 8-bit data bus (only used in writing mode), two chip select lines, two register select lines, a read/write line and an enable line.

Data bus (D0-D7) - The write only data lines allow the transfer of data from the DSP to the TS68950. Input buffers are high-impedance devices.

Enable ($\overline{E}$) - The enable pulse ($\overline{E}$) is the basic timing signal that is supplied to the TS68950. All the other signals are referenced to the leading and trailing edges of the $\overline{E}$ pulse.

Read/Write (R/$\overline{W}$) - This signal is generated by the DSP to control the direction of data transfers on the data bus. A low level state on the TS68950 read/write line enables the input buffers and data is transferred from the DSP to the TS68950 on the $\overline{E}$ signal if the circuit has been selected. The device is unselected when a high level signal is applied to the R/$\overline{W}$ pin.

Chip Select ($\overline{CS0}$, CS1) - These two input signals are used to select the chip. $\overline{CS0}$ must be low and CS1 must be high for selection of the device. Data transfers are then performed under the control of the enable and R/$\overline{W}$ signals. The chip select lines must be stable for the duration of the $\overline{E}$ pulse.

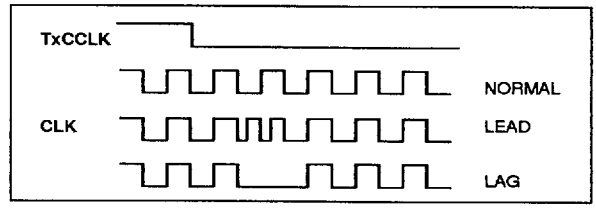
Register Select (RS0, RS1) - The two register select lines are used to access the different registers inside the chip. For instance these two lines are used in conjunction with the internal control register ARC to select a particular register RC4. The register select lines must be stable when the $\overline{E}$ signal is low.

Clock Interface between TS68950 and TS68952

The TS68950 receives two clock lines from the clock generator TS68952.

MASTER CLOCK SEQUENCING (CLK) : The typical frequency is 1.44MHz but the recurrence frequency must be an exact multiple of the terminal clock frequency. The TxDPLL included in the clock generator circuit (TS68952) operates by adding or subtracting pulses to a 2.88MHz internal clock. This corresponds to phase leads or phase lags of about 350ns duration. To ensure correct device operation, clock synchronization must be done immediately after the negative-going transition of TxCCLK clock.

Figure 1



TRANSMIT CONVERSION CLOCK (TxCCLK) : The conversion clock TxCCLK must be derived from the master clock CLK. Three nominal values are possible : 9.6kHz, 8kHz and 7.2kHz. 9.6kHz is the highest allowable frequency.

To run properly the TxCCLK clock must be a submultiple of CLK/5 :

$$TxCCLK \times 5 \times N = CLK \text{ (with N integer)}$$

This is ensured when using the TS68952 clock generator.

The sampling clock of the switched capacitor filter section is obtained by dividing the CLK frequency by five and performing internal synchronization on the leading edges of TxCCLK.

The Tx samples are converted from digital to analog during the low state of TxCCLK. The estimated echo samples are converted during the high state of TxCCLK.

Internal Controls

POWER-ON : The chip contains internal power-on reset logic to initialize the RC4 control register in order to avoid undesirable signal transmission on the telephone line with infinite attenuation.

INTERNAL ADDRESSING

RS0	RS1	Access	Write Cycle Number
0	0	TR1 Transmitted Sample Register	2
0	1	TR2 Estimated Echo Sample Register	2
1	0	ARC Address Register	1
1	1	RC4 Control Register (if addressed by ARC)	1

SAMPLE REGISTERS (TR1 AND TR2) : TR1 is the transmitted sample register and TR2 the estimated echo sample register. TR1 and TR2 store two's complement 12-bit data (DAC0 to DAC11). As indicated below, writing each sample requires two cycles.

First Cycle

D7	D6	D5	D4	D3	D2	D1	D0
DAC 3	DAC 2	DAC 1	DAC 0	X	X	X	X

Second Cycle

DAC 11	DAC 10	DAC 9	DAC 8	DAC 7	DAC 6	DAC 5	DAC 4

An internal flip-flop is used to select the first or the second byte. It advances one count on the positive-going edge of the $\overline{E}$ pulse when the sample registers are selected ($\overline{CS0}$ = 0, CS1 = 1 and RS0 = 0). When the sample registers are disabled, the latch is reset on any $\overline{E}$ positive-going edge.

Both TR1 and TR2 registers are sampled by the DAC on the falling edge of TxCCLK. Therefore their contents must remain stable during this edge.

CONTROL REGISTER (RC4) : The RC4 control register has two different functions. Its four most significant bits give the transmit attenuator gain following the table below.

RC4 REGISTER

D7	D6	D5	D4	D3	D2	D1	D0	Attenuation (dB)
ATT 4	ATT 3	ATT 2	ATT 1		EM 2	EM 1		
0	0	0	0					0
0	0	0	1					2
0	0	1	0					4
0	0	1	1					6
0	1	0	0					8
0	1	0	1					10
0	1	1	0					12
0	1	1	1					14
1	0	0	0					16
1	0	0	1					18
1	0	1	0					20
1	0	1	1					22
1	1	0	0					Infinite
1	1	0	1					Infinite
1	1	1	0					Infinite
1	1	1	1					Infinite

Depending on the EM1 and EM2 states in the RC4 register, the programmable analog input (EXI) can be connected to the filter input or to the transmit attenuator input.

RC4 REGISTER

D7	D6	D5	D4	D3	D2	D1	D0	EXI INPUT
ATT 4	ATT 3	ATT 2	ATT 1	–	EM 2	EM 1	–	
					0	0		Disabled
					0	1		Transmit Filter Input
					1	0		Transmit Attenuator Input
					1	1		Disabled

Following power-up, all RC4 bits are preset at one : EXI input is disabled and the transmit signal is cancelled.

D0 and D3 bits are not used in the RC4 register.

ADDRESS REGISTER (ARC) : The address register stores 3 bits (D5, D6 and D7). Among the 8 possible addresses, only one is used inside the TS68950 (RC4 address).

RC4

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	X	X	X	X	X

X : don't care

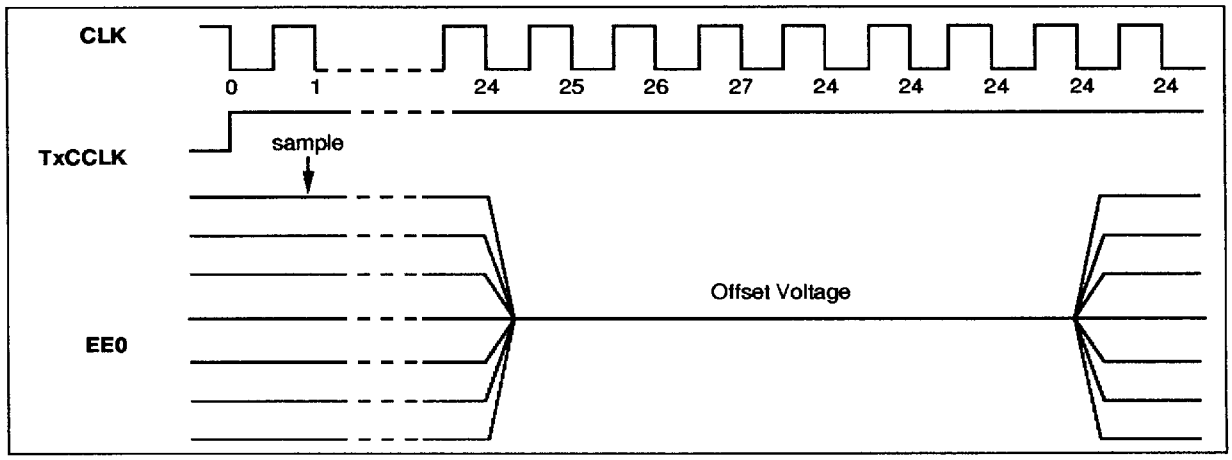
The address of the ARC register is automatically increased by one each time the control register is accessed. This allows indirect or cyclical addressing to RC4.

EEO OUTPUT WAVEFORM

The EEO output is not valid during S/H sampling. The output presents at this time the S/H offset voltage.

This offset voltage appears at the 24th CLK period after rise transition of TxCCLK and disappears at the 31th.

Figure 2



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	DGND Digital Ground to AGND Analog Ground	-0.3, +0.3	V
	V^+ Supply Voltage to DGND or AGND Ground	-0.3, +7	V
	V^- Supply Voltage to DGND or AGND Ground	-7, +0.3	V
V_I	Voltage at any Digital Input or Output	DGND -0.3, V^+ +0.3	V
V_{IN}	Voltage at any Analog Input or Output	V^- -0.3, V^+ +0.3	V
I_{OUT}	Analog Output Current	-10, +10	mA
P_{tot}	Power Dissipation	500	mW
t_{oper}	Operating Temperature	0 to +70	°C
t_{stg}	Storage Temperature	-65 to +150	°C
t_{sold}	Pin Temperature (soldering 10s)	+260	°C

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Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4.75	5	5.25	V
V^-	Negative Supply Voltage	-5.25	-5	-4.75	V
I^+	V^+ Operating Current			15	mA
I^-	V^- Operating Current	-15			mA

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DC AND OPERATING CHARACTERISTICS

Unless othewised noted, Electrical Characteristics are specified over the operating range.
Typical values are given for $V^+ = +5V$ and $T_{amb} = 25°C$.

Symbol	Parameter	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE					
V_{IL}	Input Low Level Voltage			0.8	V
V_{IH}	Input High Level Voltage	2.2			V
I_{IL}	Input Low Level Current (DGND < V_I < $V_{IL\ max}$)	-10		10	µA
I_{IH}	Input High Level Current ($V_{IH\ min}$ < V_I < V^+)	-10		10	µA
ANALOG INTERFACE, EXI PROGRAMMABLE INPUT					
V_{in}	Input Voltage Swing	-2.5		+2.5	V
I_{in}	Input Current (input Tx filter selected)	-10		+10	µA
C_{in}	Input Capacitance (input ATT selected) f < 50kHz f > 50kHz			 50 20	 pF pF
R_{in}	Input Resistance (input ATT selected)	20			kΩ
ANALOG INTERFACE, ATO TRANSMIT OUTPUT					
V_{os}	Output DC Offset	-250		+250	mV
C_L	Load Capacitance			50	pF
R_L	Load Resistance	1200			Ω
V_{out}	Output Voltage Swing (R_L > 1200Ω and C_L < 50pF)	-2.5		+2.5	V
R_{out}	Output Resistance			5	Ω
ANALOG INTERFACE, EEO ESTIMATED ECHO OUTPUT					
V_{os}	Output DC Offset	-100		+100	mV
C_L	Load Capacitance			50	pF
R_L	Load Resistance	10			kΩ
V_{out}	Output Voltage Swing (R_L > 10kΩ and C_L < 50pF)	-2.5		+2.5	V
R_{out}	Output Resistance	350	500	650	Ω
DAC TRANSFER					
	Converter Resolution		12		Bit
V_{out}(max)	Nominal Output Peak to Peak Amplitude		5.0		V
LSB	Least Significant Bit Amplitude		1.2		mV
	Integral Linearity Error	-1		+1	LSB
	Differential Linearity Error	-0.7		+0.7	LSB
TRANSMIT FILTER TRANSFER CHARACTERISTICS (see appendix 1)					
G_{AR}	Absolute Passband Gain at 1kHz		0		dB
G_{RR}	Gain Relative to Gain at 1kHz without Sin x/x Correction of DAC Sampling Below 3100Hz 3200Hz 4000Hz 5000Hz to 12000Hz	 -0.5 -3		 0.2 -36 -46	dB
D_{AR}	Absolute Group Delay (600Hz to 3000Hz)	160		680	µs
ATTENUATOR TRANSFER CHARACTERISTICS					
A_{TT}	Absolute Gain at 0dB Nominal Value		0		dB
R_{AT}	Attenuation Relative to Nominal Value	-0.5		+0.5	dB
B_{AT}	Maximum Attenuation	40			dB

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DC AND OPERATING CHARACTERISTICS (continued)

Unless othewised noted, Electrical Characteristics are specified over the operating range.
Typical values are given for $V^+ = +5V$ and $T_{amb} = 25°C$.

Symbol	Parameter	Min.	Typ.	Max.	Unit
GENERAL TRANSFER CHARACTERISTICS (from DATA BUS to ATO)					
G_{EX}	ATO Absolute Gain at 1kHz	-0.5	0	+0.5	dB
	ATO Psophometric Noise			200	µV
	ATO Positive Power Supply Rejection Ratio (V_{AC} = 200mV_{PP}, f = 1kHz)		40		dB
	ATO Negative Power Supply Rejection Ratio (V_{AC} = 200mV_{PP}, f = 1kHz)		40		dB
	Signal to Harmonic Distorsion Ratio (psophometric band)	60			dB
GENERAL TRANSFER CHARACTERISTICS (from DATA BUS to EEO)					
G_{AX}	EEO Absolute Gain at 1kHz	-0.5	0	+0.5	dB
	EEO Psophometric Noise			200	µV
	EEO Positive Power Supply Rejection Ratio (V_{AC} = 200mV_{PP}, f = 1kHz)		40		dB
	EEO Negative Power Supply Rejection Ratio (V_{AC} = 200mV_{PP}, f = 1kHz)		40		dB

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BUS TIMING CHARACTERISTICS (See Note 1 and 2) (See Figure 3)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cyc}	Cycle Time	320			ns
t_{WEL}	Pulse Width, $\overline{E}$ Low Level	180			ns
t_{WEH}	Pulse Width, $\overline{E}$ High Level	100			ns
t_r, t_f	Clock Rise and Fall Time			20	ns
t_{HCE}	Control Signal Hold Time	10			ns
t_{SCE}	Control Signal Set-up Time	40			ns
t_{SDI}	Input Data Set-up Time	120			ns
t_{HDI}	Input Data Hold Time	10			ns

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Notes : 1. Voltage levels shown are V_L < 0.4V, V_H > 2.4V, unless otherwise specified.
2. Measurements points shown are 0.8V and 2.2V, unless otherwise specified.

CLOCK TIMING CHARACTERISTICS (See Figure 4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_C	CLK Clock Period		695		ns
P_{CL}	CLK During Phase Lead on DPLL		348		ns
t_{WCL}	CLK Low Level Width	150			ns
t_{WCH}	CLK High Level Width	150			ns
t_{RC}, t_{FC}	CLK Rise and Fall Time			100	ns
t_{RT}, t_{FT}	TxCCLK Rise and Fall Time			100	ns
t_{DC}	TxCCLK Delay Time	20		130	ns

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Figure 3 : Bus Timing

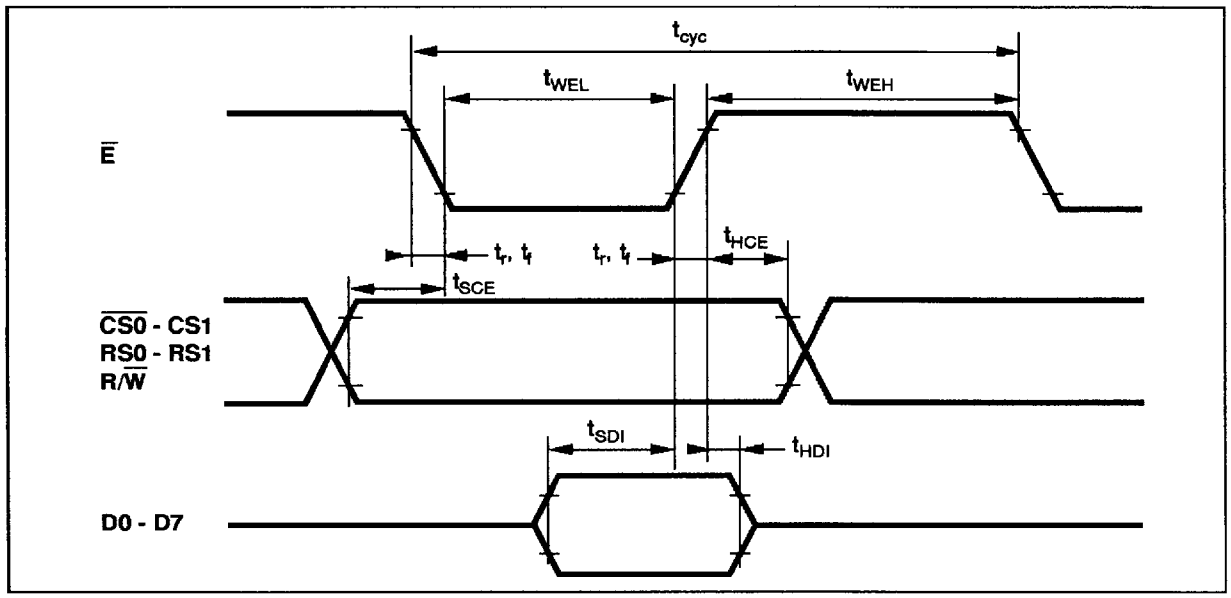
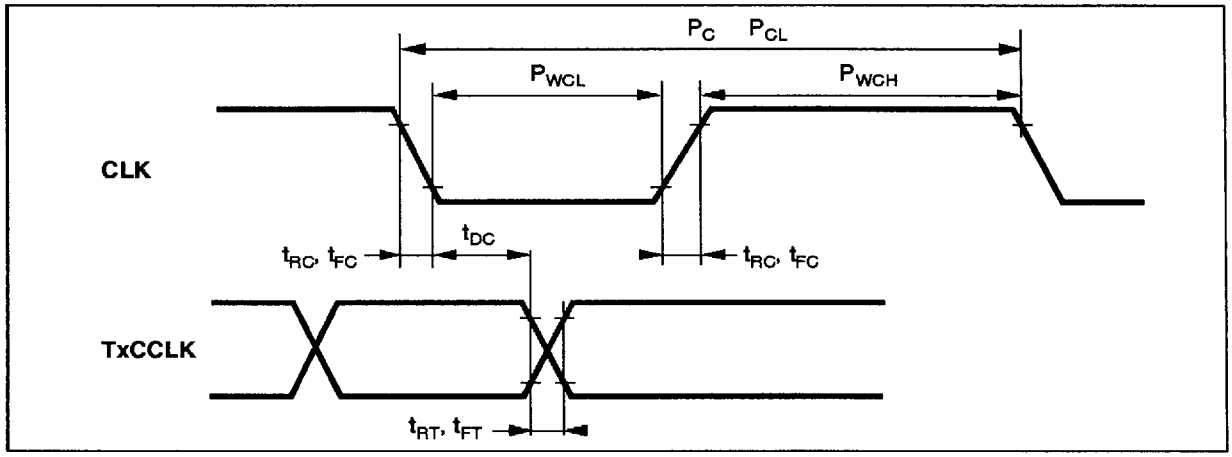
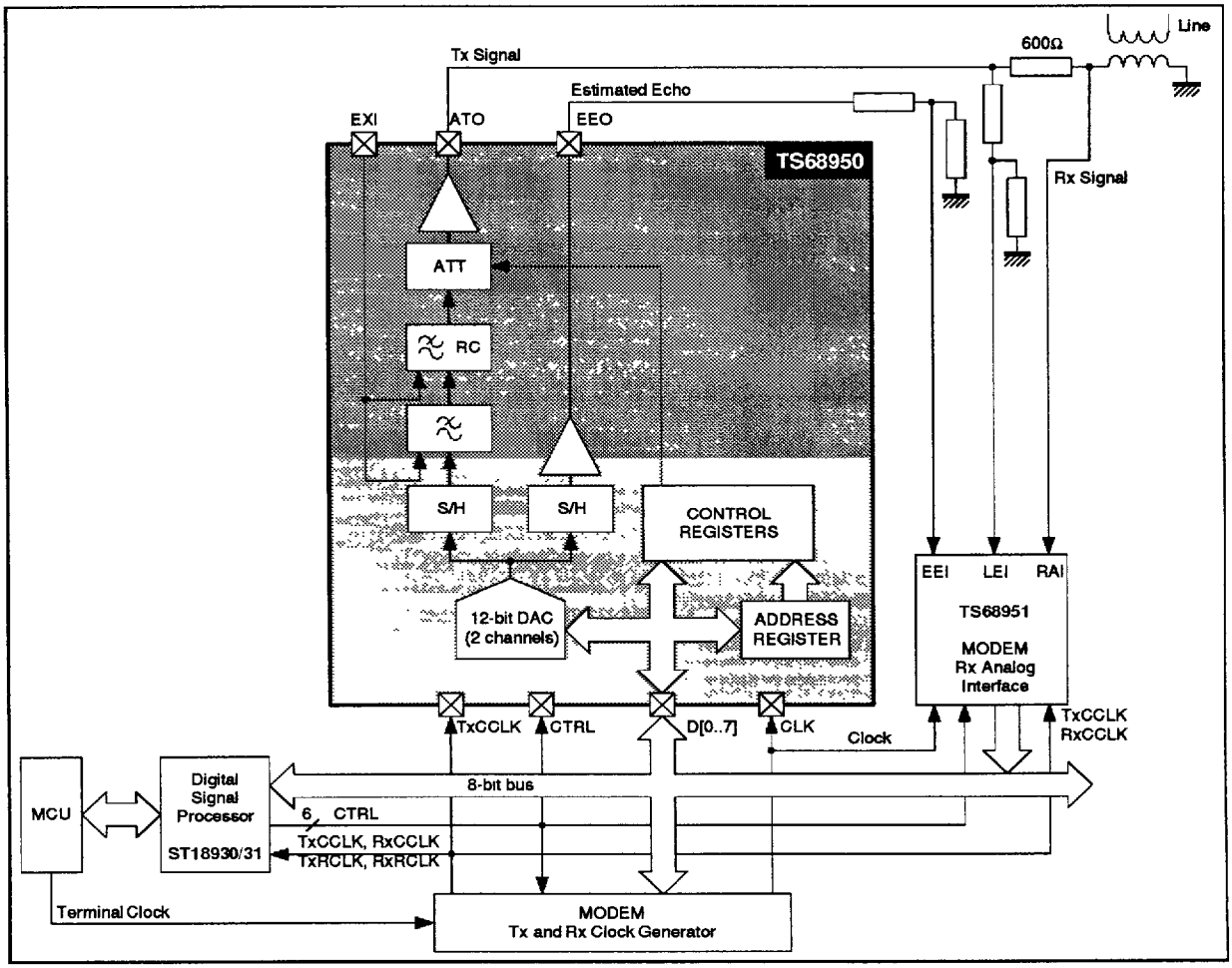


Figure 4 : Clock Timing

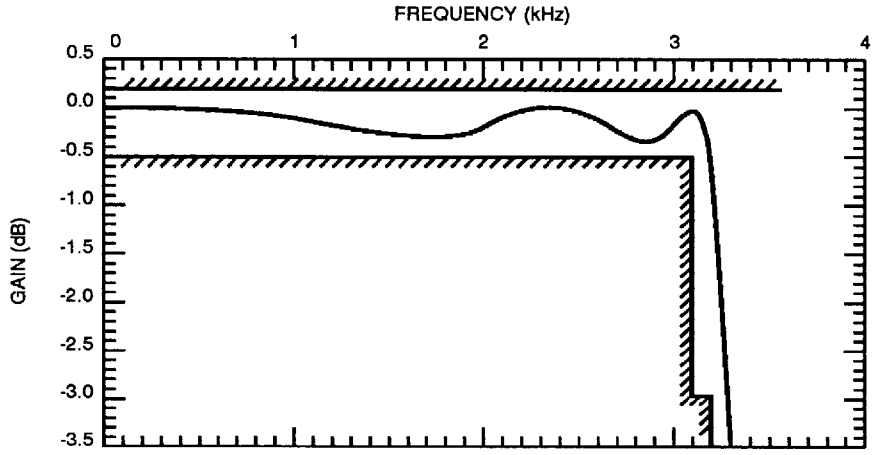


APPLICATION INFORMATION



APPENDIX 1

TRANSMIT LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART



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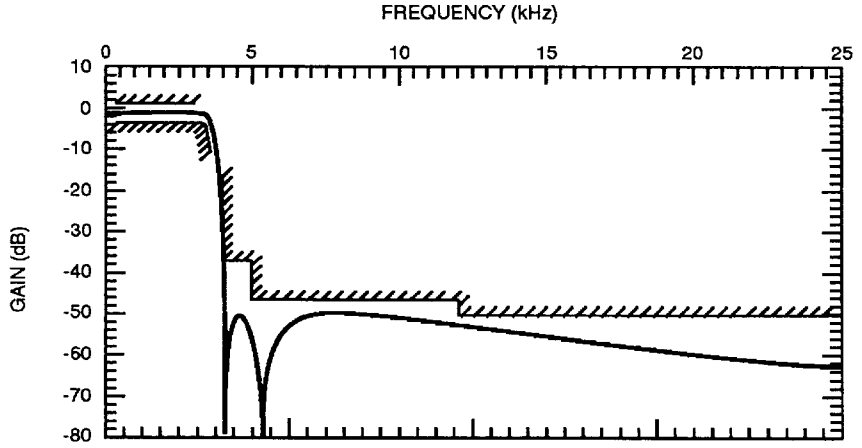
TRANSMIT LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART



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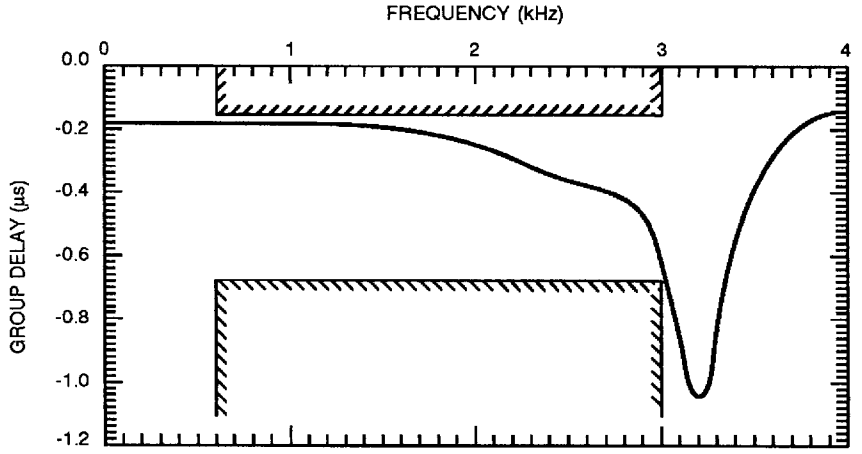
TRANSMIT LOW-PASS FILTER TYPICAL GROUP DELAY AND LIMITS CHART



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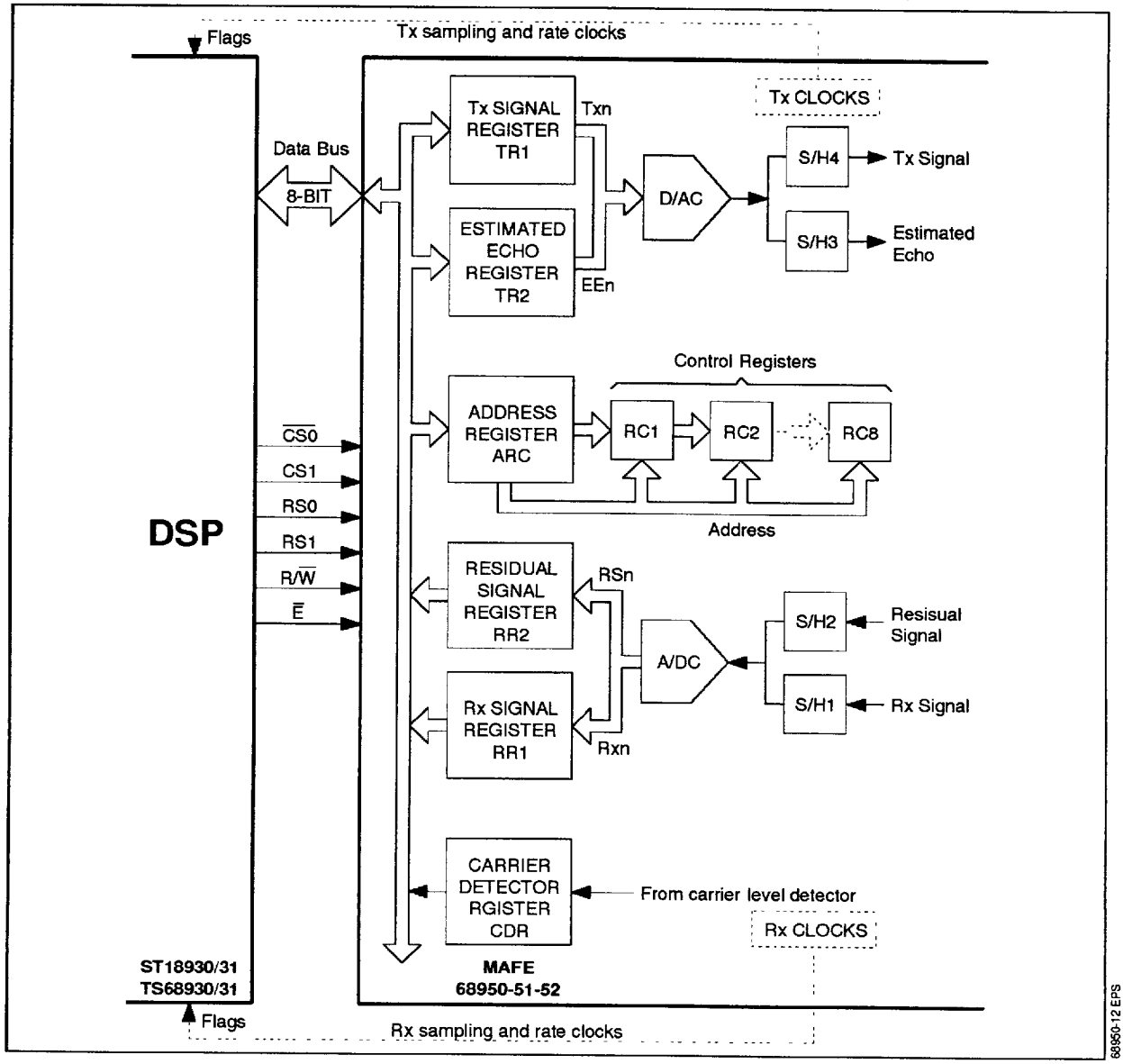
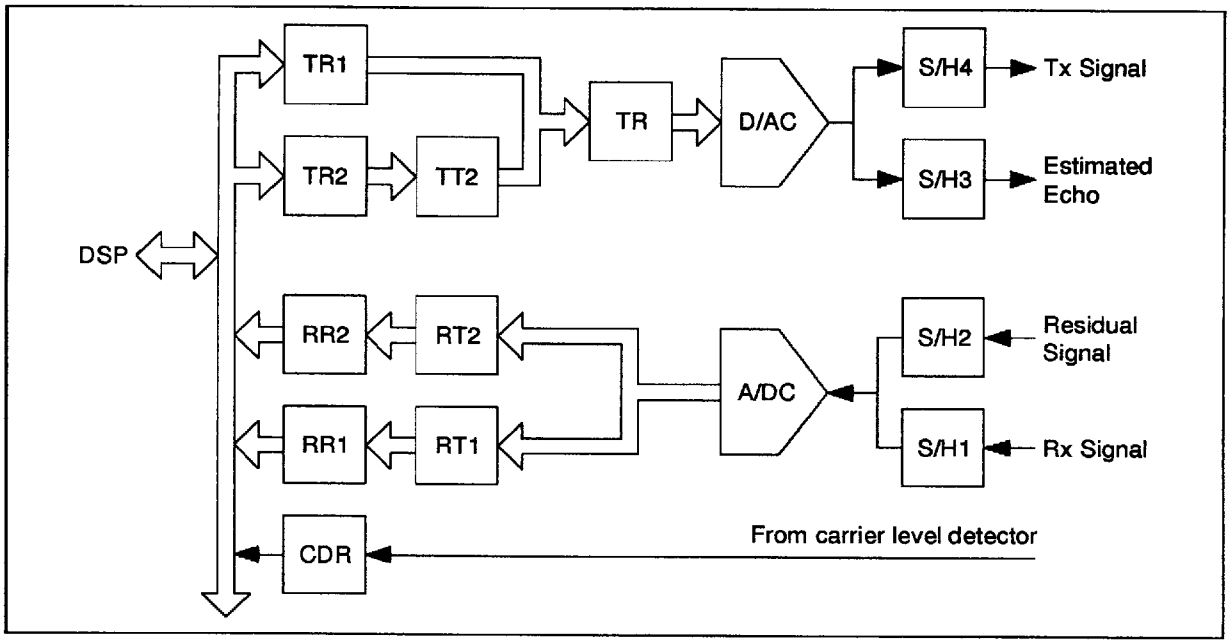
APPENDIX 2

INTERFACE BETWEEN DSP AND MODEM ANALOG FRONT-END (TS68950/51/52)



APPENDIX 3

DETAILED INPUT/OUTPUT REGISTERS DIAGRAM



68950-13 EPS

	R/$\overline{W}$	RS0	RS1	Register Accessed
Writing	0	0	0	TR1
	0	0	1	TR2
	0	1	0	ARC
	0	1	1	Control Register Addressed by ARC
Reading	1	0	0	RR1
	1	0	1	RR2
	1	1	0	CDR
	1	1	1	Not Used

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APPENDIX 4

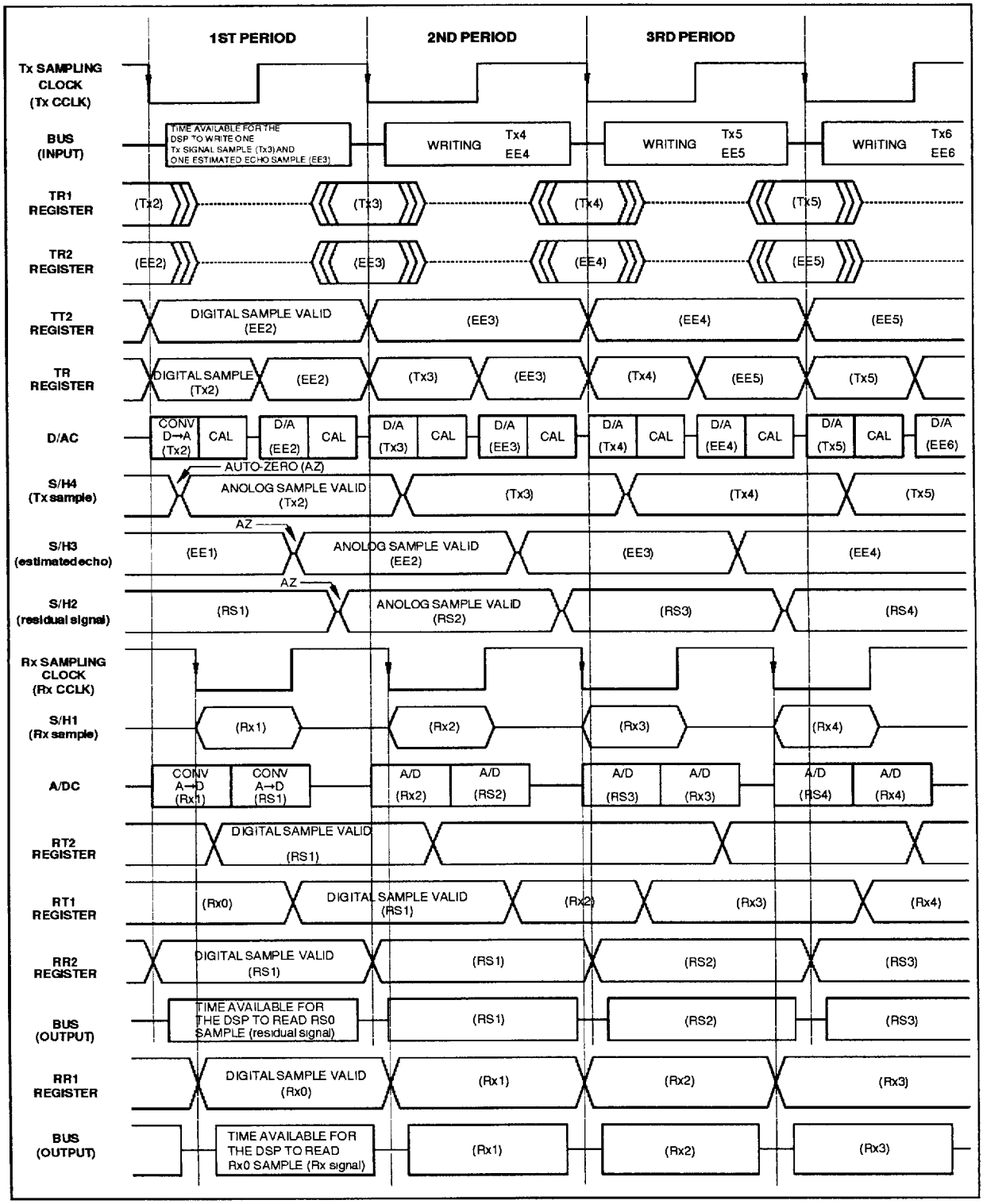
CONTROL REGISTERS PROGRAMMING

Register Name	Circuit Including this Register	Register Content								ARC Content (register address)		
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5
RC1	68952	HB4	HB3	HB2	HB1	HR3	HR2	HR1	-	0	0	1
RC2	68952	HM3	HM2	HM1	HS2	HS1	HTHR	-	-	0	0	1
RC3	68951	HP2	HP1	LP2	LP1	REJ	S/A	REC	-	0	1	0
RC4	68950	ATE4	ATE3	ATE2	ATE1	-	EM2	EM1		0	1	1
RC5	68951	GR5	GR4	GR3	GR2	GR1	-	-		1	0	0
RC6	68951	GDS2	GDS1	HDS	-	-	-	-		1	0	1
RC7	68952	SP5	SP4	SP3	SP2	SP1	-	-		1	1	0
RC8	68952	MPE	SPR	AVRE	VAL	INIT	-	-		1	1	1

68950-06 TBL

APPENDIX 5

PROGRESSION OF THE DIGITAL AND ANALOG SAMPLES IN THE MAFE



APPENDIX 6 : FURTHER REFERENCES

Mafe Characterization Report

This report gives the results of the measurements performed on the TS68950/51/52 Modem Analog Front-End (MAFE) chip set.

Chapter 1 describes the configuration and the method used for these measurements.

Chapter 2 comments the results obtained on the two signal paths of the transmit (Tx) analog front-end TS68950, i.e. the echo path and the Tx signal path Similarly chapter 3 gives the results obtained on the echo path and the receive (Rx) signal path of the Rx analog front-end TS68951

Performances obtained on the TS68951 when using plesiochronous clocks are given in chapter 4. In this case, the TS68952 clock generator delivers the main clock and the two sampling clocks to the Rx analog interface

Mafe Evaluation Board

The MAFE evaluation board is a complete unit for evaluation of the TS68950/51/52 MAFE chip set.

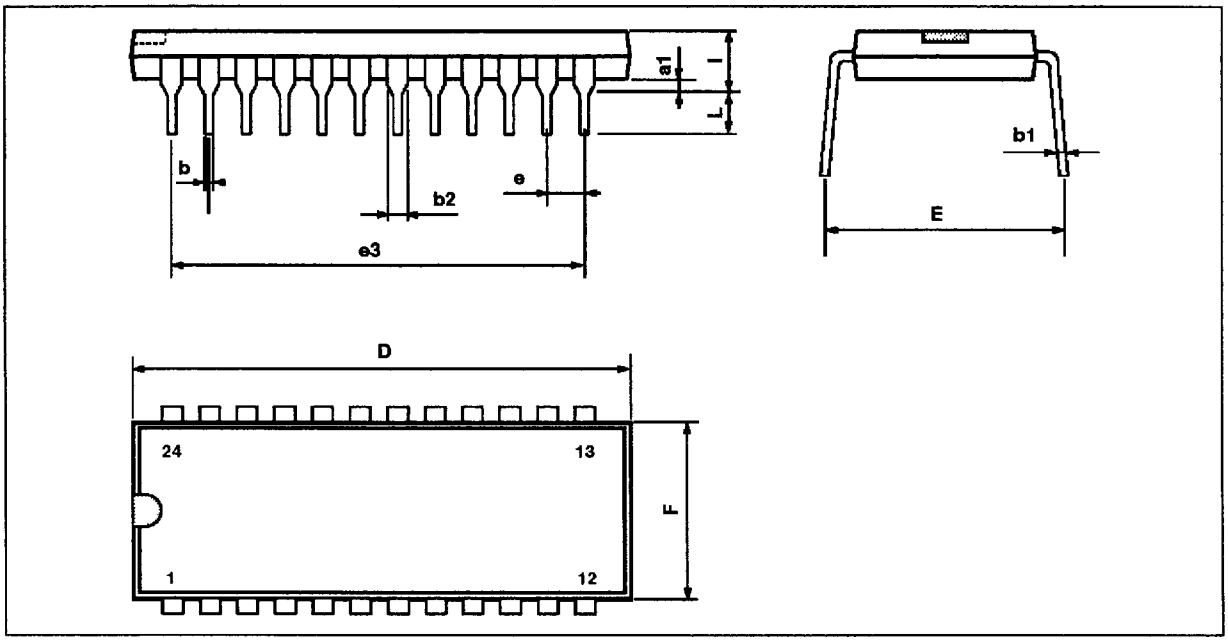
The MAFE evaluation board is equipped with the TS68950/51/52 chip set and phone line interface facilities.

It can be directly connectable to an external Digital Signal Processor through a 50-pin connector or can be linked to the SGS-THOMSOM family of digital signal processors emulation-evaluation tools. In this case, along with the software tools (MACROASSEMBLER, SIMULATOR and LINKER), it provides a ready-to-use Digital Signal Processor System Interface well adapted to the analog word and high speed modems development.

Application Note

This Application Note describes the development of Real-Time Algorithms using the SGS-THOMSON Digital Signal Processor TS68930 and the MAFE chip set.

PACKAGE MECHANICAL DATA
24 PINS - PLASTIC DIP

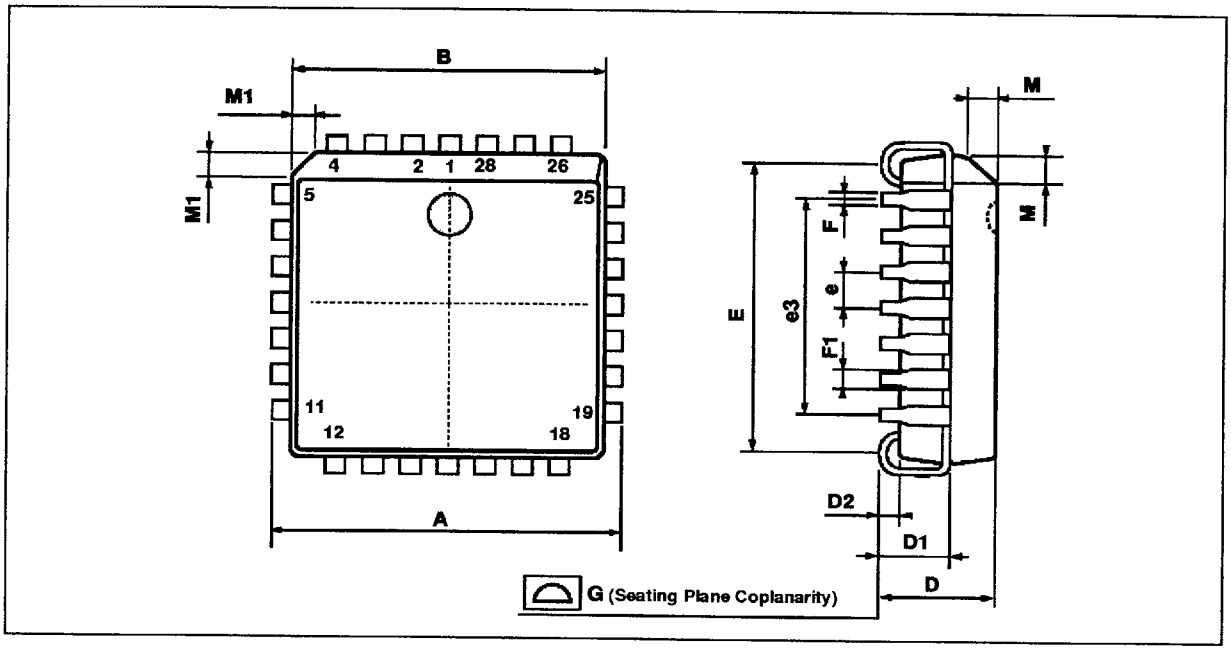


PM-DIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP24.TBL

PACKAGE MECHANICAL DATA
28 PINS - PLASTIC CHIP CARRIER



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

PLCC28 TBL

SGS-THOMSON MICROELECTRONICS