T-75-33-05

SGS-THOMSON MICROELECTRONICS

TS7524

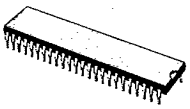
V.22 BIS, V.22, BELL 212, V.21 V.23, BELL 103 MODEM CHIP SET

S G S-THOMSON 30E D

ADVANCE DATA

- CCITT V.22 BIS COMPATIBLE MODEM CHIP SET
- CCITT V.21, V.22 AND V.23 COMPATIBLE MODEM CHIP SET
- BELL 103 AND 212 COMPATIBLE MODEM CHIP SET
- DIGITAL SIGNAL PROCESSING (TS75240) AND ANALOG FRONT-END (TS68950/51/52) IMPLEMENTATION
- QAM, DPSK AND FSK MODULATION AND DEMODULATION
- DATA TRANSMISSION SPEED :
  - 2400 bps in QAM
  - 1200 or 600 bps in DPSK
  - 1200 or 300 or 75 bps in FSK
- ADAPTIVE EQUALIZATION
- TRANSMIT AND RECEIVE FILTERING
- SHARP ADJACENT CHANNEL REJECTION
- PROGRAMMABLE TRANSMIT OUTPUT LEVELS
- ON-CHIP 4/2-WIRE HYBRID CAPABILITY
- ANSWER TONE DETECTION AND GENERATION FOR CCITT (2100 Hz), BELL (2225 Hz), AND TRANSPAC (1650 Hz) RECOMMENDATIONS
- 550 Hz AND 1800 Hz GUARD TONE GENERATION
- DTMF TONE GENERATION
- CALL PROGRESS TONE DETECTION
- SELECTABLE SCRAMBLER AND DESCRAMBLER
- DYNAMIC RECEIVE RANGE 0 TO – 48 dBm
- TYPICAL 10^{-4} B.E.R. ACHIEVED WITH A 13 dB S/N RATIO (V.22 BIS)
- ± 10 Hz FREQUENCY OFFSET CAPABILITY
- SUPPLY VOLTAGE : ± 5 V

of modems complying with CCITT V.21, V.22, V.23, and BELL 103, 212 recommendations. The modem hardware consists of a DSP chip and a 3-chip analog front end (MAFE). The modem signal processing functions are implemented on a TS68930 programmable digital signal processor, namely TS75240. The three analog front end chips (TS68950/51/52) are respectively the transmit interface, the receive interface and the clock generator.



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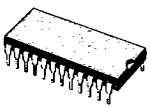
TS75240



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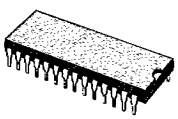
TS68950



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TS68951/2

TS68950/51/52 available in PLCC Packages

(Ordering Information at the end of the datasheet)

DESCRIPTION

The SGS-THOMSON Microelectronics multi-standard V.22 bis chip set is a high performance modem engine, which can operate up to 2400 bps in full duplex over public switched telephone network or leased lines. The TS7524 also allows implementation

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1. PIN DESCRIPTION

1.1. SYSTEM INTERFACE

TS75240 (DSP)

Name	N°	Type	Description
AD0.AD7	27.34	I/O	System Data Bus : these lines are used for transfer between the TS7524 mailbox and the control processor.
$\overline{CS}$	21	I	Chip Select : this input is asserted when the TS7524 is to be accessed by the control processor.
$\overline{RS}$	22	I	Register Select : this signal is used to control the data transfers between the control processor and the TS7524 mailbox.
$\overline{SDS}$	20	I	System Data Strobe : synchronizes the transfer between the TS7524 mailbox and the control processor.
SR/$\overline{W}$	19	I	System Read/Write : Control Signal for the TS7524 Mailbox Operation
$\overline{IRQ}$	24	O	Interrupt Request : signal sent to the control processsor to access the TS7524 mailbox.
$\overline{RESET}$	23	I	Reset of the TS7524. Must be maintened for a minimum of five clocks cycles.

1.2. ANALOG INTERFACE

TS68950 (analog front end transmitter)

Name	N°	Type	Description
ATO	15	O	Analog Transmit Output

TS68951 (analog front end receiver)

Name	N°	Type	Description
RAI	16	I	Receive Analog Input
LEI	17	I	Local Echo Input. This signal is subtracted from signal RAI.

1.3. CLOCK INTERFACE

TS68952 (clock generator)

Name	N°	Type	Description
TxCLK	23	O	Transmit Bit Clock
TxRCLK	16	O	Transmit Baud Clock
TxCCLK	24	O	Transmit Conversion Clock
TxMCLK	18	O	Additional Transmit Clock
RxCLK	22	O	Receive Bit Clock
RxRCLK	20	O	Receive Baud Clock
RxCCLK	21	O	Receive Conversion Clock
RxMCLK	19	O	Additional Receive Clock
TxSCLK	11	I	Transmit Synchro Clock : can be used to synchronize the transmitter on an external bit clock provided by the RS232C (or V 24) junction.

2. FUNCTIONAL DESCRIPTION

2.1. SYSTEM ARCHITECTURE

The SGS-THOMSON V.22 bis chip set is a highly integrated modem engine which provides the functionality and performance requirements for full-duplex 2400 bps modem solutions at a low cost with excellent performance due to digital signal processing technology. On top of the V.22 bis, the TS7524 chip set also implements the CCITT V.21, V.22, V.23 and BELL 103, 212 requirements.

The TS75240 is a programmable digital signal processor which implements the complete signal processing functions required to send and receive data according to the standard requirement and utilities such as call progress tone detection, auto-answer tone detection and tone generation.

The TS68950/51/52 MAFE (modem analog front end) is designed to meet the requirements of the whole range of voiceband modems.

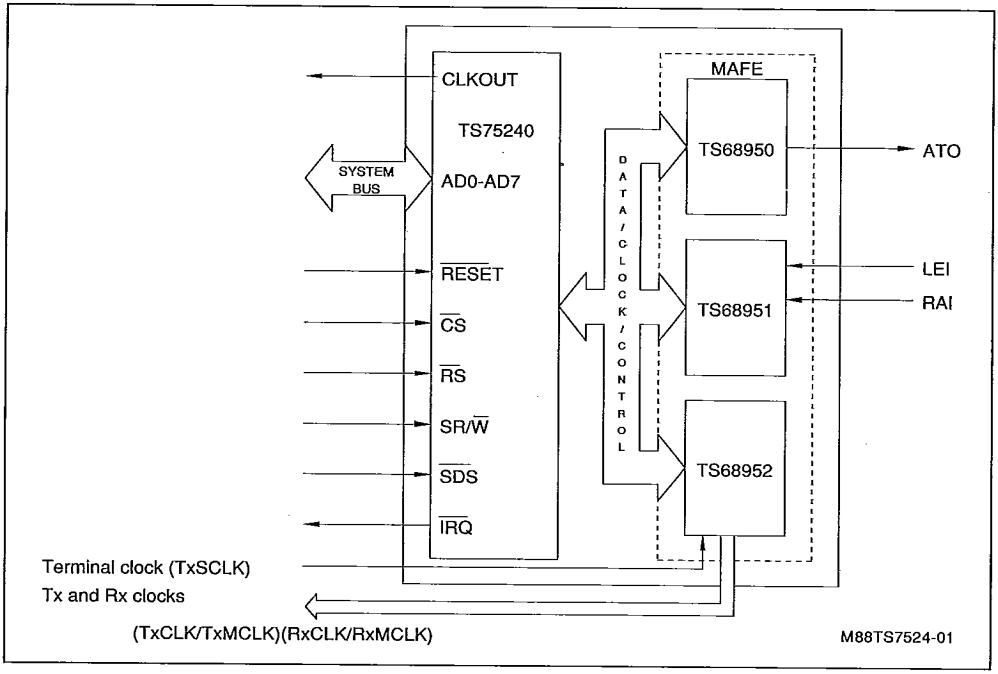
The MAFE incorporates all the required programmable gain control and clock circuitry, and signal filtering (band-limiting, anti-aliasing and smoothing filters).

Interfacing the TS7524 chip set to a control processor is very straightforward and requires no external interface circuitry.

The TS7524 chip set along with a data access arrangement (DAA), a control processor and a V.24/RS232 interface and/or an UART, is particularly well-suited for high-performance modem.

The modem supervision is insured by a control processor which implements the handshake monitoring, the auto/manual answer and dialing modes, the test modes and fall back capability and the async/sync and sync/async conversion.

Figure 1 : TS7524 Block Diagram.

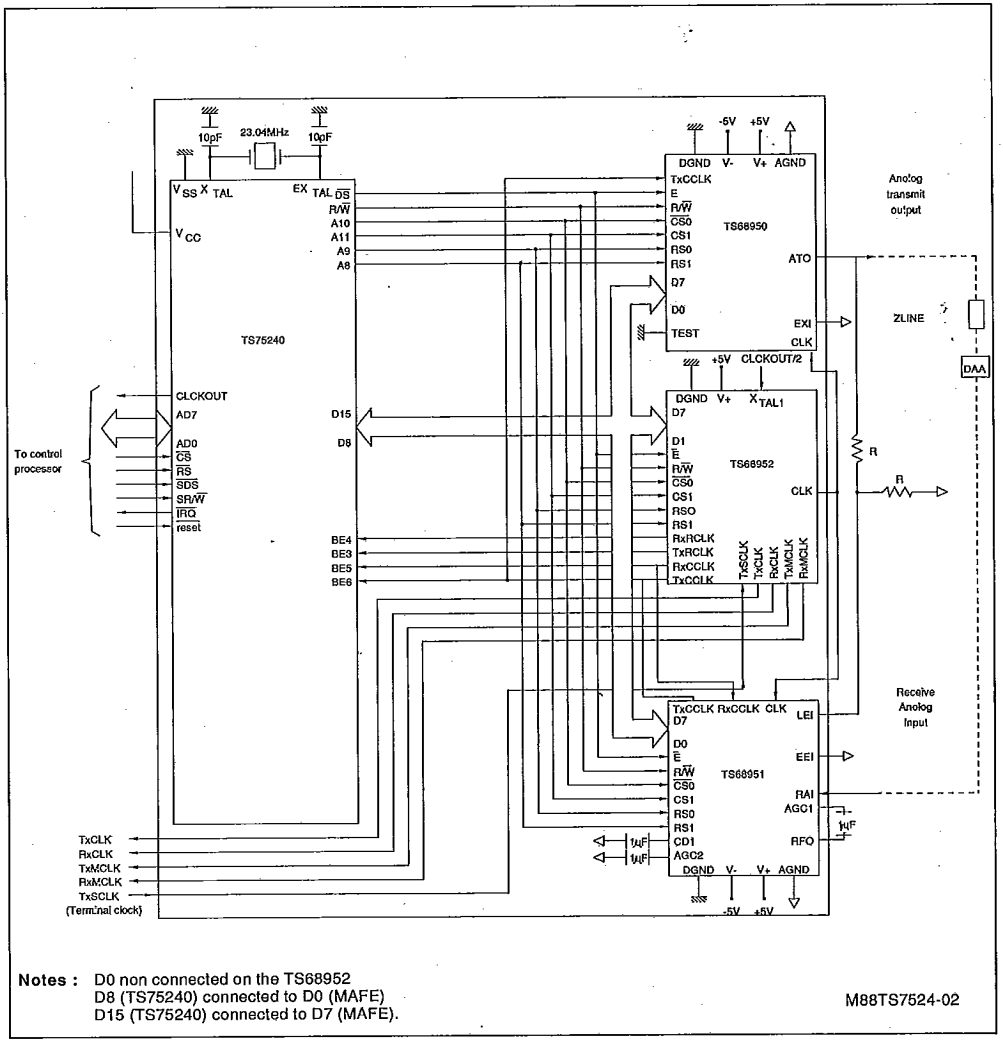


2.2. PROCESSOR AND MAFE CHIPS ARRANGEMENT

The TS75240 is connected to the analog front end chips through its local bus where D8 through D15 are the 8-bit data bus and A8 through A11 are four address lines used to address directly the three analog front end chips.

Data-Strobe (DS) is used to synchronize the transfer of data. Read/Write (R/W) indicates the direction of data. Four Branch-on-External-Condition signals (BE3 to BE6) are connected to the different clock signals issued from the clock generator interface (TS68952). They are used by the TS75240 to perform its real-time task scheduling.

Figure 2 : Interconnections between the Analog Front End Chips and the Digital Signal Processor TS75240.



Notes : D0 non connected on the TS68952
D8 (TS75240) connected to D0 (MAFE)
D15 (TS75240) connected to D7 (MAFE).

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2.3. OPERATION

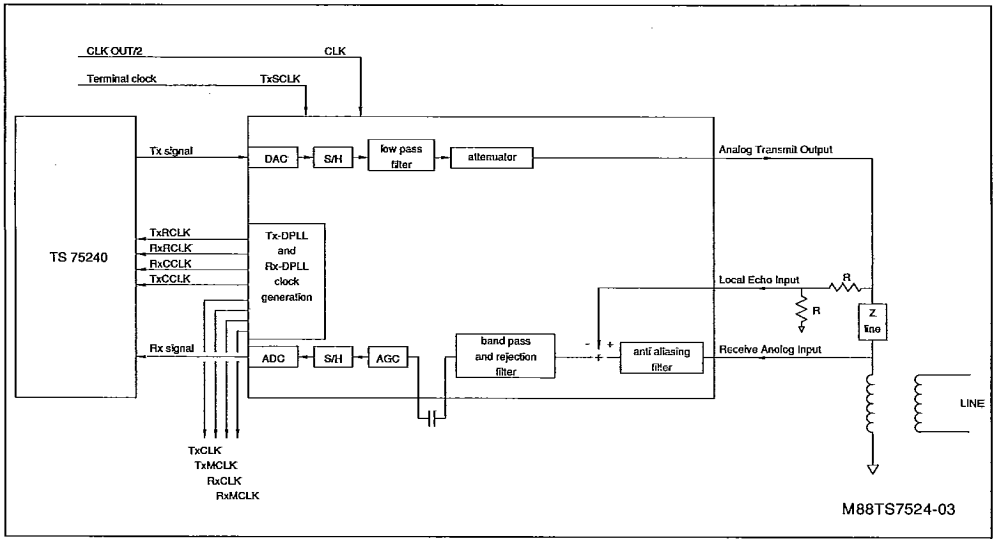
2.3.1. ANALOG FRONT END DESCRIPTION. The MAFE (TS68950/1/2) is a modem analog front end designed in three chips which performs the following functions controlled by the TS75240 digital signal processor according to the selected modem standard.

Transmit Analog Interface (TS68950) :
- 12-bit D/A converter synchronized with the sampling transmit clock.
- Low-pass and smoothing continuous-time filters
- 0 to 22 dB (or infinite) programmable attenuation.

Receive analog Interface (TS68951) :
- 12-bit A/D converter synchronized with the sampling receive clock.
- Band-pass programmable filter.
- Back channel rejection filter.
- Smoothing filter.
- 0 to 46.5 dB gain amplifier.

Clock Generation Interface (TS68952) :
- Transmit time base with programmable synchronization on data terminal equipment clock or extracted receive clock.
- Programmable receive time base DPLL.
- Four programmable plesiochronous transmit and receive clocks (rate, sampling, bit and additional clocks).

Figure 3 : MAFE Block Diagram.



2.3.2. OPERATING MODES. The modem implementation is fully compatible with different CCITT and BELL recommendations as listed in table 1. It may operate at different bit rates, from 75 bps to 2400 bps.
In case of switching from any mode to another, a reset must be applied to the TS75240 reset pin, except during the V.22 bis handshaking (the V.22 bis and V.22/BELL 212 software modules implemented in the TS75240 are compatible).

A DTMF tone generator is provided to output one of 16 standard dual tones coded by a combination of two frequencies. For specific applications where single tone is required, the DTMF generator provides the possibility to select either the high frequency or the low frequency of the standard dual tones.

A tone detector and a carrier detector respectively recognize the different answer tones (CCITT 2100 Hz, BELL 2225 Hz and Transpac 1650 Hz) and call progress tones (300 Hz to 700 Hz), as well as the presence or the absence of the on-line carrier signal (both for PSTN and leased lines).

Table 1 : TS7524 Operating Modes.

Recommendation	Bauds	BPS	Duplex	Answer	Orig	Modulation
V. 22 BIS	600	2400	Full	Yes	Yes	QAM (quadribit)
V. 22	600	1200	Full	Yes	Yes	DPSK (dibit)
BELL 212	600	1200	Full	Yes	Yes	DPSK (dibit)
V. 22	600	600	Full	Yes	Yes	DPSK (bit)
V. 21	300	300	Full	Yes	Yes	FSK
BELL 103	300	300	Full	Yes	Yes	FSK
V. 23	1200/75	75/1200	Full	Yes	Yes	FSK

2.3.3. TRANSMIT (fig. 4) :

- *V.22 bis, V.22 and BELL 212.* QAM or DPSK modulation is used to send four (V.22 bis) or two (V.22 and BELL 212) or one (V.22) bit (s) of information at 600 bauds modulation rate.

The scrambler can be bypassed, as user's option usually during the handshake procedure. After coding, a raised cosine filter (roll-off factor 0.75) performs pulse shaping and provides a 45 dB rejection between the channels so as to comply with V.22 bis, V.22 and BELL 212 standard requirements. When required, a 1800 Hz or 550 Hz guard tone can be added to the transmitted signal.

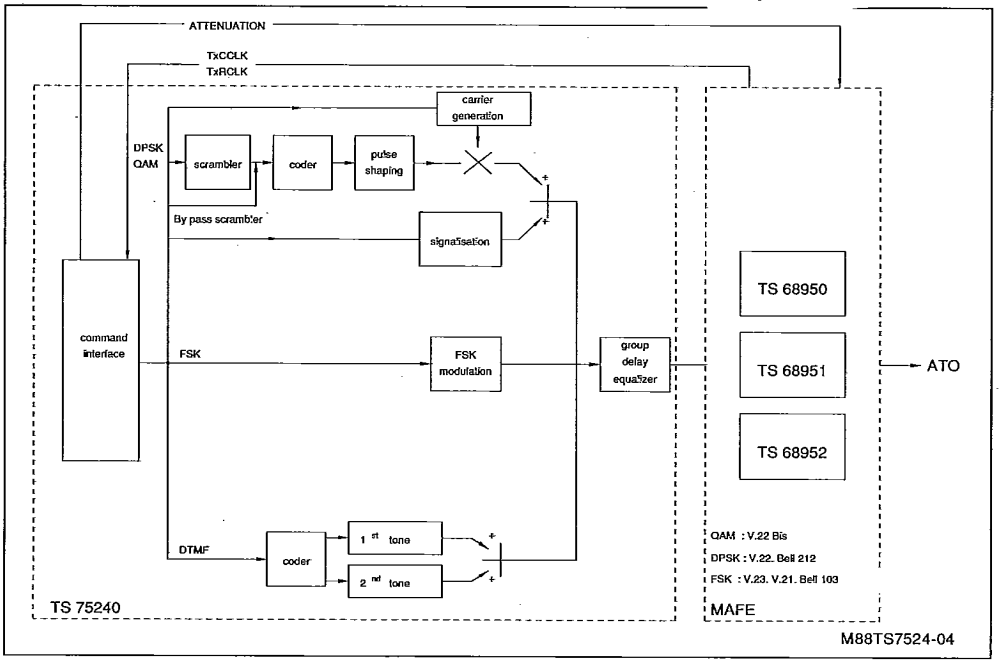
- *V.23, V.21 and BELL 103*

The FSK modulation is used to send one bit of information at 1200 or 75 baud (V.23) or 300 bauds (V.21 and Bell 103).

- *DTMF*

The DTMF generator outputs one of 16 standard dual tones synthetized by the TS75240 and selected by a 4-bit binary value as described later. Each tone is coded by a combination of two frequencies. The DTMF generator may be programmed to generate one tone at a time.
The transmit attenuation level is programmable over a 23 dB dynamic range by 1 dB steps.

Figure 4 : TS7524 Transmit Block Diagram.



2.3.4. RECEIVE (fig. 5) :

- V.22 bis, V.22 and BELL 212.

QAM or DPSK demodulation is used to receive four (V.22 bis) or two (V.22 and BELL 212) or one (V.22) bit (s) of information at 600 bauds.

- V.23, V.21 and BELL 103

The FSK demodulation is used to receive one bit of information at 1200 or 75 bauds (V.23) or 300 bauds (V.21 and BELL 103).

- Tone Detection

The TS7524 recognizes the following tones :

- 2100 Hz and 2225 Hz answer tone detection
- 1650 Hz V.21 Transpac answer tone detection
- 300 to 700 Hz call progress tone detection

Adaptive equalization, DPLL and AGC compensate for line impairments, frequency offset, group delay and amplitude distorsions.

Efficient rythm recovery algorithms provides accurate sampling on the receive signal with a variation up to $\pm 2.10^{-4}$.

Decoded data are provided in scrambled or descrambled format.

2.4. TS7524 INTERFACE (fig. 6)

2.4.1. TS7524 ANALOG INTERFACE. The transmit signal at the line interface (output ATO) is programmable over a 23 dB dynamic range by 1 dB steps through the TS75240 mailbox.

The receive signal at the line interface (input RAI) can have a dynamic range from 0 to – 48 dBm.

With a simple circuit using a minimum of external components, the TS7524 can transmit with a level of – 12 dBm on line and provide the adequate rejection of the transmit signal on the receive channel.

2.4.2. TS7524 DIGITAL INTERFACE. The interface between the TS7524 chip set and the control processor is managed by the TS75240 via its system bus and internal mailbox. The mailbox allows the control processor to read/write three consecutive data-bytes through AD0-AD7 bus. The mailbox exchanges follows the protocol described in fig. 2.4.3.

The TS75240 digital interface signals, and their definition are listed in table 2.

Figure 5 : TS7524 : Receive Block Diagram.

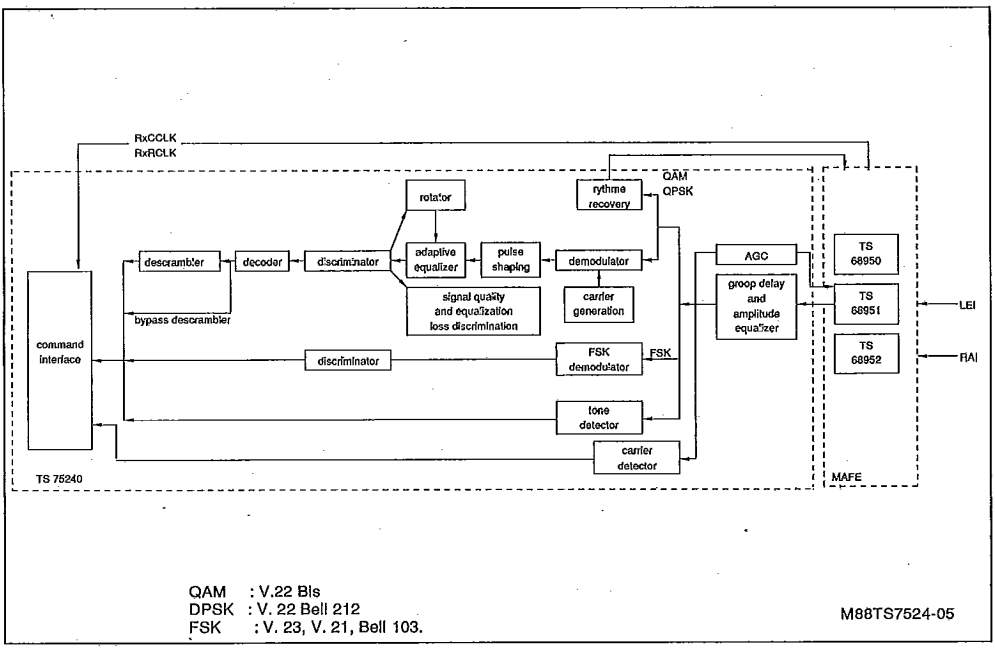
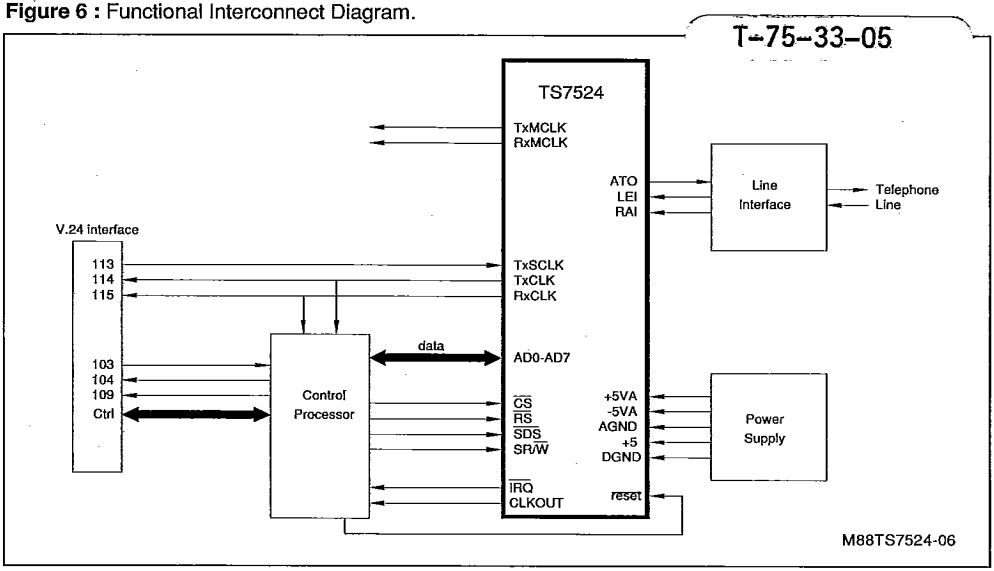


Table 2 : Digital Interface Signals.

Interface Signals	Input/output I/O	Signal Definition
AD0	I/O	Data-Bus (LSB)
AD1	I/O	Data-Bus
AD2	I/O	Data-Bus
AD3	I/O	Data-Bus
AD4	I/O	Data-Bus
AD5	I/O	Data-Bus
AD6	I/O	Data-Bus
AD7	I/O	Data-Bus (MSB)
SR/$\overline{W}$	I	Read/write Signal
$\overline{SDS}$	I	Data Strobe
$\overline{IRQ}$	O	Mailbox Handshake
$\overline{CS}$	I	TS75240 Chip Select
$\overline{RS}$	I	Register Select
$\overline{Reset}$	I	TS75240 Reset
TxMCLK *	O	Additional Transmit (2400 Hz) Clock
RxMCLK *	O	Additional Receive (2400 Hz) Clock
TxCLK	O	Transmit Bit Rate Clock
RxCLK	O	Receive Bit Rate Clock
TxSCLK	I	Transmit Terminal Clock

* These additional clocks may be used for specific applications.

Figure 6 : Functional Interconnect Diagram.



2.4.3. MAILBOX DESCRIPTION. The TS75240 requires the attention of the control processor at regular intervals in order to perform properly. The control processor must interact with the modem chip set in a timely manner to avoid improper operation.

To initialize communication exchanges between the TS7524 and the control processor, the TS7524 RESET pin must be maintained in its active (low) state during at least 870 ns (5 clock cycles) by the microprocessor. At the end of reset, the 75240 gives the mailbox control to the processor.

It is also recommended to maintain the RESET in its active state until the exchanges can start.

Following a reset the status word read from the mailbox is not significant, and the content of the command word is ignored. So, the first mailbox exchange is a dummy exchange.

The mailbox located internally to the TS75240 DSP contains 3-bytes input and 3-bytes output shift registers. The TS75240 has an internal flag which indicates whether the TS75240 or the control processor has access to the mailbox. The TS75240 can relinquish its accessability to the mailbox by setting this internal flag, but it can no longer regain access to the mailbox as the flag is reset only after the control processor relinquishes its accessability to the mailbox.

The access protocol and system bus transfers are controlled by an internal I/O sequencer within the TS75240 which operates as follows :

1/ The mailbox is made available to the control processor by the TS75240 which drives the IRQ mailbox handshake signal to the active (low) state.

2/ The control processor detects IRQ active and dummy reads the mailbox by forcing the TS75240 chip select (CS) and register select (RS) low along with the write signal (SR/W) high. The activated data strobe signal (SDS = 0) validates the above signals.

3/ The TS75240 detects the dummy read of its mailbox via the control signals mentioned in step 2 and negates IRQ mailbox handshake signal after 1 µS (at least 5 clock cycles).

4/ The control processor detects the negation of IRQ indicating that the TS75240 mailbox is available for data transfers. The control processor reads three bytes (one status word) and then writes three bytes (one command word) in the mailbox. If the status word is a transmit status word, then a transmit command word must be written into the mailbox. Else, a receive command word must be written into the mailbox.

5/ The control processor ends the exchange protocol performing a dummy read of the mailbox as in step 2 but with RS in the high state.

The TS75240 then owns the mailbox and can make it available again to the control processor as in step 1.

3. USER INTERFACE

3.1. COMMAND AND STATUS WORDS

The TS7524 chip set functionalities and status reporting are managed by the control processor through the TS75240 mailbox, according to the protocol outlined earlier.

The command words are issued by the control processor and received by the TS75240.

The command words provide the necessary functional control of the TS7524 chip set.

The status words are issued by the TS75240 and delivered to the control processor.

The status words provide the status reporting.

Each command and status word of both the transmit and receive part comprises three bytes as described in the following sections.

The control processor must be able to handle :

- one mailbox transfer per transmit baud period and,
- one mailbox transfer per receive baud period.
- these transfers are plesiochronous. (Tx and Rx clocks have the same nominal frequency but can shift of $\pm 1.10^{-4}$, so the phase relation between Tx and Rx is time varying).

3.2. TRANSMIT AND RECEIVE COMMAND WORDS

Both the transmit and receive command words are built on the same programming model, but have to be programmed completely independently.

3.2.1. TRANSMIT COMMAND WORD. The table 3 shows the transmit command word (three bytes) programmation and transmit functionalities.

The first byte of the transmit command word permits the choice of the DTMF mode or the selection of the requested CCITT (with or without guard tone) or BELL standards.

The second byte contains the transmit parameters information register.

The third byte is the transmit data register of DTMF tone selection register. In this byte is also included the transmit enable bit which instructs the TS7524 to transmit (or not) data to the line.

To manage the TS7524 in an efficient way, it is recommended to work with a table stored in the control processor memory space. This table will reflect the three bytes of the transmit command word and will be sent from the control processor to the TS7524 at

Table 3 : Transmit Command Word Format.

BIT	First Byte	Second Byte	Third Byte				
0	Transmit Mode Selection		Transmit (0)				
1	0000 : Modem Disabled 0001 : V.22 Bis		D0	DPSK	QAM	FSK	DTMF
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21	Transmit Attenuation	D1				
3	0110 : Bell 103 0111 : D.T.M.F.		D2	0			
4	Transmit Signalling 00 : Signalling Disabled		D3	0			
5	01 : 550 Hz 11 : 1800 Hz	Scrambler (ON/$\overline{\text{OFF}}$)	D4	0	0		0
6	**Reserved**	**Reserved**	D5	0	0		0
7	$\overline{\text{ANSW}}$/ORIG or DTMF	V.22 Binary Rate Select or DTMF	$\overline{\text{Transmit Enable}}$				

Note : All the "RESERVED" bits must be cleared to "0" by the user.

each transmit baud. In this table, the different fields could be programmed according to the CCITT or BELL standard needed taking into account the transmit parameters. Once the contents of the first and second byte have been determined for the whole transmission, only the transmit data field in the third byte has to be updated in the table. So, at each transmit baud, the TS75240 will receive the complete three bytes, will check them and send the data.

FIRST BYTE :

Bit 3, 2, 1 and 0 : Transmit mode selection

These bits select the standard to use or the DTMF mode

0000	: Modem disabled
0001 to 0110	: Transmit mode selection
0111	: DTMF.In this mode, the number which may be dialed is given by the proper binary combination of bits 4, 3, 2 and 1 in the third byte. Refer to paragraph "DTMFmode" for detailed information.

Other bit codes are reserved.

Bit 5 and 4 : Transmit Signalling

These bits represent the tone to send regarding the requested functionalities.

00	: Signalling disabled
01 or 11	: Guard tone 550 Hz or 1800 Hz which can be added to the modulated signal.
10	: Reserved

Bit 6 : Reserved

Bit 7 : $\overline{\text{ANSWER}}$ / ORIGINATE or DTMF

This bit has two main functions. Its first function is to select the answer or originate mode. The second function is used in DTMF mode as explained in details in paragraph "DTMF mode".

In $\overline{\text{ANSWER}}$/ORIGINATE mode, the bit 7 cleared to zero selects the answer mode (transmit in high channel). The bit 7 set to one selects the originate mode (transmit in low channel).

SECOND BYTE :

Bit 4, 3, 2, 1, and 0 : Transmit attenuation

The transmit levels without attenuation at the transmit interface output (ATO) on 600 ohms are as follows :

- in FSK modes (V.23, V.21 and BELL 103)
  - 0 dBm
- in QAM (V.22 bis) and DPSK (V.22 and BELL 212) modes
  - 5 dBm when transmission on low channel
  - 4 dBm when transmission on high channel with guard tone composed by :
    - 5 dBm (signal)
    - 12 dBm (guard tone)
  - 5 dBm when transmission on high channel without guard tone
- 4 dBm in DTMF mode composed by
  - 5 dBm (high frequency)
  - 7 dBm (low frequency)

These are maximum levels which can be decreased by programming the transmit attenuation, with attenuation levels falling within 0 dB (00000) and 23 dB (10111) range, selectable in 1 dB steps.

Selection within 11000 to 11111 correspond to an infinite attenuation.

At power-on, or after a reset applied on the reset pin of the TS75240, an infinite attenuation is automatically programmed.

Bit 5 : Scrambler

The TS7524 incorporates an auto-synchronized scrambler/descrambler in accordance with CCITT V.22 bis and V.22 and BELL 212 recommendation.

The scrambler is enabled (1) or disabled (0) by programming the bit 5.

When the scrambler is enabled, the input data is scrambled by dividing the data by a generating polynomial as defined in the V.22 bis and V.22 recommendations.

When the scrambler is disabled, the input data is routed around the scrambler in the transmit path.

Bit 6 : Reserved

Bit 7 : V.22 binary rate selection or DTMF

This bit has two main functions. Its first function allows the possibility to select the lowest binary rate (V.22 at 600 bps) when set to one, or the highest binary rate (V.22 at 1200 bps) when cleared to zero.

The second function is used in DTMF mode as explained in details in paragraph "DTMF mode".

THIRD BYTE :

Bit 0 : Transmit

This bit indicates the nature of the command word. It must be cleared to zero by the control processor to indicate to the TS7524 that the command word is a transmit command word, and that the 3-bytes written in the mailbox contain transmit information.

Bit 6 Thru 1 : Transmitted data or DTMF tone selection. These bits have two main functions. The first function is to represent the data which will be sent according to the appropriate mode. The second function, used in DTMF mode, is to select by programming the bits 4, 3, 2, and 1 the generated tone which will be used to dial the proper number as shown in paragraph "DTMF mode" in table 5.

In QAM (V.22 bis) or DPSK (V.22 or BELL 212) modes, the bits 4, 3, 2, and 1 represent the data sent by the TS7524. According to the selected mode, up to 4 bits will be used :

- In V.22 bis, each symbol (baud) is coded by 4 bits (quadribit)
- In V.22 at 1200 bps and BELL 212 modes, each symbol is coded by 2 bits (dibit)
- In V.22 at 600 bps, each symbol is coded by only one bit.

In these modes, the mailbox exchanges are executed at the rate of 600 exchanges per second.

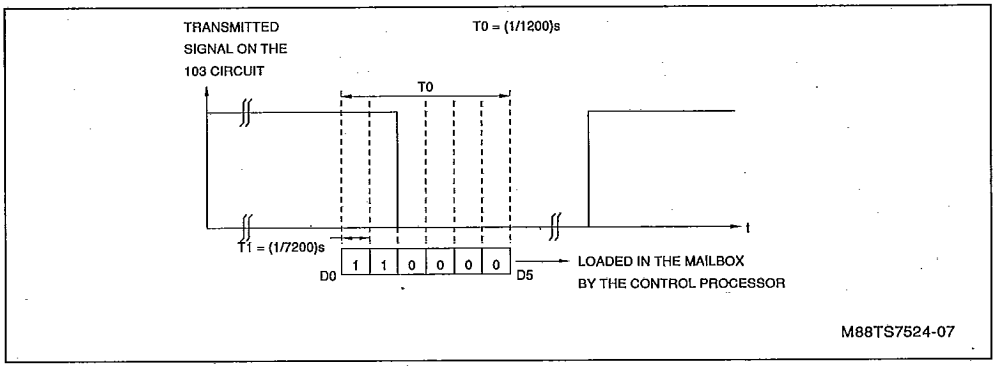
In FSK modes (V.21, V.23, and BELL 103) all the 6 bits (bit 6 thru 1) are used to represent the binary value of six samples of the transmitted signal. In these modes, the mailbox exchanges are executed at the rate of 1200 exchanges per second. Consequently, to perform a serial to parallel conversion the control processor has to sample the 103 circuit of the V.24/RS232 junction at 7.2 kHz which is the sampling clock frequency (TxCCLK).

The bit 1 (which correspond to D0) is the first sample of the signal transmitted over the line as shown in figure 7.

Bit 7 : transmit enable

This bit low instructs the TS7524 to send data.

Figure 7 : FSK Mode.



DTMF MODE

The DTMF generator outputs one of 16 standard dual-tones. For specific applications where single tone is required, the DTMF generator provides the possibility to select either the high frequency or the low frequency of the standard dual tones.

All the bytes used to program the DTMF mode and mentioned in this section are those of the transmit command word.

The DTMF mode is selected by programming bits 3 to 0 in the first byte.

Choosing the dual-tone mode, which is the normal operating mode, is done with bit 7 in the second byte cleared to zero. The DTMF generator then outputs one of the sixteen standard dual tones selected through bits 4 to 1 in the third byte as shown in table 5.

The single-tone mode is selected by setting to 1 the bit 7 in the second byte. This mode is used in specific cases where one frequency is to be generated. After one frequency pair is selected through bits 4 to 1 in the third byte as shown in table 5, the choice of the higher or lower frequency is made through bit 7 of the first byte. When bit 7 is set to 1 (respectively 0), the lower (respectively higher) frequency is generated.

In DTMF mode, the mailbox exchanges are executed at the rate of 1200 exchanges per second.

The programming of DTMF mode is summarized in table 4.

Table 4 : DTMF (dual or single tone) Programmation.

DTMF	First Byte Bits 3, 2, 1, 0		2nd Byte Bit 7	Third Byte Bits 4, 3, 2, 1
Dual-tone	0111		0	4-bit Binary Value Coding one of 16 Dual Tone
Single-tone	First Byte Bit 7	Bits 3, 2, 1, 0	2nd Byte Bit 7	Third Byte Bits 4, 3, 2, 1
High Frequency Selected	0	0111	1	4-bit Binary Value Coding one of 16 Dual Tone (high)
Low Frequency Selected	1	0111	1	4-bit Binary Value Coding one of 16 Dual Tone (low)

In DTMF mode the transmit levels at the analog transmit interface output (ATO) are respectively −5 dBm for the high group frequencies, and −7 dBm for the low group frequencies. These are maximum levels and can be decreased by programming the transmit attenuation in the second byte.

Table 5 : Tone Encoding.

Number to Dial	DTMF Code in Third Byte Generated Tones (Hz)						
	Bit4	Bit3	Bit2	Bit1	Low		High
0	0	0	0	0	941	&	1336
1	0	0	0	1	697	&	1209
2	0	0	1	0	697	&	1336
3	0	0	1	1	697	&	1477
4	0	1	0	0	770	&	1209
5	0	1	0	1	770	&	1336
6	0	1	1	0	770	&	1477
7	0	1	1	1	852	&	1209
8	1	0	0	0	852	&	1336
9	1	0	0	1	852	&	1477
A	1	0	1	0	697	&	1633
B	1	0	1	1	770	&	1633
C	1	1	0	0	852	&	1633
D	1	1	0	1	941	&	1633
*	1	1	1	0	941	&	1209
#	1	1	1	1	941	&	1477

The accuracy of the frequencies is $\pm 10^{-4}$.
The harmonic rejection level is at − 65 dB.

ANSWER TONE GENERATION

The TS7524 chip set may generate four different standard frequencies which represent the usual auto answer tones.

- 1300 Hz : V.23 Automatic connection tone
- 1650 Hz : V.21 Transpac specific answer tone
- 2100 Hz : CCITT V.22 bis, V.22, V.23 and V.21 answer tone
- 2225 Hz : BELL 212 and BELL 103 answer tone

For answer tone generation, mailbox exchanges are executed at the rate of 1200 exchanges/second.

Table 6 : Answer Tone Generation.

Tone	FSK Mode to Use	First Byte Bit 7	First Byte Bits 3, 2, 1, 0	Third Byte Bits 6, 5, 4, 3, 2, 1
1300 Hz	V. 23 Answer	0	0100	111 111
1650 Hz	V. 21 Answer	0	0101	111 111
2100 Hz	V. 23 Answer	0	0100	000 000
2225 Hz	B103 Answer	0	0110	111 111

3.2.2. RECEIVE COMMAND WORD. In the receive command word, the first byte permits the choice of the call progress and answer tone detection modes or the selection of the requested CCITT or BELL standards.

The second byte defines additional receive parameters.

The third byte informs the TS7524 that the command word is a receive command word.

To manage the TS7524 in an efficient way, it is recommended to work with a table stored in the control processor memory space. This table will reflect the three bytes of the receive command word and will be sent from the memory by the control processor to the TS7524 at each receive baud. In this table, the different fields could be programmed according to the CCITT or BELL standard needed taking into account the receive parameters. At each receive baud, the TS75240 will receive and processes the complete three bytes.

Table 7 : Receive Command Word Format.

BIT	First Byte	Second Byte	Third Byte
0	Receive Mode Selection	Reserved	Receive (1)
1	0000 : Modem Disabled 0001 : V.22 Bis 0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21 0110 : Bell 103 0111 : Call Prog. / Answer Tone		Reserved
2			
3			
4	Answer Tone Selection		
5	Tx Synchronization	Descrambler (ON/$\overline{OFF}$)	
6	Carrier Detect Level	Reserved	
7	$\overline{Answer}$/originate	V.22 Binary Rate Select	

Note : All the "RESERVED" bits must be cleared to "0" by the user.

FIRST BYTE :

Bit 3, 2, 1, and 0 : Receive mode selection

These bits select the standard to use or the call progress and answer tone detection mode.

0000 : Modem disabled
0001 to 0110 : Receive mode selection
0111 : Call progress and answer tone detection mode. In this mode the TS7524 recognizes different tones as explained in paragraph "call progress and answer tone detection"
Other bit codes are reserved.

Bit 4 : Answer tone selection

This bit defines the answer tone to be detected. It selects either 1650 Hz (Transpac) or 2100/2225 Hz answer tone. When high, the detect answer tone is 1650 Hz. When low, the detect answer tone is 2100/2225 Hz.

Bit 5 : Tx synchronization signal programming

This bit allows synchronization of all transmit clocks on a selected source. When bit 5 is set to 1, all the TS7524 transmit clocks (TxCLK, TxCCLK, TxRCLK, TxMCLK) are synchronized on TxSCLK input (typically a terminal clock signal coming from

the V.24/RS232 interface). This avoids overspeed and maintains a complete synchronization during the transmission. If there is no signal on TxSCLK coming from the terminal clock, the transmit clocks are free-running at their nominal frequencies.

When the bit 5 is set to 0, the TS7524 transmit clocks are synchronized on the receive clocks. This possibility may be used for remote digital loopback.

Bit 6 : Carrier detection level

The TS7524 can be used both on the public switched telephone network (PSTN) and with leased lines.

When the bit 6 is set to 0, the carrier detection threshold are :

– 43 and – 48 dBm (PSTN).

When the bit 6 is set to 1, the carrier detection threshold are :

– 33 and – 38 dBm (leased lines).

Bit 7 : $\overline{\text{Answer}}$ / originate

The bit 7 cleared to zero selects the answer mode (receive in low channel). The bit 7 set to one selects the originate mode (receive in high channel).

SECOND BYTE :

Bit 4, 3, 2, 1, and 0 : Reserved (must be cleared to 0)

Bit 5 : Descrambler

The TS7524 incorporates an auto-synchronized scrambler/descrambler in accordance with CCITT V.22 bis and V.22 and BELL 212 recommendation.

The descrambler is enabled when bit 5 is set to 1, or disabled when bit 5 is set to 0.

When the descrambler is enabled, the data stream is multiplied by the same polynomial that divided the data at the scrambler in the transmission path.

When the descrambler is disabled, the data stream is routed around the descrambler in the receive path.

Bit 6 : Reserved (must be cleared to 0)

Bit 7 : V.22 binary rate select

This bit allows the possibility to select the lowest binary rate (V.22 at 600 bps) when set to one, or the highest binary rate (V.22 at 1200 bps) when set to zero.

THIRD BYTE :

Bit 0 : Receive

This bit indicates the nature of the command word. It must be set to one to indicate to the TS7524 that the command word is a receive command word. This involves that the 3-bytes written in the mailbox by the control processor to the TS7524 contain receive command information.

Bit 7 Thru 1 : Reserved (must be cleared to 0)

3.3. TRANSMIT AND RECEIVE STATUS WORD

The status words are issued by the TS75240 and provide the status reporting to the control processor.

3.3.1. TRANSMIT STATUS WORD

Table 8 : Transmit Status Word Format.

BIT	First Byte	Second Byte	Third Byte
0	Transmit (0)	Reserved	Reserved
1	Reserved		
2			
3			
4			
5			
6			
7			

FIRST BYTE :

Bit 0 : Transmit

This bit when low informs the control processor that the status word issued by the TS7524 is a transmit status word.

Bit 7 Thru 1 : Reserved

SECOND BYTE :

Bit 7 Thru 0 : Reserved

THIRD BYTE :

Bit 7 Thru 0 : Reserved

3.3.2. RECEIVE STATUS WORD

Table 9 : Receive Status Word Format.

BIT	First Byte		Second Byte	Third Byte			
0	Receive (1)		Reserved	Reserved			
1	D0	Data Before		D0	Data	D0	Data (F.S.K.)
2	D1	Descrambling		D1	After	D1	
3	D2	(Q.A.M. , D.P.S.K.)		D2	Descr.	D2	
4	D3		Equallzation Status	D3	(Q.A.M., D.P.S.K.)	D3	
5	Reserved		$\overline{\text{Signal Quality}}$	1		D4	
6	S1 Sequence		$\overline{\text{Carrier Detect}}$	1		D5	
7	$\overline{\text{S1 Sequence or Call Progress Tone Detection}}$		Reserved	$\overline{\text{Answer Tone Detection}}$			

Note : In QAM and DPSK modes, both for the data after and before descrambling, the unused bits are set to "1" by the TS7524.

FIRST BYTE :

Bit 0 : Receive

This bit set to one by the TS7524 indicates to the control processor that the current status word is a receive status word.

Bit 4, 3, 2, and 1 : Data before descrambling

Used only in QAM and DPSK modes, these four bits represent the data received before descrambling, i.e., after the demodulator and before the descrambler. Data is coded on four bits (D3, D2, D1, D0) in V.22 bis, on two bits (D1, D0) in V.22 at 1200 bps and BELL 212, on only one bit (D0) in V.22 at 600 bps. The unused bits are set to 1 by the TS7524.

The mailbox exchange rate between the TS75240 and the control processor is done at 600 exchanges per second. Both for QAM and DPSK modes, D0 (which correspond to the bit 1) is the first bit received.

Bit 5 : Reserved

Bit 7 and 6 : S1 handshake sequence (V.22 bis) mode

During the V.22 bis handshake sequence, these two bits indicate the presence or the absence of the "S1" sequence detected by the TS7524. If the TS7524 gives an alternance (at each baud period in reception) of values "10" and "01" on bit 7 and 6, the "S1" sequence is present in reception. Else, this means its absence.

Bit 7 : Call progress tone detection (call progress/answer tone mode).

This bit low indicates detection of energy in the band 300 – 700 Hz with a detection threshold of – 43 dBm. This bit high means there is no energy detected. (see paragraph call progress and answer tone detection).

SECOND BYTE

Bit 3, 2, 1, and 0 : Reserved

Bit 4 : Equalization status

This bit will go high (1) in case of equalization loss (retrain sequence initialization or fallback mode).

Bit 5 : Signal quality

This bit will go high (1) when the quality of the received signal is too low for a good transmission.

Bit 6 : Carrier detect

This bit indicates the presence or the absence of the on-line signal as follows :

- This bit will go low (0) if the signal level is higher than – 43 dBm on PSTN or – 33 dBm on

leased lines
- This bit will go high (1) if the signal level is lower than – 48 dBm on PSTN or – 38 dBm on leased lines

The minimum hysteresis level is 2 dB.

The information on the on-line signal may be used by the control processor to manage the 109 signal of the V.24 junction.

Bit 7 : Reserved

THIRD BYTE :

Bit 0 : Reserved

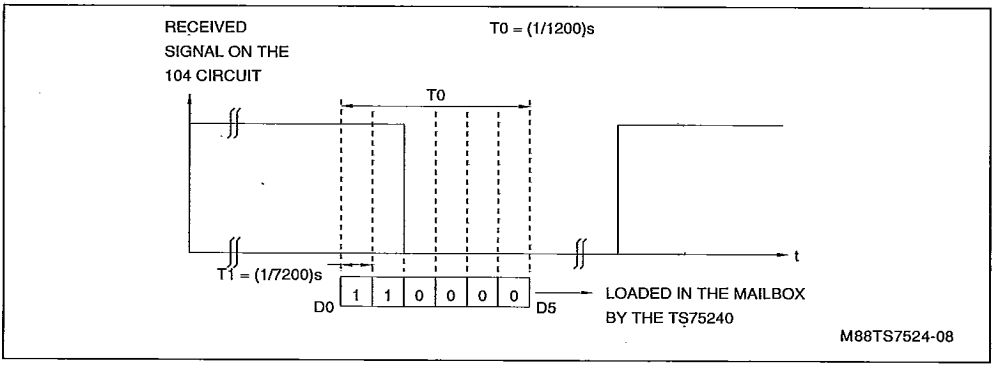
Bit 6 Thru 1 : Data received or data after descrambling.

These six bits contain the received data and have to be processed by the control processor according to the selected standards :
- In QAM and DPSK modes, bit 4 thru 1 represent the data received after descrambling, if the descrambler is enabled. Otherwise, they represent the data received without descrambling.

The data is encoded on four bits (D3, D2, D1, D0) in V.22Bis, on two bits (D1, D0), in V.22 at 1200 bps and Bell 212, on only one bit (D0) in V.22 at 600 bps. The unused bits are set to one by the TS7524.

The mailbox exchange rate between the TS75240 and the control processor is done at 600 exchanges per second. For both QAM and DPSK modes, D0 (which correspond to bit 1) is the first bit received.
- In FSK modes (V.21, V.23, and BELL 103) all the six bits are used to represent the digital value of six samples of the received signal. In these modes, the mailbox exchange must be executed at the rate of 1200 exchanges per second. Consequently to perform a parallel to serial conversion the control processor has to resend these bits on the 104 circuit of the V.24/RS232 junction at 7.2 kHz.
Bit 1 (which correspond to D0) is the first sample of the incoming signal received over the line as shown in figure 8.

Figure 8 : FSK Receive Mode.



Bit 7 : Answer tone detection

Used in answer tone detection mode, this bit when low (0), indicates the presence of the answer tone (CCITT 2100 Hz, BELL 2225 Hz or Transpac 1650 Hz) sent by the far-end modem. When high (1), it means no detection of answer tone. Refer to paragraph "call progress and answer tone detection" for further details.

CALL PROGRESS AND ANSWER TONE DETECTION

The TS7524 call progress detection part is activated by detection of energy in the 300 to 700 Hz call progress tone bandwidth. The call progress mode must be selected in the first byte (bit 3 thru 0) of the receive command word.

Then the bit 7 of the first byte of the receive status word indicates to the control processor that the call progress tone is detected (bit 7 = 0) or not (Bit 7 = 1).

In answer tone mode, the TS7524 may recognize three different standard frequencies which represent the usual answer tones sent by the far-end modem as described hereunder :

- 2100 Hz : CCITT modes answer tone V.21 and V.23
- 2225 Hz : BELL answer tones
- 1650 Hz : Transpac V.21 answer tone

The answer tone mode must be selected in the first byte (bit 3 thru 0) of the receive command word and the answer tone selection (1650 Hz or 2100/2225 Hz) with the bit 4.

Then bit 7 in the third byte of the receive status word indicates to the control processor that the answer tone is detected (bit 7 = 0) or not (bit 7 = 1).

The table 10 shows the programmation of the receive command word, and the status reporting contained in the receive status word.

DTMF mode and transmit enable = 1 must be selected in the transmit command word.

Table 10 : Call Progress and Answer Tone Detection Programming Model.

	Receive Command Word		Receive Status Word	
	First Byte Bit 3, 2, 1, 0,	Bit 4	First Byte Bit 7	Third Byte Bit 7
Call Progress Mode and 2100/2225 Answer Tone	0111	0	1 No Call Progress Tone Detected 0 Presence of Call Progress Tone	0 2100/2225 Hz Detected 1 No Detection
Call Progress Mode and 1650 Hz Answer Tone	0111	1	1 No Call Progress Tone Detected 0 Presence of Call Progress Tone	0 1650 HZ Detected 1 No Detection

4. ELECTRICAL SPECIFICATIONS

4.1. MAXIMUM RATINGS

TS75240

Symbol	Parameter	Value	Unit
V_{CC} *	Supply Voltage	– 0.3 to 7.0	V
V_{in} *	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

Symbol	Parameter	Value	Unit
	Supply Voltage between V^+ and AGND or DGND	− 0.3 to + 7	V
	Supply Voltage between V^+ and AGND or DGND	− 7 to + 0.3	V
	Voltage between AGND and DGND	− 0.3 to + 0.3	V
	Digital Input Voltage	DGND − 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Voltage	DGND − 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Current	− 20 to + 20	mA
	Analog Input Voltage	V_{CC}^- − 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Voltage	V_{CC}^- − 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Current	− 10 to + 10	mA
	Power Dissipation	500	mW
T_{oper}	Operating Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature	− 65 to + 150	°C

4.2. DC ELECTRICAL CHARACTERISTICS DGND = AGND = 0 V

Digital Supply

V_{CC} = 5.0V ± 5% , V_{SS} = 0, T_A = 0 to + 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	− 0.3		0.8	V
V_{IH}	Input High Voltage. All inputs except $\overline{RESET}$	24		V_{CC}	V
V_{IH}	$\overline{RESET}$ Input High Voltage	2.8		V_{CC}	V
I_I	Input Extal Current	− 50		+ 50	µA
I_{in}	Input Leakage Current BS0, BS1, BS2, BE3, BE4, $\overline{RS}$, $\overline{SDS}$, $\overline{CS}$, $\overline{SRW}$, $\overline{RESET}$	− 10		+ 10	µA
V_{OH}	Output High Voltage (I_{load} = − 300µA). All Outputs Except $\overline{DTACK}$	2.7			V
V_{OL}	Output Low voltage (I_{load} = 3.2mA). All Outputs			0.5	V
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current @ 2.4V/0.4V $\overline{DTACK}$, BA, D0-D15, AD0-AD7	− 20		+ 20	µA
T_A	Operating Free-air Temperature (notes 1 and 2)	0		70	°C
I_{CC}	Supply Current TS75240 T_A = 25°C			480	mA
I_{CC}	T_C = 100°C			420	mA

Notes : 1. Case temperature Tc must be maintained below 100°C.
2. $R_{\theta JA}$ 39°C/watts Side-brazed ceramic DIL-48.
28°C/watts PDIL-48 heath spreader.

Analog Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	− 5.25		− 4.75	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current	− 35			mA

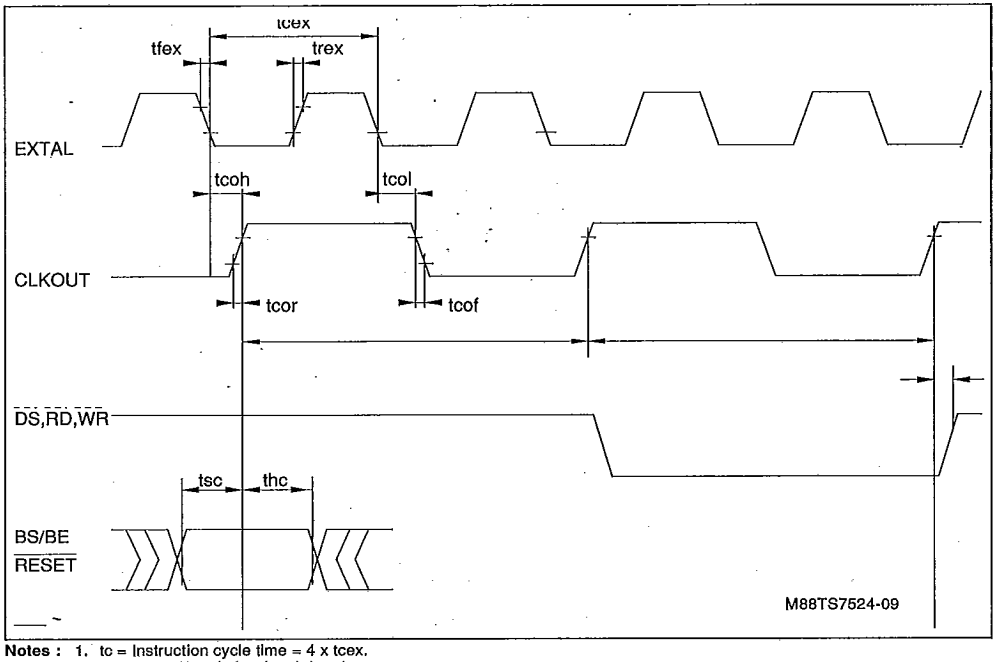
4.3. AC ELECTRICAL SPECIFICATIONS

4.3.1. CLOCK AND CONTROL PINS TIMING (V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C, see figure 9)
OUTPUT LOAD = 50 pF + DC characteristics I load

Reference Levels : V_{IL} : 0 V V_{IH} : 2.4 V
V_{OL} : 1.5 V V_{OH} : 1.5 V tr, tf ≤ 5 ns for Input Signals

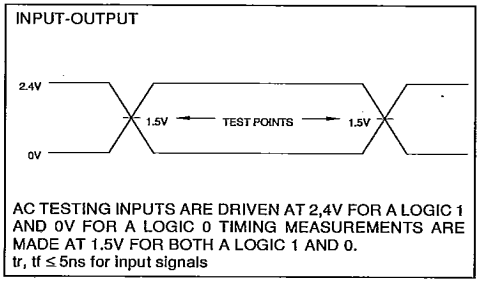
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time	43.4			ns
t_{fex}	External Clock Fall Time			5	ns
t_{rex}	External Clock Rise Time			5	ns
t_{coh}	EXTAL to CLKOUT High Delay		25		ns
t_{col}	EXTAL to CLKOUT Low Delay		25		ns
t_{cor}	CLKOUT Rise Time			10	ns
t_{cof}	CLKOUT Fall Time			10	ns
t_{dlc}	CLKOUT to Control Output Low ($\overline{IRQ}$, BA)			50	ns
t_{dhc}	CLKOUT to Control Output High ($\overline{IRQ}$, BA)			50	ns
t_{dsl}	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low		5		ns
t_{dsh}	CLKOUT to $\overline{DS}$, $\overline{RP}$, $\overline{WR}$ High		5		ns
t_{sc}	Control Inputs Set-up Time (BS0 ... BE6, $\overline{RESET}$)	20			ns
t_{hc}	Control Inputs Hold Time (BS0 ... BE6, $\overline{RESET}$)	10			ns

Figure 9 : Clock and Control Pins Timing.



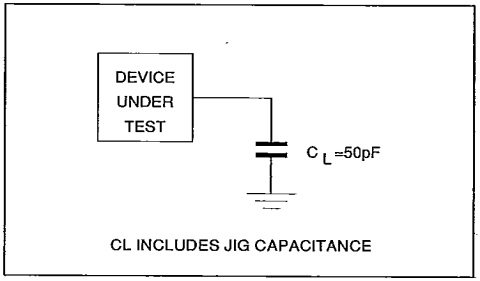
Notes : 1. tc = Instruction cycle time = 4 x tcex.
2. BE3.....BE6 min low level duration = tc.

A.C. TESTING INPUT, OUTPUT WAVEFORM



AC TESTING INPUTS ARE DRIVEN AT 2,4V FOR A LOGIC 1 AND 0V FOR A LOGIC 0 TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC 1 AND 0.
tr, tf ≤ 5ns for input signals

A.C. TESTING LOAD CIRCUIT

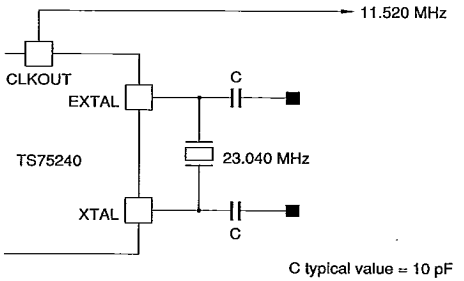


CL INCLUDES JIG CAPACITANCE

INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT is half the crystal fundamental frequency, and can be used by the control processor.

Then the 5.76 MHz required by the Analog Front End can be easily obtained.



C typical value = 10 pF

M88TS7524-10

Crystal nominal parameters :

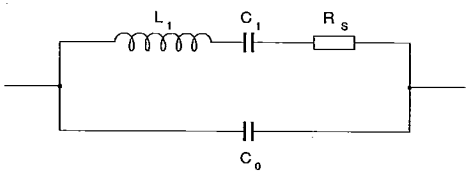
Parallel resonance fundamental mode - AT CUT

R_S = 10 Ω

C_1 = 0.018 pF

C_0 = 3.5 pF

Q > 30 K



M88TS7524-11

4.3.2. TS68952 : CLOCK GENERATOR

Crystal Oscillator Interface

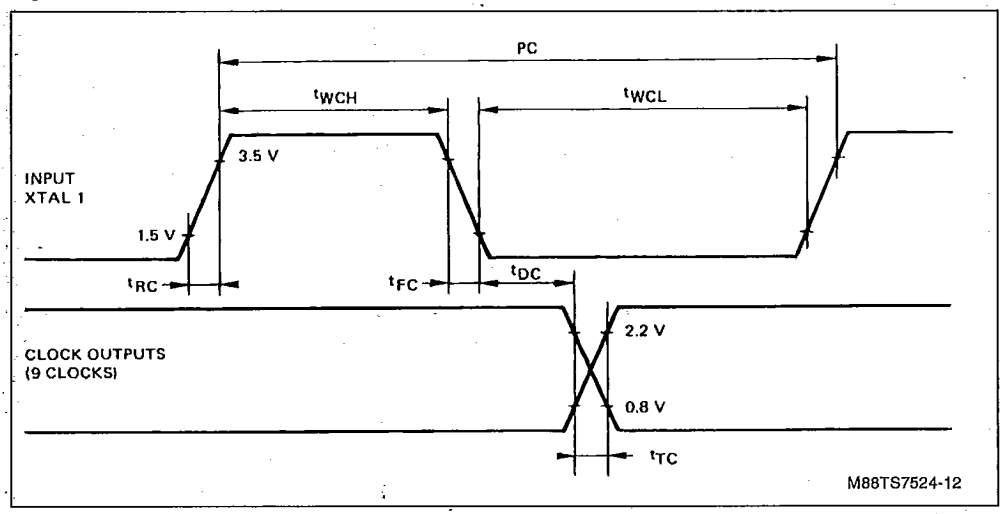
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Voltage		3.5			V
I_{IL}	Input Low Level Current	$DGND \leq V_I \leq V_{IL\,max}$	– 15			µA
I_{IH}	Input High Level Current	$V_{IH\,min} \leq V_I \leq V^+$			15	µA

CLOCK WAVE FORMS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PC	Main Clock Period	XTAL1 Input		173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL = 50 pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL = 50 pF			100	ns

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = 5.0$ V and $T_{amb} = 25$ °C.

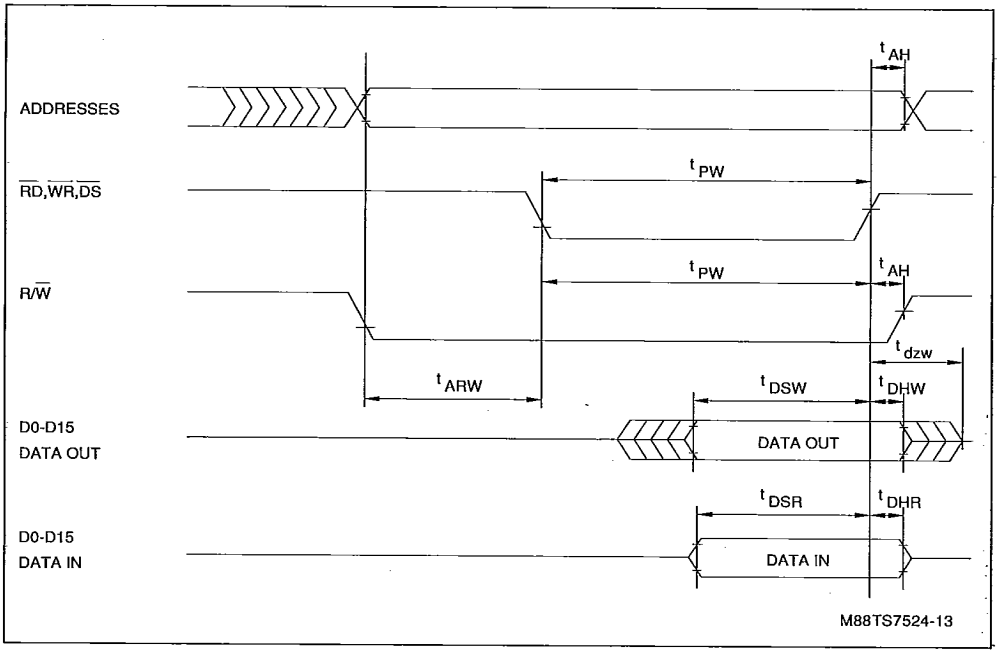
Figure 10 : Clock Generator.



4.3.3. LOCAL BUS TIMING (TS75240 and TS68950/51/52)
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70 °C, see figure 11)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width	1/2 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{DS}$, $\overline{RD}$ Low	1/2 tc – 40		ns
t_{DZW}	$\overline{DS}$ High to Data High Impedance, Write Cycle		40	ns

Figure 11 : Local Bus Timing Diagram.

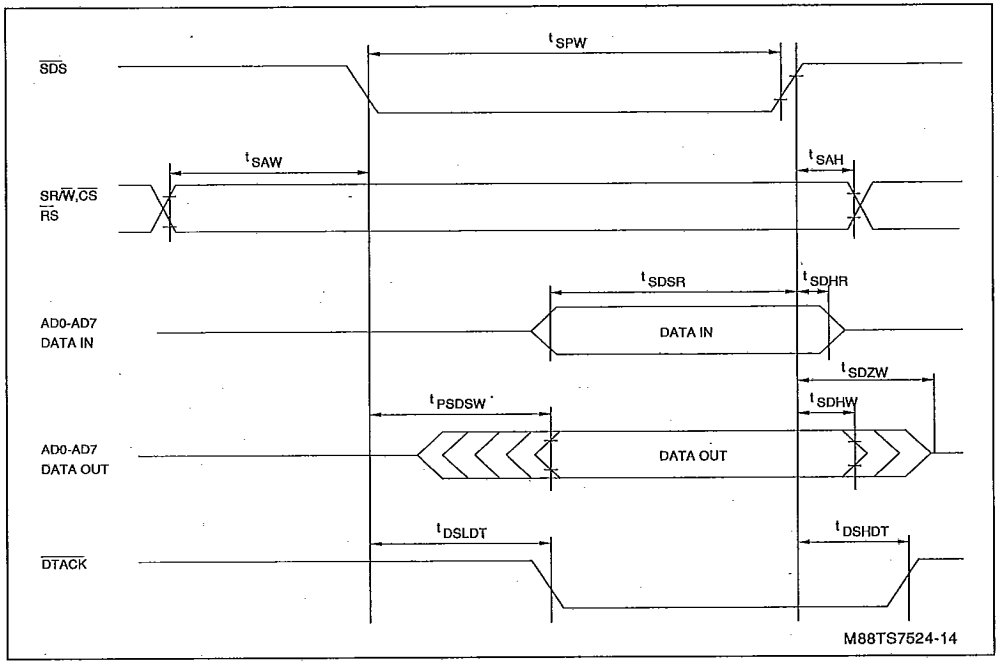


4.3.4. SYSTEM BUS TIMING (TS75240 and control processor)
V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70 °C

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60		ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{PSDSW}	Data Propagation Delay, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10		ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle		40	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low		50	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High*		50	ns

* DTACK is an open drain output test load include R_L = 820 Ω at V_{CC}.

Figure 12 : System Bus Timing Diagram.



4.3.5. DAA INTERFACE (DAA and TS68950 and TS68951)

Analog Transmit Output (ATO)
$V^+ = 5\ V \pm 5\ \%$, $0\ °C \leq T_{amb} \leq +70\ °C$ $V^- = -5\ V \pm 5\ \%$, $0\ °C \leq T_{amb} \leq +70\ °C$
(unless otherwise specified)

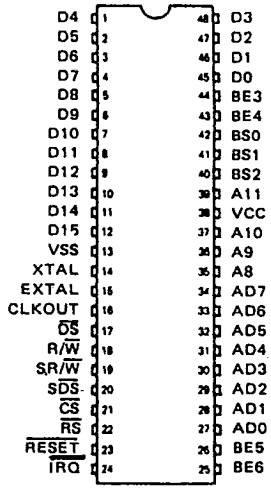
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OS}	Output DC Offset	− 250		+ 250	mV
C_L	Load Capacitance			50	pF
R_L	Load Resistance	1.2			kΩ
V_{out}	Output Voltage Swing ($R_L > 1.2\ k\Omega$ $C_L < 50\ pF$)	− 2.5		+ 2.5	V
R_{out}	Output Resistance (read cycle)			5	Ω

Receive Analog Input (RAI).

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{in}	Input Voltage	− 2.5		+ 2.5	V
I_{in}	Input Current (write cycle)	− 1		+ 1	µA

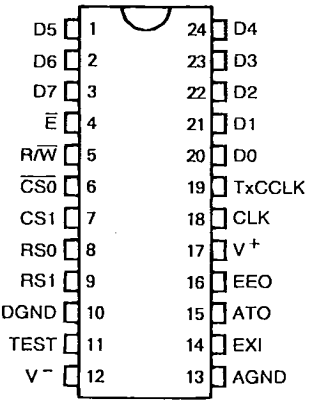
5. PIN CONNECTIONS

TS75240



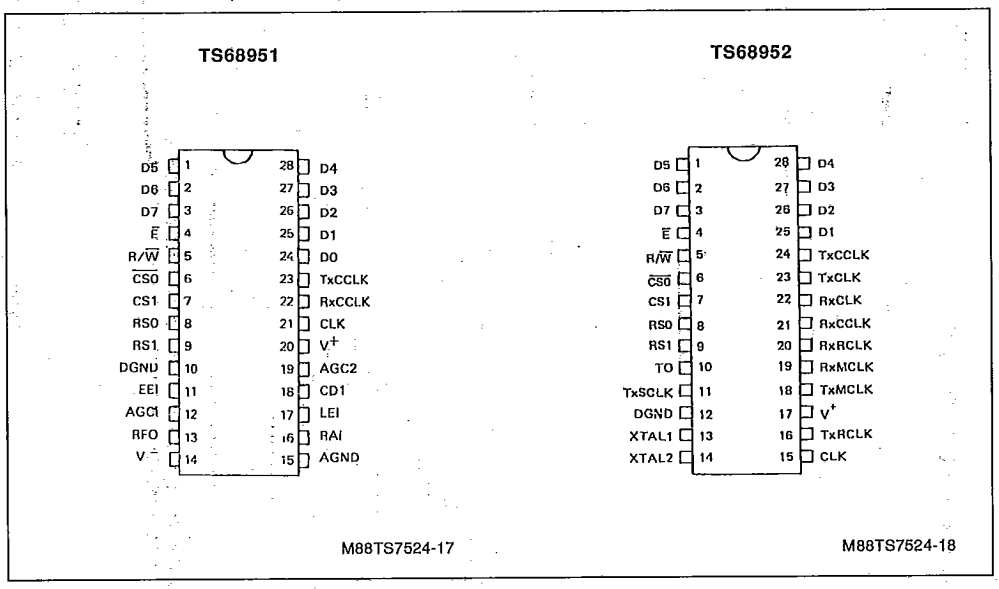
M88TS7524-15

TS68950



M88TS7524-16

PIN CONNECTIONS (continued)



TS75240

MAFE Interface

Name	Pin	Function	Description
D0 thru D15	I/O	Local Data Bus	Only D8 thru D15 lines are used for data transfer between the TS75240 and MAFE Kit. D0 thru D7 are not used and are left unconnected.
A8 thru A11	O	Local Address Bus	Address Lines to the MAFE Kit.
$\overline{DS}$	O	Data Strobe	This signal synchronizes the transfer between the TS75240 and the MAFE Kit.
R/$\overline{W}$	O	Read/Write	Indicates the current bus cycle state.
CLKOUT	O	Clock Output	This signal generated by the TS75240 is at half the frequency of the crystal. It can be divided by 2 to provide the 5.76 MHz clock for the MAFE Kit.
BE3 thru BE6	I	Receive and Transmit Clocks	These four inputs are connected to the receive and transmit clocks generated by the clock generator circuit (TS68952) of the MAFE Kit.

System Interface.

Name	Pin	Function	Description
AD0 thru AD7	I/O	System Data Bus	These bi-directional lines are used for data transfer between the TS75240 mailbox and a system processor.
$\overline{CS}$	I	Chip Select	This active low input is asserted when the TS75240 is to be accessed by the system processor.
$\overline{RS}$	I	Register Select	This signal is used with $\overline{CS}$ to control the data transfer between the system processor and the TS75240 mailbox.
$\overline{SDS}$	I	System Data Strobe	Synchronizes the transfer on the system bus.
SR/$\overline{W}$	I	System Read/Write	Indicates the current system bus cycle state.
$\overline{IRQ}$	O	Interrupt Request	Handshake signal sent to the master to gain access to the mailbox.

Others Pins.

Name	Pin	Function	Description
BS0 thru BS2	I	Branch on State	These three inputs are not used and must be grounded.
EXTAL	I	Clock	Crystal Input for Internal Oscillator or Input Pin for External Oscillator.
XTAL	I	Clock	Together with EXTAL this pin is used for the external 23.040 MHz crystal.
V_{CC}	Supply	Power Supply	
V_{SS}	Supply	Ground	
$\overline{RESET}$	I	Reset	

TS68950

Name	N°	Description
D5-D7	1-3	8 bit data bus inputs giving access to Tx estimated echo, control and address registers. (same for pins 20-24).
$\overline{E}$	4	Enable Input. Data are strobed on the positive transitions of this input.
R/$\overline{W}$	5	Read/Write Selection. Internal registers can be written when R/$\overline{W}$ = 0. Read mode is not used.
$\overline{CS0}$-CS1	6-7	Chip Select Inputs. The chip set is selected when $\overline{CSO}$ = 0 and CS1 = 1.
RS0-RS1	8-9	Register Select Inputs. Used to select D/A input registers or control/address registers in the write mode.
DGND	10	Digital Ground = 0 V. All digital signals are referenced to this pin.
TEST	11	Test Input. Used for test purposes. This pin must be grounded in all applications
V^-	12	Negative Supply Voltage = − 5 V ± 5 %
AGND	13	Analog Ground = 0 V.
EXI	14	Programmable analog input tied to filter or attenuator input according to the RC4 register content.
ATO	15	Analog Transmit Output.
EEO	16	Analog Echo Cancelling Output.
V^+	17	Positive Power Supply Voltage = + 5 V ±5 %
CLK	18	Master Clock Input. Nominal Frequency 1.44 MHz
TxCCLK	19	Transmit Conversion Clock Input.
D0-D4	20-24	See description of D5-D7 (pins1-3) given above.

Name	N°	Description
D5-D7	1-3	Data Bus.
$\overline{E}$	4	Enable Input. Enables Selection Inputs. Active on a low level for read operation. Active on a positive level for write operation.
R/$\overline{W}$	5	Read/Write Selection Input. Read operation is selected on a high level. Write operation is selected on a low level.
$\overline{CS0}$-CS1	6-7	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1.
$\overline{RS0}$-$\overline{RS1}$	8-9	Register Select Inputs. Select the register involved in a read or write operation.
DGND	10	Digital Ground. All digital signals are referenced to this pin.
EEI	11	Estimated Echo Input. When operating in echo cancelling mode, this signal is added to the reception band-pass filter output.
AGC1	12	Analog Input of the Automatic Gain Control Amplifier and of the Carrier Level Dectector.
RFO	13	Reception Filter Analog Output. Designed to be connected to AGC1 input through a 1 µF non polarized capacitor.
V^-	14	Negative Supply Voltage = – 5 V ± 5 %
AGND	15	Analog Ground. All analog signals are referenced to this pin.
RAI	16	Receive Analog Input. Analog input tied to the transmission line.
LEI	17	Local Echo Input. Analog input subtracted from the receive anti-aliasing filter output.
CD1	18	This pin must be connected to the analog ground trough a 1 µF non polarized capacitor, in order to cancel the offset voltage of the carrier level detector amplifier.
AGC2	19	This pin must be connected to the analog ground trough a 1 µF non polarized capacitor, in order to cancel the offset voltage of the offset AGC amplifier.
V^+	20	Positive Supply Voltage = + 5 V ± 5 %
CLK	21	Master Clock Input. Nominal Frequency 1.44 MHz.
RxCCLK	22	Receive Conversion Clock.
TxCCLK	23	Transmit Conversion Clock.
D0-D4	24-28	Data Bus.

TS68952

Name	N°	Description
D5-D7	1-3	Data Bus Inputs to Internal Registers
$\overline{E}$	4	Enable Input. Data are strobed on the positive transitions of this input.
R/$\overline{W}$	5	Read/Write Selection Input. Internal registers can be written when R/$\overline{W}$ = 0. Read mode is only used for Rx front-end-chip.
$\overline{CS0}$-CS1	6-7	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1.
RS0-RS1	8-9	Register Select Inputs. Used to select address or control registers
TO	10	Test Output. Must be left open in all applications.
TxSCLK	11	Transmit Synchronizing Clock Input. Normally tied to an external clock terminal. When this pin is tied to a permanent logical level, transmit DPLL free-runs or can be synchronized to the receive clock system.
DGND	12	Digital Ground = 0 V. All digital signals are referenced to this pin.
XTAL1	13	Crystal Oscillator or Pulse Generator Input.
XTAL2	14	Crystal Oscillator Output.
CLK	15	1.44 MHz Clock Output. Useful for TS68950/51.
TxRCLK	16	Transmit Baud Rate Clock Output
V^+	17	Positive Supply Voltage = + 5 V ± 5 %
TxMCLK	18	Transmit Multiplexing Clock Output
RxMCLK	19	Receive Multiplexing Clock Output
RxRCLK	20	Receive Baud Rate Clock Output
RxCCLK	21	Receive Conversion Clock Output
RxCLK	22	Receive Bit Rate Clock Output
TxCLK	23	Transmit Bit Rate Clock Output
TxCCLK	24	Transmit Conversion Clock Output
D1-D4	25-28	Data Bus Inputs to Internal Registers (D0 is not used)

6. ORDERING INFORMATION

The TS7524 corresponds to four different components which must be ordered separately.

Furthermore, a stand-alone evaluation board is available for a fast characterization improvement of the TS7524 in a real application.

Part Number	Temp Range	Package	Device
TS75240CP/XX	0 °C to 70 °C	DIP-48	V. 22Bis Masked DSP
TS68950CP	0 °C to 70 °C	DIP-24	Transmit Analog Interface
TS68951CP	0 °C to 70 °C	DIP-28	Receive Analog Interface
TS68952CP	0 °C to 70 °C	DIP-28	Clock Generator Interface
TS7524EVA *	N. A		Stand Alone Evaluation Board

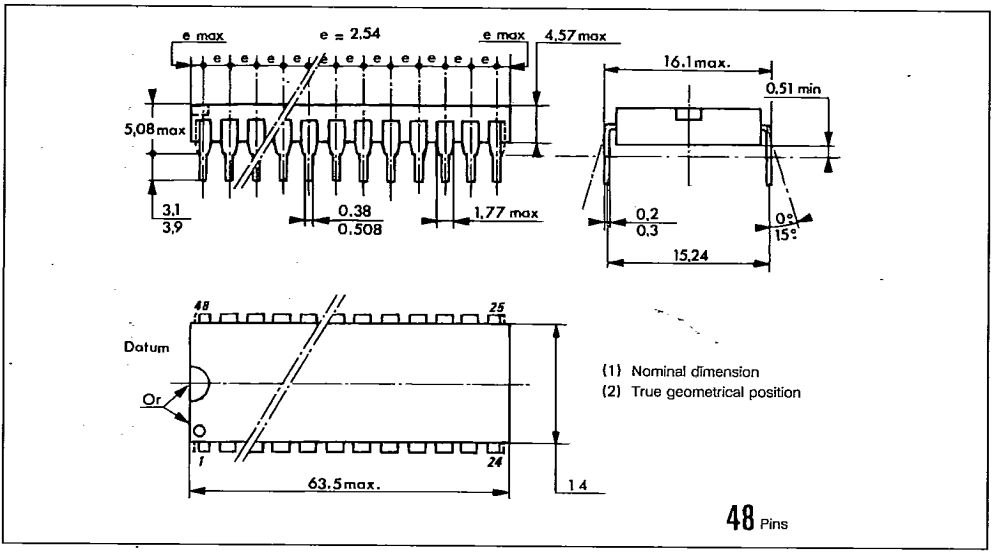
* Contact your SGS-THOMSON representative.

7. PACKAGE MECHANICAL DATA

TS75240

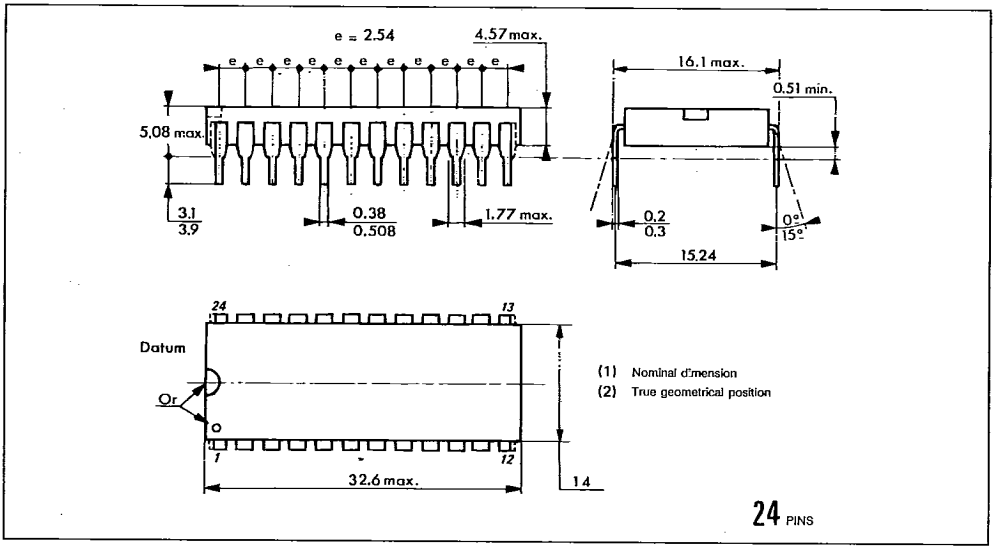
T-75-33-05

48 Pins – Plastic Dip.



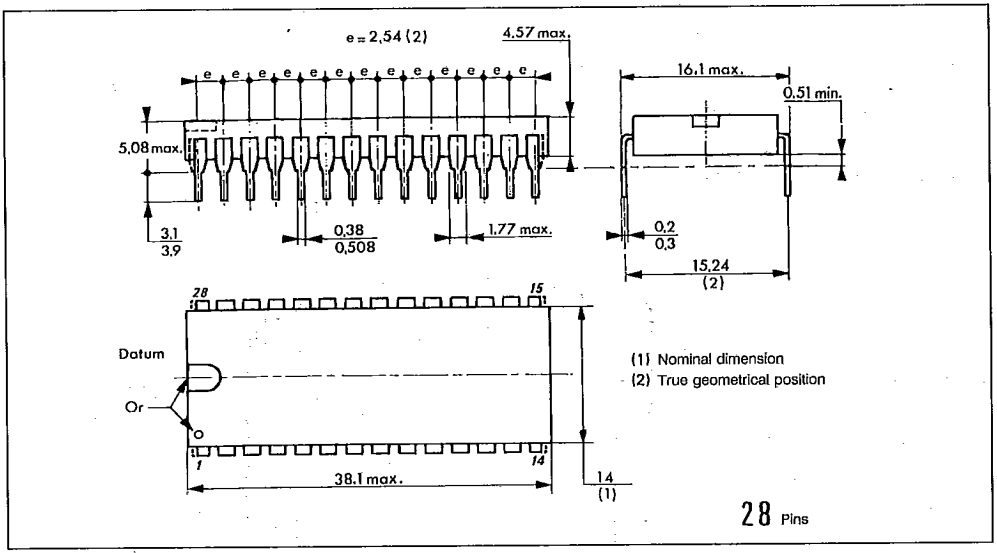
TS68950

24 Pins – Plastic Dip.



TS68951/TS68952

28 Pins – Plastic Dip.



ELECTRICAL CONSIDERATIONS

To avoid possible high frequency problems, the following precautions should be considered for PC board layout design :

- A ground plane on the component side connected to analog ground of the TS68950/51
- Analog and Digital ground tracks corresponding to different signals, e.g. clocks, input signals, references, ... should be adequately separated and terminated at a single point.
- Optimal distribution of power supplies and ground links using star-connection.
- Adequate decoupling capacitor mounted as close as possible to each device, and connected to analog ground.
- DSP and MAFE power supplies should be separated.

APPENDIX A

TRANSMIT/RECEIVE COMMAND WORDS

Transmit Command Word.

BIT	First Byte	Second Byte	Third Byte				
0	Transmit Mode Selection	Transmit Attenuation	Transmit (0)				
1	0000 : Modem Disabled 0001 : V.22 Bis		D0	DPSK	QAM		DTMF
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21		D1				
3	0110 : Bell 103 0111 : D.T.M.F.		D2	0			
4	Transmit Signalling 00 : Signalling Disabled		D3	0			
5	01 : 550 Hz 11 : 1800 Hz	Scrambler (ON/$\overline{OFF}$)	D4	0	0		0
6	**Reserved**	**Reserved**	D5	0	0		0
7	$\overline{ANSW}$/ORIG or DTMF	V.22 Binary Rate Select or DTMF	$\overline{Transmit\ Enable}$				

Note : All the "RESERVED" bits must be cleared to "0" by the user.

Receive Command Word.

BIT	First Byte	Second Byte	Third Byte
0	Receive. Mode Selection	**Reserved**	Receive (1)
1	0000 : Modem Disabled 0001 : V.22 Bis		**Reserved**
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21		
3	0110 : Bell 103 0111 : Call Prog / Answer Tone		
4	Answer Tone Selection		
5	Tx Synchronization	Descrambler (ON/$\overline{OFF}$)	
6	Carrier Detect Level	**Reserved**	
7	$\overline{Answer}$/originate	V.22 Binary Rate Select	

Note : All the "RESERVED" bits must be cleared to "0" by the user.

APPENDIX B

TRANSMIT/RECEIVE STATUS WORDS

Transmit Status Word.

BIT	First Byte	Second Byte	Third Byte
0	Transmit (0)	Reserved	Reserved
1	Reserved		
2			
3			
4			
5			
6			
7			

Receive Status Word.

BIT	First Byte	Second Byte	Third Byte
0	Receive (1)	Reserved	Reserved
1	D0 Data Before		D0 Data After Descr. (Q.A.M., D.P.S.K.) D0 Data (F. S. K.)
2	D1 Descrambling		D1
3	D2 (Q.A.M. , D.P.S.K.)		D2
4	D3	Equalization Status	D3
5	Reserved	$\overline{\text{Signal Quality}}$	1 D4
6	S1 Sequence	$\overline{\text{Carrier Detection}}$	1 D5
7	$\overline{\text{S1 Sequence or Call Progress Tone Detection}}$	Reserved	$\overline{\text{Answer Tone Detection}}$

Note : In QAM and DPSK modes, both for the data after and before descrambling, the unused bits are set to "1" by the TS7524.