- **Fully Supports Provisions of IEEE 1394-1995 Standard for High-Performance Serial Bus† and the IEEE 1394a-2000 Supplement**
- **Fully Interoperable With FireWire™ and i.LINK™ Implementation of IEEE Std 1394**
- **Meets Intel™ Mobile Power Guideline 2000**
- **Full IEEE 1394a-2000 Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-By Concatenation, Port Disable/Suspend/ Resume**
- **Power-Down Features to Conserve Energy In Battery-Powered Applications Include: Automatic Device Power Down During Suspend, PCI Power Management for Link-Layer, and Inactive Ports Powered Down**
- **Ultralow-Power Sleep Mode**
- **Provides Two IEEE 1394a-2000 Fully Compliant Cable Ports at 100/200/400 Megabits Per Second (Mbits/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Cable Power Presence Monitoring**
- **Separate Cable Bias (TPBIAS) for Each Port**
- **3.3-V Core Logic With Universal PCI Interfaces Compatible With 3.3-V and 5-V PCI Signaling Environments**
- **Physical Write Posting of up to Three Outstanding Transactions**
- **Implements PCI Burst Transfers and Deep FIFOs to Tolerate Large Host Latency**
- **Supports $\overline{\text{PCI-CLKRUN}}$ Protocol**
- **External Cycle Timer Control for Customized Synchronization**
- **Extended Resume Signaling for Compatibility With Legacy DV Components**
- **PHY-Link Logic Performs System Initialization and Arbitration Functions**
- **PHY-Link Encode and Decode Functions Included for Data-Strobe Bit Level Encoding**
- **PHY-Link Incoming Data Resynchronized to Local Clock**
- **Low-Cost 24.576-MHz Crystal Provides Transmit and Receive Data at 100/200/400 Mbits/s**
- **Node Power Class Information Signaling for System Power Management**
- **Serial ROM Interface Supports Two-Wire Devices**
- **Provides Two General-Purpose I/Os**
- **Register Bits Give Software Control of Contender Bit, Power Class Bits, Link Active Control Bit and IEEE 1394a-2000 Features**
- **Fabricated in Advanced Low-Power CMOS Process**

PRODUCT PREVIEW

description

The Texas Instruments TSB43AA22 is an integrated PHY/link device that is fully compliant with *PCI Local Bus (Rev. 2.2)*, *PCI Bus Power Management Interface (Rev. 1.1)*, IEEE 1394-1995, IEEE 1394a-2000, and *1394 Open Host Controller Interface Specification (Rev. 1.0)*. It is capable of transferring data between the 33-MHz PCI bus and 1394 bus at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s. The TSB43AA22 provides two 1394 ports which have separate cable bias (TPBIAS). The TSB43AA22 also supports IEEE 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

The TSB43AA22 design provides PCI bus master bursting, and it is capable of transferring a cacheline of data at 132 Mbytes/s after connection to the memory controller. Since PCI latency can be large even on PCI Revision 2.2 systems, deep FIFOs are provided to buffer the 1394 data.

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description (continued)

The TSB43AA22 provides physical write posting buffers and a highly tuned physical data path for SBP-2 performance. The TSB43AA22 also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus holding buffers.

An advanced CMOS process is used to achieve low power consumption while operating at PCI clock rates up to 33 MHz.

The TSB43AA22 provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The TSB43AA22 requires only an external 24.576-MHz crystal as a reference for the cable ports. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded strobe and data information. A 49.152-MHz clock signal is supplied to the integrated link layer controller (LLC) for synchronization and is used for resynchronization of the received data.

PRODUCT PREVIEW

Data bits to be transmitted through the cable ports are received from the integrated LLC and are latched internally in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 393.216 Mbits/s (referred to as S100, S200, and S400 speeds, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are resynchronized to the local 49.152-MHz system clock and sent to the integrated LLC. The received data is also transmitted (repeated) on the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB43AA22 provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains two independent TPBIAS circuits. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1.0 μF.

The line drivers in the TSB43AA22 operate in a high-impedance current mode and are designed to work with external 112-Ω line-termination resistor networks in order to match the 110-Ω cable impedance. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair-A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair-B terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current setting resistor has a value of 6.34 kΩ ±1%.

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description (continued)

When the power supply of the TSB43AA22 is off while the twisted-pair cables are connected, the TSB43AA22 transmitter and receiver circuitry presents a high impedance to the cable and will not load the TPBIAS voltage at the other end of the cable.

When the device is in a low-power state, for example, D2 or D3, the TSB43AA22 automatically enters a low-power mode if all ports are inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB43AA22 disables its internal clock generators and also disables various voltage and current reference circuits depending on the state of the ports (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBIAS, for example). The lowest power consumption (the *ultralow-power sleep* mode) is attained when all ports are either disconnected or disabled with the port interrupt enable bit cleared. The TSB43AA22 exits the low-power mode when the LPS bit (bit 19) in the host controller control register (offset 50h/54h) is set or when a port event occurs which requires that the TSB43AA22 become active in order to respond to the event or to notify the LLC of the event (e.g., incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, a new connection is detected on a nondisabled port, etc.). The internal 49.152 MHz clock becomes active (and the integrated PHY becomes operative) within 2 ms after the LPS bit (bit 19) in the host controller control register (offset 50h/54h) is set when the TSB43AA22 is in the low-power mode.

ORDERING INFORMATION

ORDERING NUMBER	NAME	VOLTAGE	PACKAGE
TSB43AA22	iOHCI-Lynx	3.3 V	PDT

PRODUCT PREVIEW

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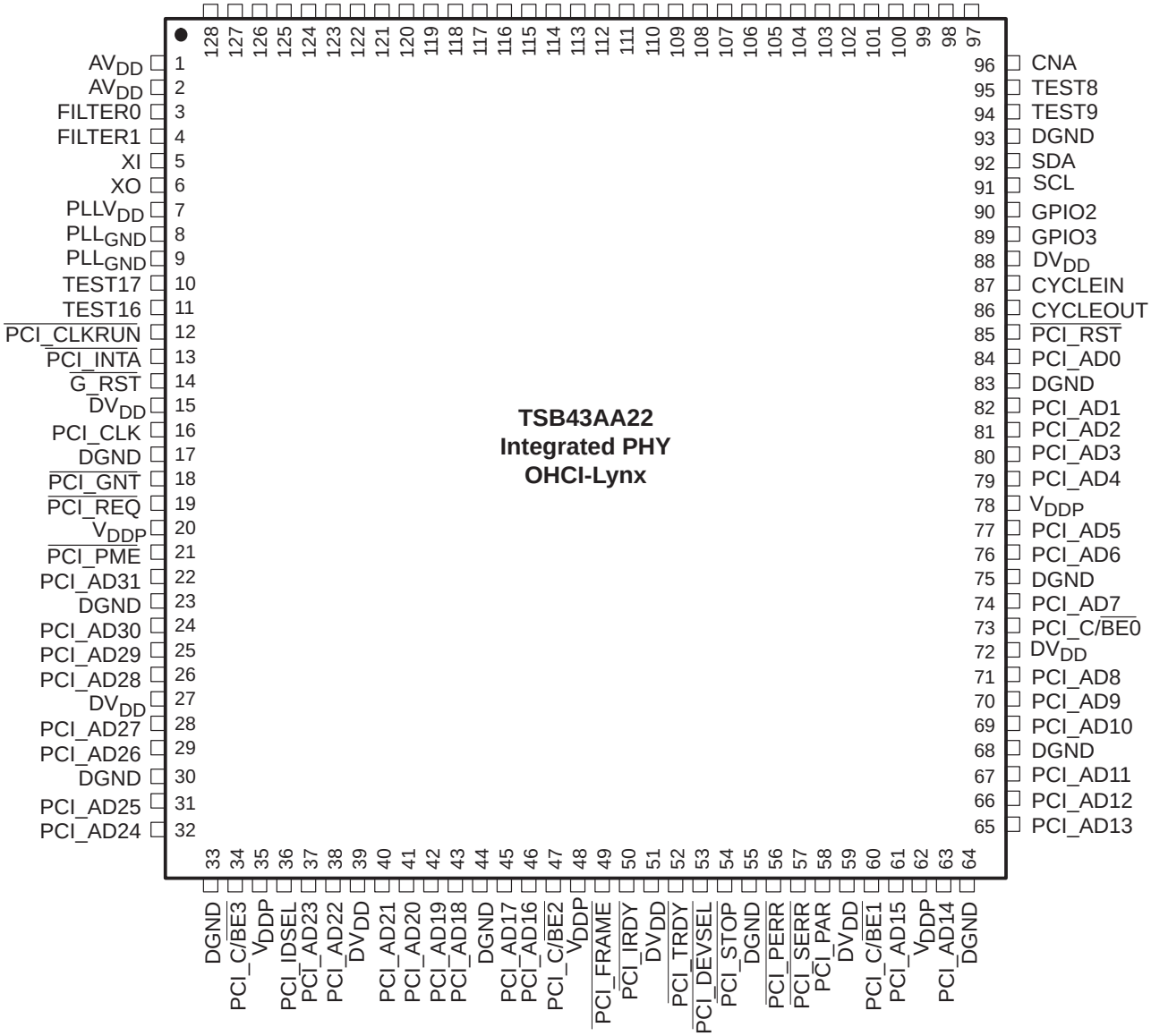
PRODUCT PREVIEW

PACKAGE
(TOP VIEW)



The TSB43AA22 is packaged in a 128-terminal PDT package. The following shows the mechanical dimensions for the PDT package.

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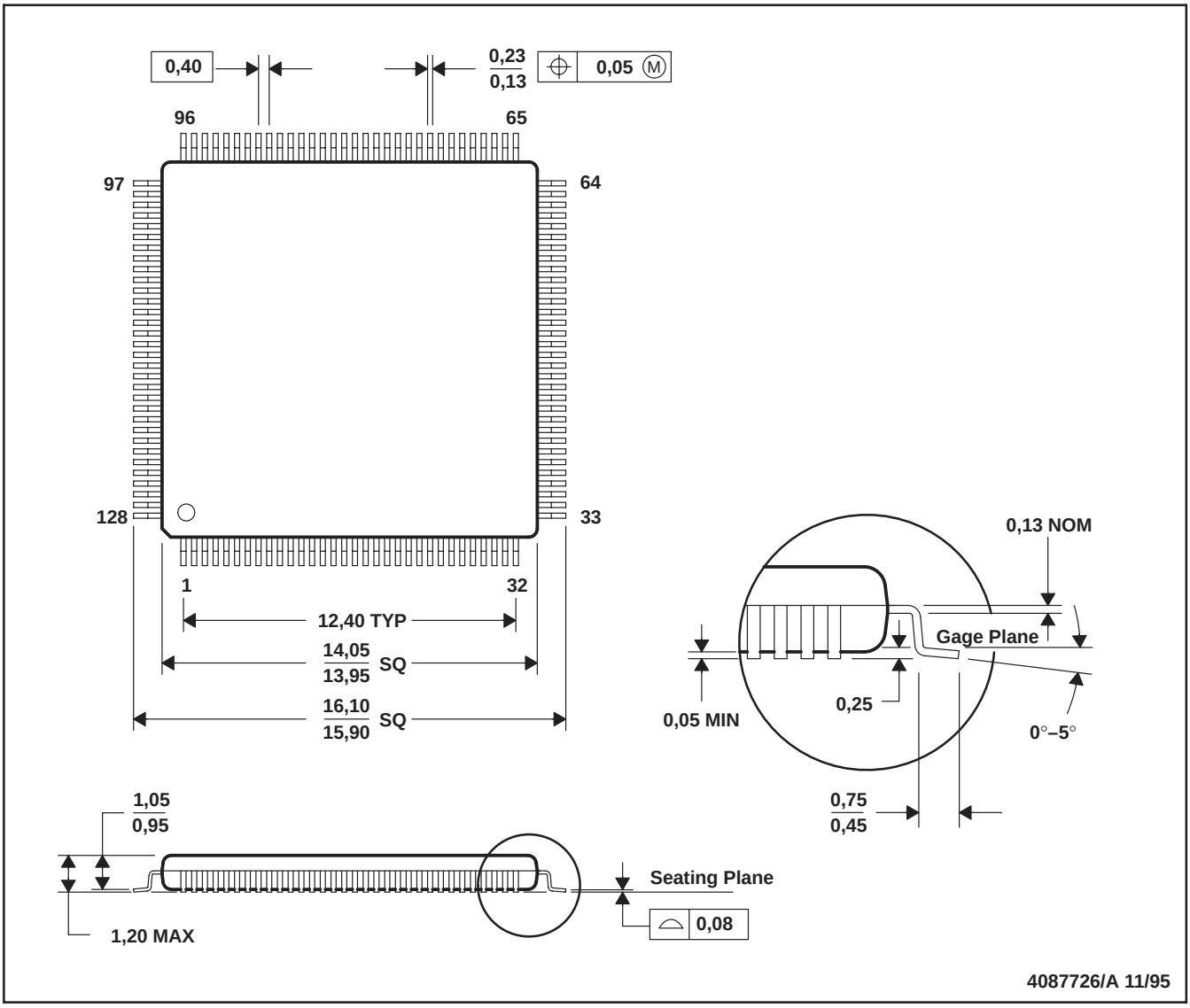
MECHANICAL DATA

PDT (S-PQFP-G128) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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