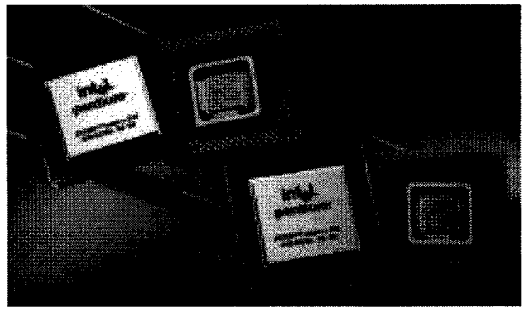
intel®

PENTIUM® PROCESSOR AT iCOMP® INDEX 815\100 MHz
PENTIUM PROCESSOR AT iCOMP INDEX 735\90 MHz
PENTIUM PROCESSOR AT iCOMP INDEX 610\75 MHz
WITH VOLTAGE REDUCTION TECHNOLOGY

- **Compatible with Large Software Base**
  - **MS-DOS‡, Windows‡, OS/2‡, UNIX‡**
- **32-Bit CPU with 64-Bit Data Bus**
- **Superscalar Architecture**
  - **Two Pipelined Integer Units Are Capable of 2 Instructions/Clock**
  - **Pipelined Floating Point Unit**
- **Separate Code and Data Caches**
  - **8K Code, 8K Writeback Data**
  - **MESI Cache Protocol**
- **Advanced Design Features**
  - **Branch Prediction**
  - **Virtual Mode Extensions**
- **Low Voltage BiCMOS Silicon Technology**
- **4M Pages for Increased TLB Hit Rate**
- **IEEE 1149.1 Boundary Scan**
- **Internal Error Detection Features**
- **SL Enhanced Power Management Features**
  - **System Management Mode**
  - **Clock Control**
- **Voltage Reduction Technology**
  - **2.9V V_{CC} for core supply**
  - **3.3V V_{CC} for I/O buffer supply**
- **Fractional Bus Operation**
  - **75-MHz Core / 50-MHz Bus**
  - **90-MHz Core / 60-MHz Bus**
  - **100-MHz Core / 66-MHz Bus**

The Pentium® processor is fully compatible with the entire installed base of applications for DOS‡, Windows‡, OS/2‡, and UNIX‡, and all other software that runs on any earlier Intel 8086 family product. The Pentium processor's superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor with voltage reduction technology has 3.3 million transistors. It is built on Intel's advanced low voltage BiCMOS silicon technology, and has full SL Enhanced power management features, including System Management Mode (SMM) and clock control. The additional SL Enhanced features, 2.9V core operation along with 3.3V I/O buffer operation, and the option of the TCP, which are not available in the desktop version of the Pentium processor, make the Pentium processor with voltage reduction technology ideal for enabling mobile Pentium processor designs. The Pentium processor may contain design defects or errors known as errata. Current characterized errata are available upon request.



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March 1996 Order Number 242973-001

CONTENTS

1.0. INTRODUCTION

Intel is manufacturing a reduced power version of the latest Pentium® processor, the Pentium processor with voltage reduction technology, targeting the mobile market. Voltage reduction technology allows the processor to "talk" to industry standard 3.3-volt components while its inner core, operating at 2.9 volts, consumes less power to promote a longer battery life. The Pentium processor with voltage reduction technology is offered in the Tape Carrier Package (TCP) and the Staggered Pin Grid Array (SPGA) package. It has all the advanced features of the 3.3V Pentium except for the differences listed in sections 3.1 and 7.1.1.

The Pentium processor with voltage reduction technology has several features which allow high-performance notebooks to be designed with the Pentium processor, including the following:

- TCP dimensions are ideal for small form-factor designs.
- TCP has superior thermal resistance characteristics.
- 2.9V core and 3.3V I/O buffer V_{CC} inputs reduce power consumption significantly, while maintaining 3.3V compatibility externally.
- The SL Enhanced feature set, which was initially implemented in the Intel486™ CPU.

The architecture and internal features of the Pentium processor with voltage reduction technology are identical to the desktop version of the Pentium processor specifications provided in the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors.*, except several features not used in mobile applications have been eliminated to streamline it for mobile applications.

This document should be used in conjunction with the following related Pentium processor documents.

- *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors* (Order Number: 241428)
- *Pentium® Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual* (Order Number: 241430)

2.0. MICROPROCESSOR ARCHITECTURE OVERVIEW

The Pentium processor with voltage reduction technology extends the Intel Pentium family of microprocessors. It is compatible with a host of other Intel products.

The Pentium processor family consists of the Pentium processor with voltage reduction technology described in this document, the original mobile Pentium processor and the various desktop Pentium processors. "Pentium processor" will be used in this document to refer to the entire Pentium processor family in general.

The mobile Pentium processor family architecture contains all of the features of the Intel486 CPU family, and provides significant enhancements and additions including the following:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 8K Code and 8K Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- Voltage Reduction Technology
- SL Power Management Features

2.1. Mobile Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 CPU family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 family and Intel486 family of CPUs.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the Branch Target Buffer (BTB) so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 CPU. Faster algorithms provide up to 10X speed-up for common operations including add, multiply and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache is 8 Kbytes in size, with a 32-byte line size and is 2-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be writeback or writethrough on a line-by-line basis and follows the MESI protocol. The data cache tags are triple-ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst writeback cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' MMU contains optional extensions to the architecture which allow 2-Mbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more and more functions are integrated on chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

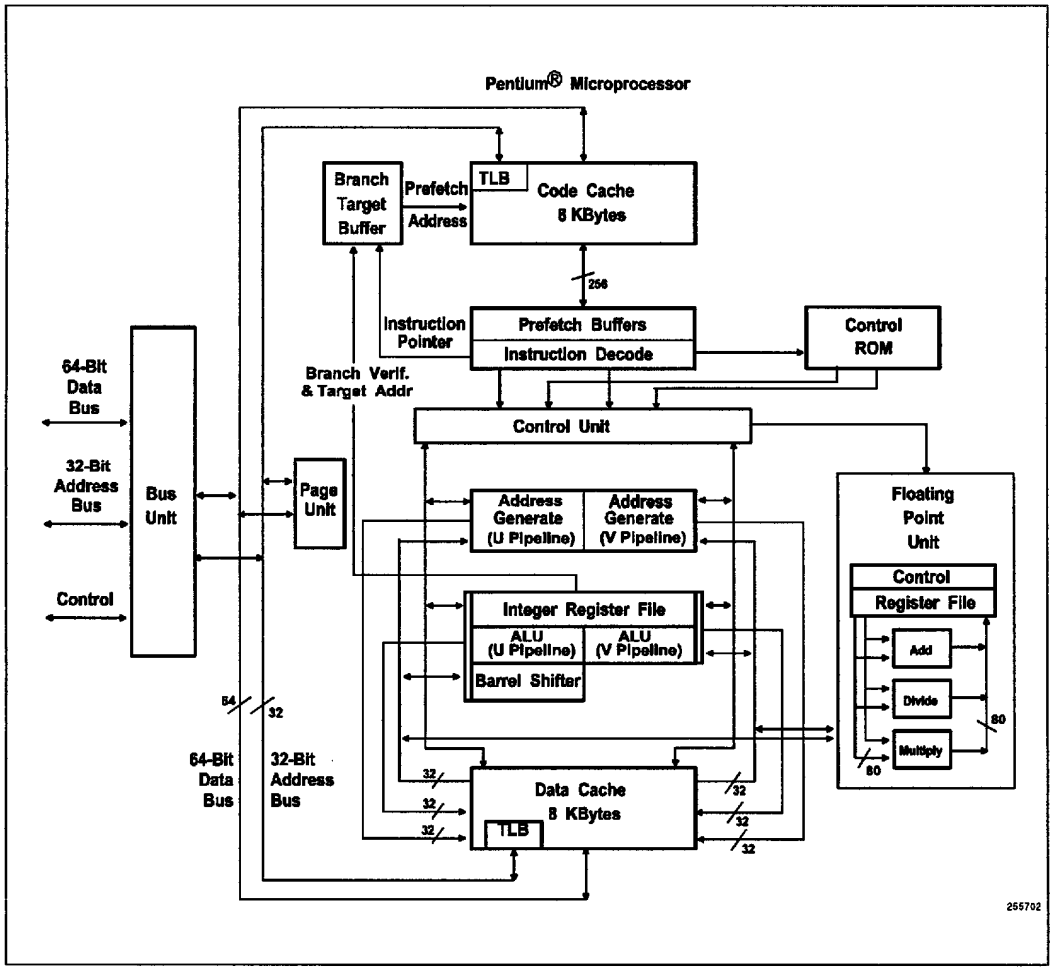


Figure 1. Pentium® Processor Block Diagram

Figure 1 shows a block diagram of the Pentium processor.

The block diagram shows the two instruction pipelines, the "u" pipe and "v" pipe. The u-pipe can execute all integer and floating point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate caches are shown, the code cache and data cache. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processor can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

The architectural features introduced in this section are more fully described in the *Pentium® Processor Family Developer's Manual, Volume 3.*

3.0. TCP PINOUT

3.1. Pentium® Processor with Voltage Reduction Technology Differences from the SPGA 3.3V Pentium Processor

To better streamline the part for mobile applications, the following features have been eliminated from the TCP and SPGA Pentium processor with voltage reduction technology: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 1 lists the corresponding pins which exist on the SPGA 3.3V Pentium processor but have been removed on the TCP and SPGA Pentium processor with voltage reduction technology.

Table 1. Signals Removed in Pentium® Processor with Voltage Reduction Technology

Signal	Function
ADSC#	Additional Address Status. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	Additional Burst Ready. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	CPU Type. This signal is used for dual processing systems.
D/P#	Dual/Primary processor identification. This signal is only used for an upgrade processor.
FRCMC#	Functional Redundancy Checking. This signal is only used for error detection via processor redundancy, and requires two Pentium® processors (master/checker).
PBGNT#	Private Bus Grant. This signal is only used for dual processing systems.
PBREQ#	Private Bus Request. This signal is used only for dual processing systems.
PHIT#	Private Hit. This signal is only used for dual processing systems.
PHITM#	Private Modified Hit. This signal is only used for dual processing systems.
PICCLK	APIC Clock. This signal is the APIC interrupt controller serial data bus clock.
PICD0 [DPEN#]	APIC's Programmable Interrupt Controller Data line 0. PICD0 shares a pin with DPEN# (Dual Processing Enable).
PICD1 [APICEN]	APIC's Programmable Interrupt Controller Data line 1. PICD1 shares a pin with APICEN (APIC Enable (on RESET)).

3.2. TCP Pinout and Pin Descriptions

3.2.1. TCP PENTIUM® PROCESSOR PINOUT

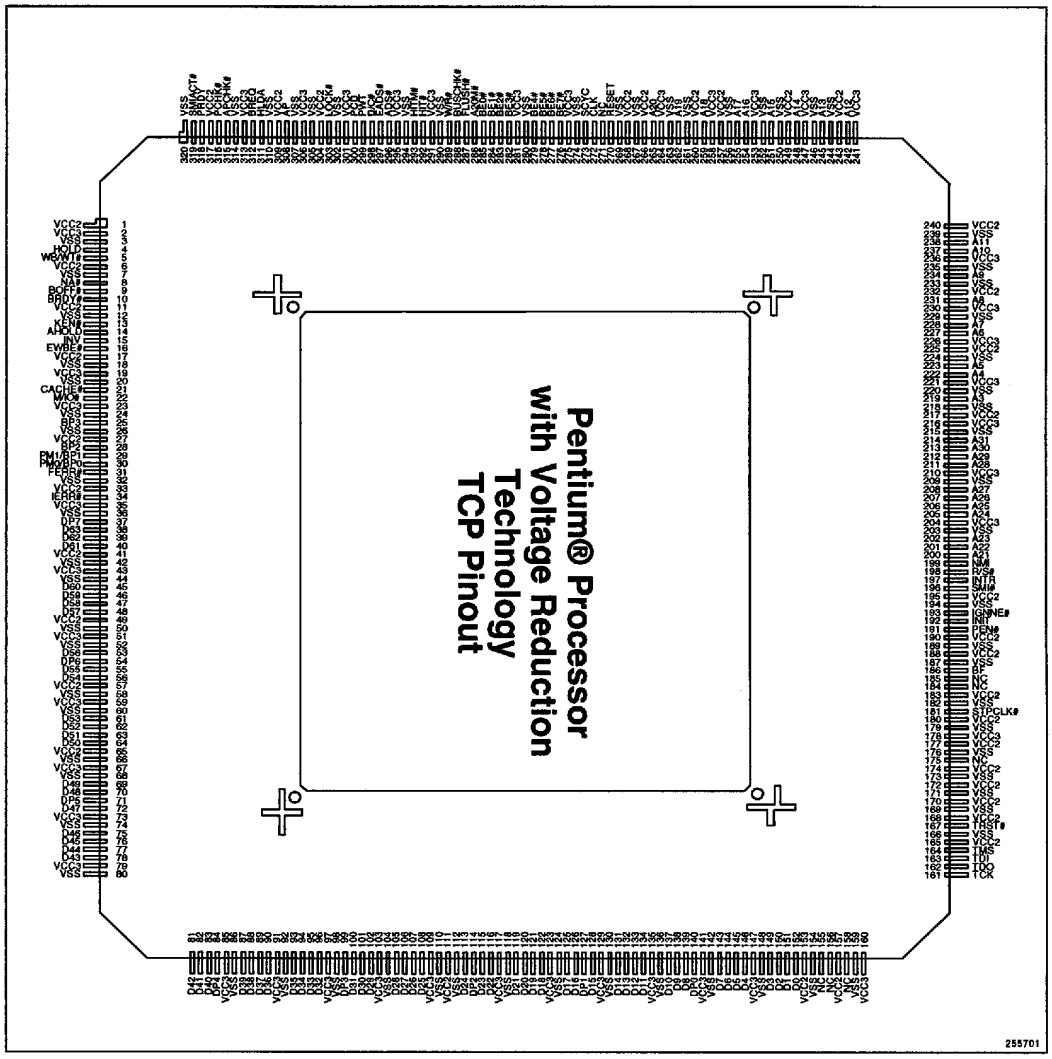


Figure 2. TCP Pentium® Processor Pinout

3.2.2. TCP PENTIUM® PROCESSOR PIN CROSS REFERENCE TABLE

Table 2. TCP Pin Cross Reference by Pin Name

Address									
A3	219	A9	234	A15	251	A21	200	A27	208
A4	222	A10	237	A16	254	A22	201	A28	211
A5	223	A11	238	A17	255	A23	202	A29	212
A6	227	A12	242	A18	259	A24	205	A30	213
A7	228	A13	245	A19	262	A25	206	A31	214
A8	231	A14	248	A20	265	A26	207		
Data									
D0	152	D13	132	D26	107	D39	87	D52	62
D1	151	D14	131	D27	106	D40	83	D53	61
D2	150	D15	128	D28	105	D41	82	D54	56
D3	149	D16	126	D29	102	D42	81	D55	55
D4	146	D17	125	D30	101	D43	78	D56	53
D5	145	D18	122	D31	100	D44	77	D57	48
D6	144	D19	121	D32	96	D45	76	D58	47
D7	143	D20	120	D33	95	D46	75	D59	46
D8	139	D21	119	D34	94	D47	72	D60	45
D9	138	D22	116	D35	93	D48	70	D61	40
D10	137	D23	115	D36	90	D49	69	D62	39
D11	134	D24	113	D37	89	D50	64	D63	38
D12	133	D25	108	D38	88	D51	63		

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

Control							
A20M#	286	BREQ	312	HITM#	293	PM1/BP1	29
ADS#	296	BUSCHK#	288	HLDA	311	PRDY	318
AHOLD	14	CACHE#	21	HOLD	4	PWT	299
AP	308	D/C#	298	IERR#	34	R/S#	198
APCHK#	315	DP0	140	IGNNE#	193	RESET	270
BE0#	285	DP1	127	INIT	192	SCYC	273
BE1#	284	DP2	114	INTR/LINT0	197	SMI#	196
BE2#	283	DP3	99	INV	15	SMIACT#	319
BE3#	282	DP4	84	KEN#	13	TCK	161
BE4#	279	DP5	71	LOCK#	303	TDI	163
BE5#	278	DP6	54	M/IO#	22	TDO	162
BE6#	277	DP7	37	NA#	8	TMS	164
BE7#	276	EADS#	297	NMI/LINT1	199	TRST#	167
BOFF#	9	EWBE#	16	PCD	300	W/R#	289
BP2	28	FERR#	31	PCHK#	316	WB/WT#	5
BP3	25	FLUSH#	287	PEN#	191		
BRDY#	10	HIT#	292	PM0/BP0	30		
				Clock Control			
				BF	186	STPCLK#	181
				CLK	272		

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

$V_{CC}2$*			
1	111	183	257
6	153	188	260
11	157	190	266
17	165	195	268
27	168	217	304
33	170	225	309
41	172	232	317
49	174	240	
57	177	243	
65	180	249	
$V_{CC}3$**			
2	91	178	258
19	97	204	264
23	103	210	275
35	109	216	281
43	117	221	291
51	123	226	295
59	129	230	301
67	135	236	306
73	141	241	313
79	147	247	
85	160	253	

NOTE:

* These $V_{CC}2$ pins are 2.9V inputs for the TCP Pentium® processor with voltage reduction technology, but may change to a different voltage on future offerings of this microprocessor family.

** All $V_{CC}3$ pins will remain at 3.3V power inputs for the TCP Pentium processor.

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

V_{SS}						
3	50	104	166	209	250	302
7	52	110	169	215	252	305
12	58	112	171	218	256	307
18	60	118	173	220	261	310
20	66	124	176	224	263	314
24	68	130	179	229	267	320
26	74	136	182	233	269	
32	80	142	187	235	274	
36	86	148	189	239	280	
42	92	154	194	244	290	
44	98	159	203	246	294	
NC						
155	156	158	175	184	185	271

Table 3. TCP Pin Cross Reference by Pin Number (Pins 1-160)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	VCC2	41	VCC2	81	D42	121	D19
2	VCC3	42	VSS	82	D41	122	D18
3	VSS	43	VCC3	83	D40	123	VCC3
4	HOLD	44	VSS	84	DP4	124	VSS
5	WB/WT#	45	D60	85	VCC3	125	D17
6	VCC2	46	D59	86	VSS	126	D16
7	VSS	47	D58	87	D39	127	DP1
8	NA#	48	D57	88	D38	128	D15
9	BOFF#	49	VCC2	89	D37	129	VCC3
10	BRDY#	50	VSS	90	D36	130	VSS
11	VCC2	51	VCC3	91	VCC3	131	D14
12	VSS	52	VSS	92	VSS	132	D13
13	KEN#	53	D56	93	D35	133	D12
14	AHOLD	54	DP6	94	D34	134	D11
15	INV	55	D55	95	D33	135	VCC3
16	EWBE#	56	D54	96	D32	136	VSS
17	VCC2	57	VCC2	97	VCC3	137	D10
18	VSS	58	VSS	98	VSS	138	D9
19	VCC3	59	VCC3	99	DP3	139	D8
20	VSS	60	VSS	100	D31	140	DP0
21	CACHE#	61	D53	101	D30	141	VCC3
22	M/IO#	62	D52	102	D29	142	VSS
23	VCC3	63	D51	103	VCC3	143	D7
24	VSS	64	D50	104	VSS	144	D6
25	BP3	65	VCC2	105	D28	145	D5
26	VSS	66	VSS	106	D27	146	D4
27	VCC2	67	VCC3	107	D26	147	VCC3
28	BP2	68	VSS	108	D25	148	VSS
29	PM1/BP1	69	D49	109	VCC3	149	D3
30	PM0/BP0	70	D48	110	VSS	150	D2
31	FERR#	71	DP5	111	VCC2	151	D1
32	VSS	72	D47	112	VSS	152	D0
33	VCC2	73	VCC3	113	D24	153	VCC2
34	IERR#	74	VSS	114	DP2	154	VSS
35	VCC3	75	D46	115	D23	155	NC
36	VSS	76	D45	116	D22	156	NC
37	DP7	77	D44	117	VCC3	157	VCC2
38	D63	78	D43	118	VSS	158	NC
39	D62	79	VCC3	119	D21	159	VSS
40	D61	80	VSS	120	D20	160	VCC3

Table 3. TCP Pin Cross Reference by Pin Number (Pins 161-320) (Contd.)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
161	TCK	201	A22	241	VCC3	281	VCC3
162	TDO	202	A23	242	A12	282	BE3#
163	TDI	203	VSS	243	VCC2	283	BE2#
164	TMS	204	VCC3	244	VSS	284	BE1#
165	VCC2	205	A24	245	A13	285	BE0#
166	VSS	206	A25	246	VSS	286	A20M#
167	TRST#	207	A26	247	VCC3	287	FLUSH#
168	VCC2	208	A27	248	A14	288	BUSCHK#
169	VSS	209	VSS	249	VCC2	289	W/R#
170	VCC2	210	VCC3	250	VSS	290	VSS
171	VSS	211	A28	251	A15	291	VCC3
172	VCC2	212	A29	252	VSS	292	HIT#
173	VSS	213	A30	253	VCC3	293	HITM#
174	VCC2	214	A31	254	A16	294	VSS
175	NC	215	VSS	255	A17	295	VCC3
176	VSS	216	VCC3	256	VSS	296	ADS#
177	VCC2	217	VCC2	257	VCC2	297	EADS#
178	VCC3	218	VSS	258	VCC3	298	D/C#
179	VSS	219	A3	259	A18	299	PWT
180	VCC2	220	VSS	260	VCC2	300	PCD
181	STPCLK#	221	VCC3	261	VSS	301	VCC3
182	VSS	222	A4	262	A19	302	VSS
183	VCC2	223	A5	263	VSS	303	LOCK#
184	NC	224	VSS	264	VCC3	304	VCC2
185	NC	225	VCC2	265	A20	305	VSS
186	BF	226	VCC3	266	VCC2	306	VCC3
187	VSS	227	A6	267	VSS	307	VSS
188	VCC2	228	A7	268	VCC2	308	AP
189	VSS	229	VSS	269	VSS	309	VCC2
190	VCC2	230	VCC3	270	RESET	310	VSS
191	PEN#	231	A8	271	NC	311	HLDA
192	INIT	232	VCC2	272	CLK	312	BREQ
193	IGNNE#	233	VSS	273	SCYC	313	VCC3
194	VSS	234	A9	274	VSS	314	VSS
195	VCC2	235	VSS	275	VCC3	315	APCHK#
196	SMI#	236	VCC3	276	BE7#	316	PCHK#
197	INTR	237	A10	277	BE6#	317	VCC2
198	R/S#	238	A11	278	BE5#	318	PRDY
199	NMI	239	VSS	279	BE4#	319	SMIACT#
200	A21	240	VCC2	280	VSS	320	VSS

NOTE:

1. $V_{cc}2$ pins are 2.9V power inputs to the core.
2. $V_{cc}3$ pins are 3.3V power inputs to the core.

3.3. Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active HIGH inputs should be connected to GND (V_{SS}).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

3.4. Quick Pin Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the "Hardware Interface" chapter in the *Pentium® Processor Family Developer's Manual, Volume 1.*

Note that all input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

The pins are classified as Input or Output based on their function in Master Mode. See the Error Detection chapter of the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors,* for further information.

Table 4. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor emulates the address wraparound at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of **address hold**, the processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).
BF	I	**Bus Frequency** determines the bus-to-core ratio. BF is sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF must not change values while RESET is active. For proper operation of the processor, this pin should be strapped high or low. When BF is strapped to V_{cc}, the processor will operate at a 2/3 bus/core frequency ratio. When BF is strapped to V_{ss}, the processor will operate to a 1/2 bus/core frequency ratio. If BF is left floating, the processor defaults to a 2/3 bus/core ratio.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception.
CACHE#	O	For processor-initiated cycles, the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST# and PICD0-1 are specified with respect to the rising edge of CLK. **NOTE:** It is recommended that CLK begin 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63-D56; DP0 applies to D7-D0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the processor address pins to be used for an inquire cycle.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating point error** pin is driven active when an unmasked floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating point error reporting.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor indicating completion of the writeback and invalidation. **NOTE:** If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the processor will resume driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the **bus hold request**, the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor **initialization** input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3; Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the processor will vector to the machine check exception before the beginning of the next instruction.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The **page writethrough** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.
R/S#	I	The **run / stop** input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	**RESET** forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode will be entered or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
$V_{CC}2$	I	These pins are the 2.9V power inputs to the Pentium processor with voltage reduction technology.
$V_{CC}3$	I	These pins are the 3.3V power inputs to the Pentium processor with voltage reduction technology.
V_{SS}	I	These pins are the ground inputs to the Pentium processor with voltage reduction technology.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

3.5. Pin Reference Tables

Table 5. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTE:
All output and input/output pins are floated during tristate test mode (except TDO).

Table 6. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BF	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

Table 7. Input/Output Pins

Name	Active Level	When Floated	Qualified (when an input)	Internal Resistor
A31-A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#-BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown*
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	

NOTES:
All output and input/output pins are floated during tristate test mode (except TDO).
*BE3#-BE0# have pulldowns during RESET only.

3.6. Pin Grouping According to Function

Table 8 organizes the pins with respect to their function.

Table 8. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF
Address Bus	A31-A3, BE7# - BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

4.0. TCP PENTIUM® PROCESSOR ELECTRICAL SPECIFICATIONS

4.1. Maximum Ratings

The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with voltage reduction technology contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Case temperature under bias _____ –65°C to 110°C

Storage temperature _____ –65°C to 150°C

3V Supply voltage with respect to V_{SS} _____ –0.5V to +4.6V

2.9V Supply voltage with respect to V_{SS} _____ –0.5V to +4.1V

3V Only Buffer DC Input Voltage _____ –0.5V to $V_{CC}3$ _____ +0.5; not to exceed 4.6V (2)

5V Safe Buffer DC Input Voltage _____ –0.5V to 6.5V (1,3)

NOTES:

1. Applies to CLK.
2. Applies to all Pentium processors with voltage reduction technology inputs except CLK.
3. See Table 10.

WARNING

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

4.2. DC Specifications

Tables 9, 10 and 11 list the DC specifications which apply to the TCP Pentium processor with voltage reduction technology. The Pentium processor with voltage reduction technology core operates at 2.9V internally while the I/O interface operates at 3.3V. The CLK input may be 3.3V or 5V. Since the 3.3V (5V safe) input levels defined in Table 10 are the same as the 5V TTL levels, the CLK input is compatible with existing 5V clock drivers. The power dissipation specification in Table 12 is provided for design of thermal solutions during operation in a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is used for design of a thermal solution for the device.

4.2.1. POWER SEQUENCING

There is no specific sequence required for powering up or powering down the $V_{CC}2$ and $V_{CC}3$ power supplies. However, for compatibility with future mobile processors, it is recommended that the $V_{CC}2$ and $V_{CC}3$ power supplies be either both on or both off within one second of each other.

Table 9. 3.3V DC Specifications

T_{CASE} = 0 to 95°C; $V_{CC}2$ = 2.9V ±165mV; $V_{CC}3$ = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}3$	Input Low Voltage	–0.3	0.8	V	TTL Level (3)
$V_{IH}3$	Input High Voltage	2.0	$V_{CC}3$+0.3	V	TTL Level (3)
$V_{OL}3$	Output Low Voltage		0.4	V	TTL Level (1) (3)
$V_{OH}3$	Output High Voltage	2.4		V	TTL Level (2) (3)
$I_{CC}2$	Power Supply Current from 2.9V core supply		2096 2515 2800	mA mA mA	@75 MHz (4) @90 MHz (4) @100 MHz (4) (5) (6)
$I_{CC}3$	Power Supply Current from 3.3V I/O buffer supply		265 318 350	mA mA mA	@75 MHz (4) @90 MHz (4) @100 MHz (4) (6)

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3V TTL levels apply to all signals except CLK.
4. This value should be used for power supply design. It was determined using a worst-case instruction mix and V_{CC}+165mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to section 4.3.2.
5. The lower power number is due to a process improvement.
6. Refer to document 242557 for new process specification.

Table 10. 3.3V (5V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}5$	Input Low Voltage	–0.3	0.8	V	TTL Level (1)
$V_{IH}5$	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTES:

1. Applies to CLK only.

Table 11. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4V (3)
I_{IL}	Input Leakage Current		–400	µA	V_{IN} = 0.4V (2)

NOTES:
1. This parameter is for input without pull up or pull down.
2. This parameter is for input with pull up.
3. This parameter is for input with pull down.
4. Guaranteed by design.

Table 12. Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical(1)	Max(2)	Unit	Notes
Active Power Dissipation	2.0–3.0 2.5–3.5 2.8–3.9	6.0 7.3 8.0	Watts Watts Watts	@75 MHz @90 MHz @100 MHz (5)
Stop Grant and Auto Halt Powerdown Power Dissipation		1.0 1.2 1.3	Watts Watts Watts	@75 MHz (3) @90 MHz (3) @100 MHz (3)
Stop Clock Power Dissipation	.02	0.05	Watts	(4)

NOTES:
1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at $V_{CC}2$ = 2.9V and $V_{CC}3$ = 3.3V running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using a worst-case instruction mix with $V_{CC}2$ = 2.9V and $V_{CC}3$ = 3.3V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. Refer to document 242557 for new process specification.

4.3. AC Specifications

The AC specifications of the TCP Pentium processor with voltage reduction technology consist of setup times, hold times, and valid delays at 0 pF. All TCP Pentium processor with voltage reduction technology AC specifications are valid for $V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV and Tcase = 0 to 95°C.

WARNING

Do not exceed the 75-MHz Pentium processor with voltage reduction technology internal maximum frequency of 75 MHz by either selecting the 1/2 bus fraction or providing a clock greater than 50 MHz.

Do not exceed the 90-MHz Pentium processor with voltage reduction technology internal maximum frequency of 90 MHz by either selecting the 1/2 bus fraction or providing a clock greater than 60 MHz.

4.3.1. POWER AND GROUND

For clean on-chip power distribution, the TCP Pentium processor with voltage reduction technology has 37 $V_{CC}2$ (2.9V power), 42 $V_{CC}3$ (3.3V power) and 72 V_{SS} (ground) inputs. Power and ground connections must be made to all external $V_{CC}2$, $V_{CC}3$ and V_{SS} pins of the Pentium processor with voltage reduction technology. On the circuit board all $V_{CC}2$ pins must be connected to a 2.9V V_{CC2} plane (or island) and all $V_{CC}3$ pins must be connected to a 3.3V $V_{CC}3$ plane. All V_{SS} pins must be connected to a V_{SS} plane. Please refer to Table 2 for the list of $V_{CC}2$, $V_{CC}3$ and V_{SS} pins.

4.3.2. DECOUPLING RECOMMENDATIONS

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3V plane and the 2.9V plane (or island). Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3V plane and the 2.9V plane (or island)) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed information, please contact Intel or refer to the *Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems* application note (Order Number 242558).

4.3.3. CONNECTION SPECIFICATIONS

All NC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active high inputs should be connected to ground.

4.3.4. AC TIMINGS FOR A 50-MHZ BUS

The AC specifications given in Table 13 consist of output delays, input setup requirements and input hold requirements for a 50-MHz external bus. All AC specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 13. Mobile Pentium® Processor AC Specifications for 50-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	25.0	50.0	MHz		
t_{1a}	CLK Period	20.0	40.0	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	4	(22)

Table 13. Mobile Pentium® ProcessorAC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_8	APCHK#, IERR#, FERR#, PCHK# Valid Delay	1.0	8.3	nS	4	(4), (22)
t_{9a}	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)
t_{10b}	HITM# Valid Delay	1.1	6.6	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	8.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.5		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	6.0		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	BOFF# Setup Time	5.5		nS	6	
t_{22a}	AHOLD Setup Time	6.0		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	

Table 13. Mobile Pentium® Processor AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25a}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs	6	(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs	6	(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.8		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)

Table 13. Mobile Pentium® Processor AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)
t_{43a}	BF Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)

Table 13. Mobile Pentium® Processor AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

4.3.5. AC TIMINGS FOR A 60-MHZ BUS

The AC specifications given in Table 14 consists of output delays, input setup requirements and input hold requirements for the 60-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 14. Mobile Pentium® Processor with Voltage Reduction Technology AC Specifications for 60-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	30.0	60.0	MHz		
t_{1a}	CLK Period	16.67	33.33	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	(22)
t_{6e}	A3-A31 Valid Delay	1.1	6.3	nS	4	(22)

Table 14. Mobile Pentium® Processor AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	4	(4), (22)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4), (22)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	4	(22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.5		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	

Table 14. Mobile Pentium® Processor AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	3.0		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)

Table 14. Mobile Pentium® Processor AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)
t_{43a}	BF Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

4.3.6. AC TIMINGS FOR A 66-MHZ BUS

The AC specifications given in Table 15 consist of output delays, input setup requirements and input hold requirements for the 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 15. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	PWT, PCD, BE0-7#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	nS	4	
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	
t_{6d}	ADS# Valid Delay	1.0	6.0	nS	4	
t_{6e}	A3-A31 Valid Delay	1.1	6.3	nS	4	
t_{6f}	M/IO# Valid Delay	1.0	5.9	nS	4	
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	4	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4)
t_{9a}	BREQ Valid Delay	1.0	8.0	nS	4	(4)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	nS	4	(4)

Table 15. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{9c}	HLDA Valid Delay	1.0	6.8	nS	4	(4)
t_{10a}	HIT# Valid Delay	1.0	6.8	nS	4	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	4	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.0		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		nS	6	
t_{24b}	PEN# Setup Time	4.8		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)

Table 15. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	2.8		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS	7	To RESET falling edge (1), (21)

Table 15. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43a}	BF, CPUTYP Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

1. Not 100 percent tested. Guaranteed by design.
2. TTL input test waveforms are assumed to be 0 to 3V transitions with 1V/nS rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8V/ns ≤ CLK input rise/fall time ≤ 8V/ns.
6. 0.3V/ns ≤ input rise/fall time ≤ 5V/ns.
7. Referenced to TCK rising edge.

8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings (t_{55-58}).
11. Setup time is required to guarantee recognition on a specific clock.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5V.
14. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF should be strapped to $V_{CC}3$ or left floating.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
21. BUSCHK# is used as a reset configuration signal to select buffer size.
22. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

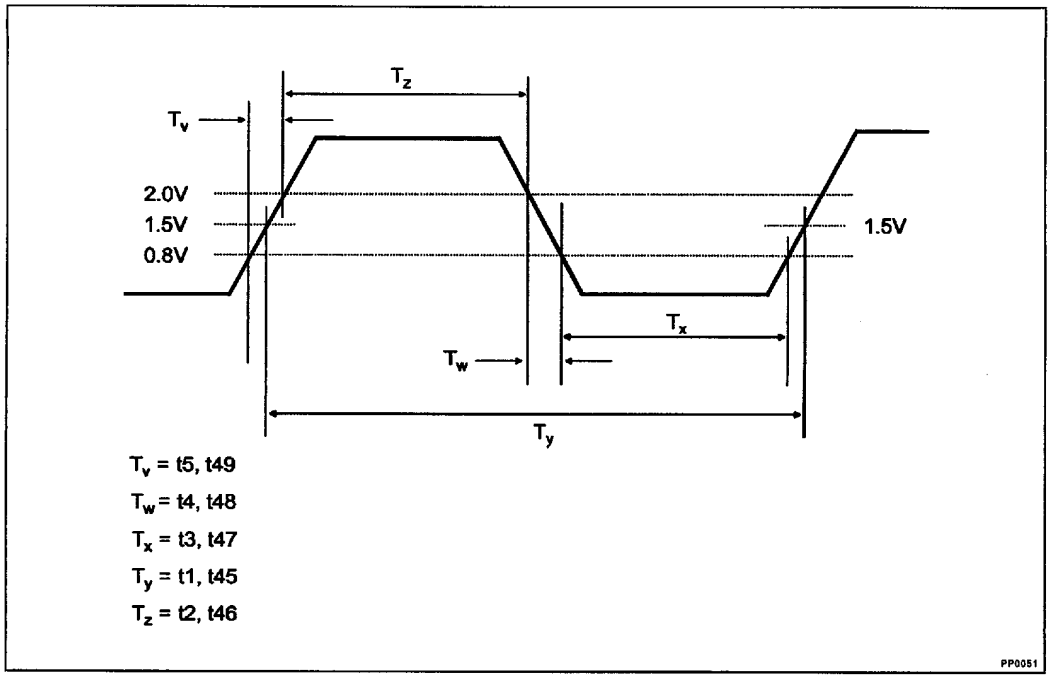


Figure 3. Clock Waveform

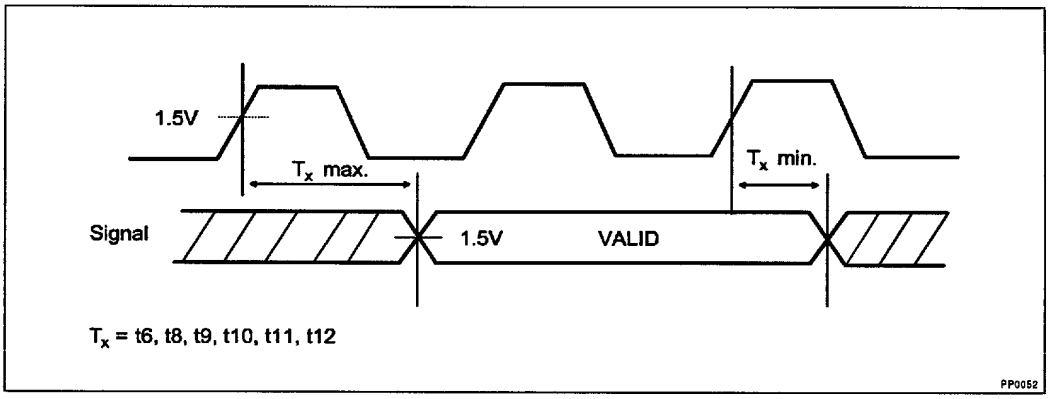


Figure 4. Valid Delay Timings

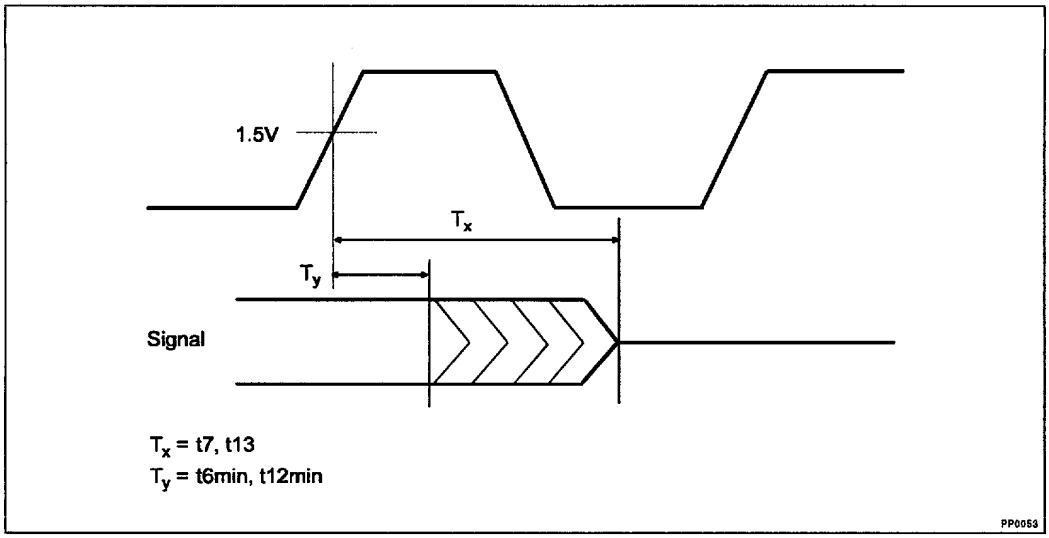


Figure 5. Float Delay Timings

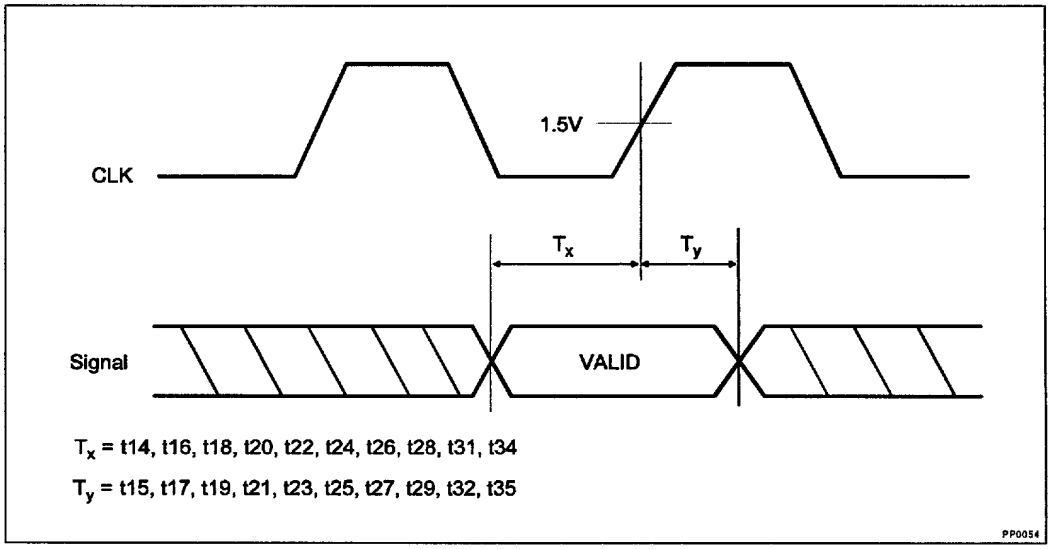


Figure 6. Setup and Hold Timings

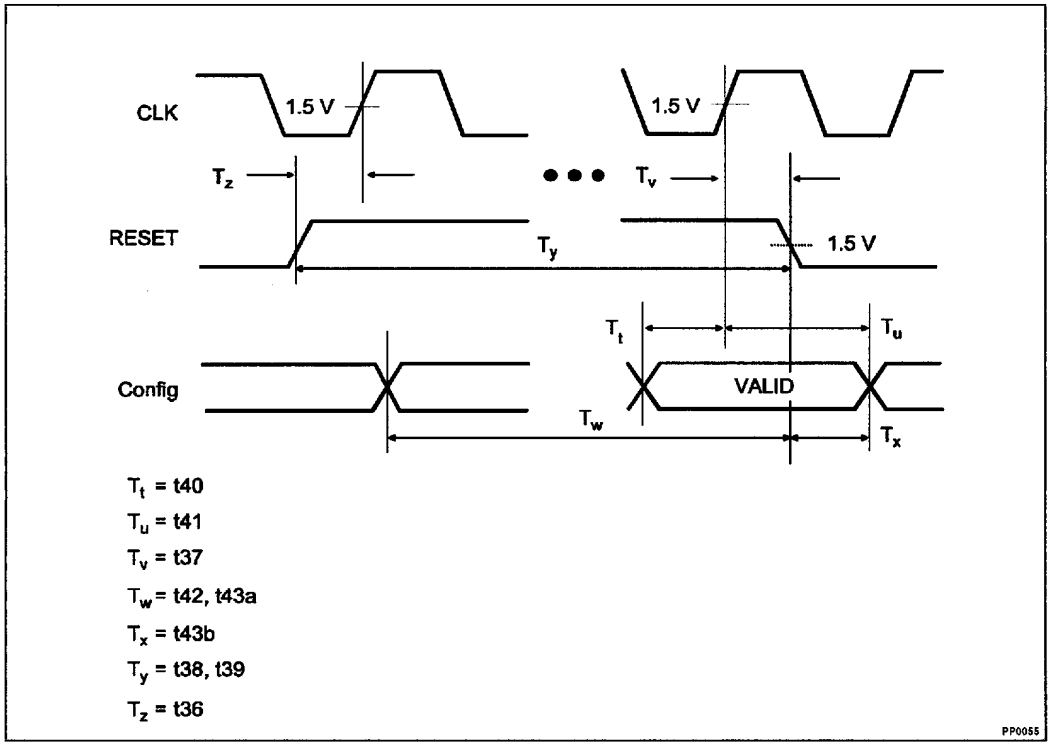


Figure 7. Reset and Configuration Timings

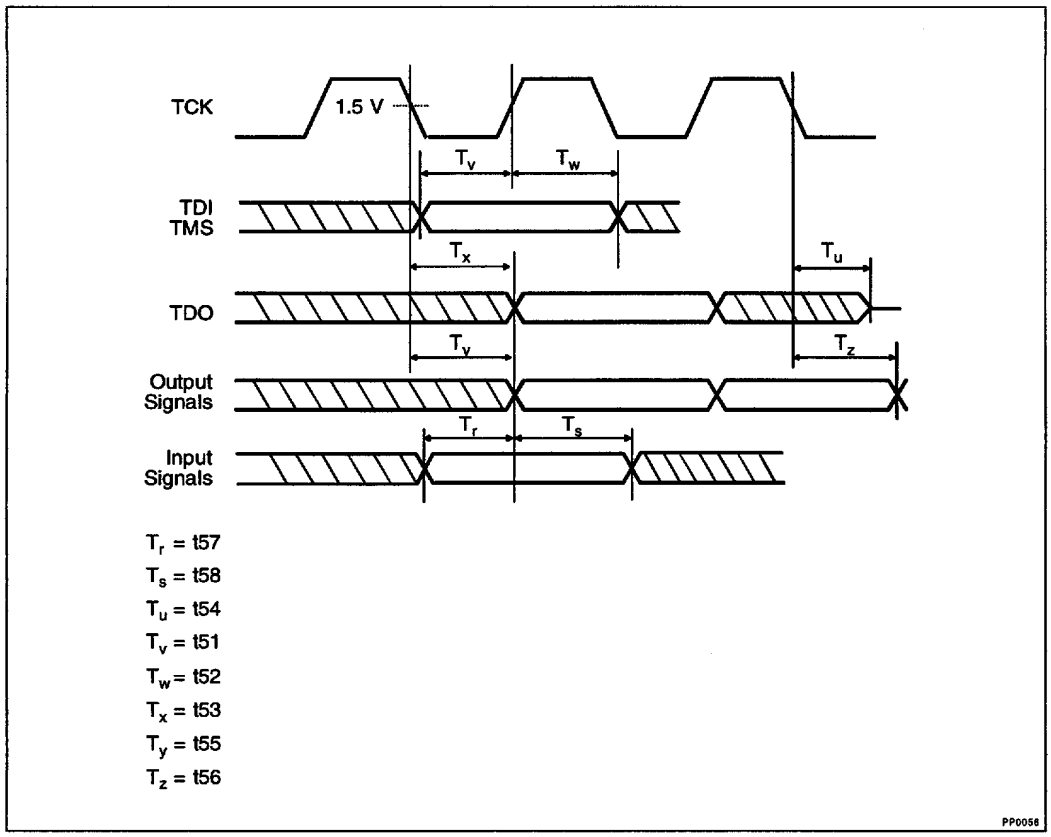


Figure 8. Test Timings

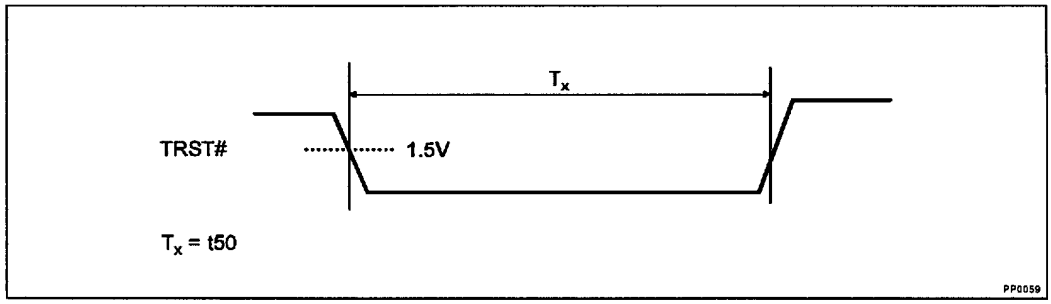


Figure 9. Test Reset Timings

4.4. I/O Buffer Models

This section describes the I/O buffer models of the Pentium processor with voltage reduction technology.

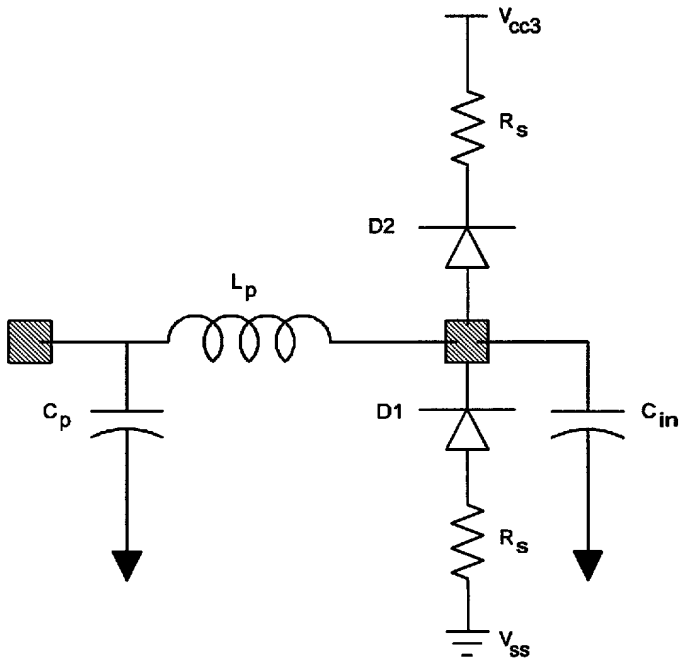
The first order I/O buffer model is a simplified representation of the complex input and output buffers used in the Pentium processor with voltage reduction technology. Figures 10 and 11 show the structure of the input buffer model and Figure 12 shows the output buffer model. Tables 16 and 17 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

The following two models represent the input buffer models. The first model, Figure 10, represents all of the input buffers except for a special group of input buffers. The second model, Figure 11, represents these special buffers. These buffers are the inputs: AHOLD, EADS#, KEN#, WB/WT#, INV, NA#, EWBE#, BOFF# and CLK.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note, however, some signal quality specifications require that the diodes be removed from the input model. The series resistors (Rs) are a part of the diode model. Remove these when removing the diodes from the input model.



Note: V_{CC} in Figure 10 refers to the I/O buffer $V_{CC}3$.

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Figure 10. Input Buffer Model, Except Special Group

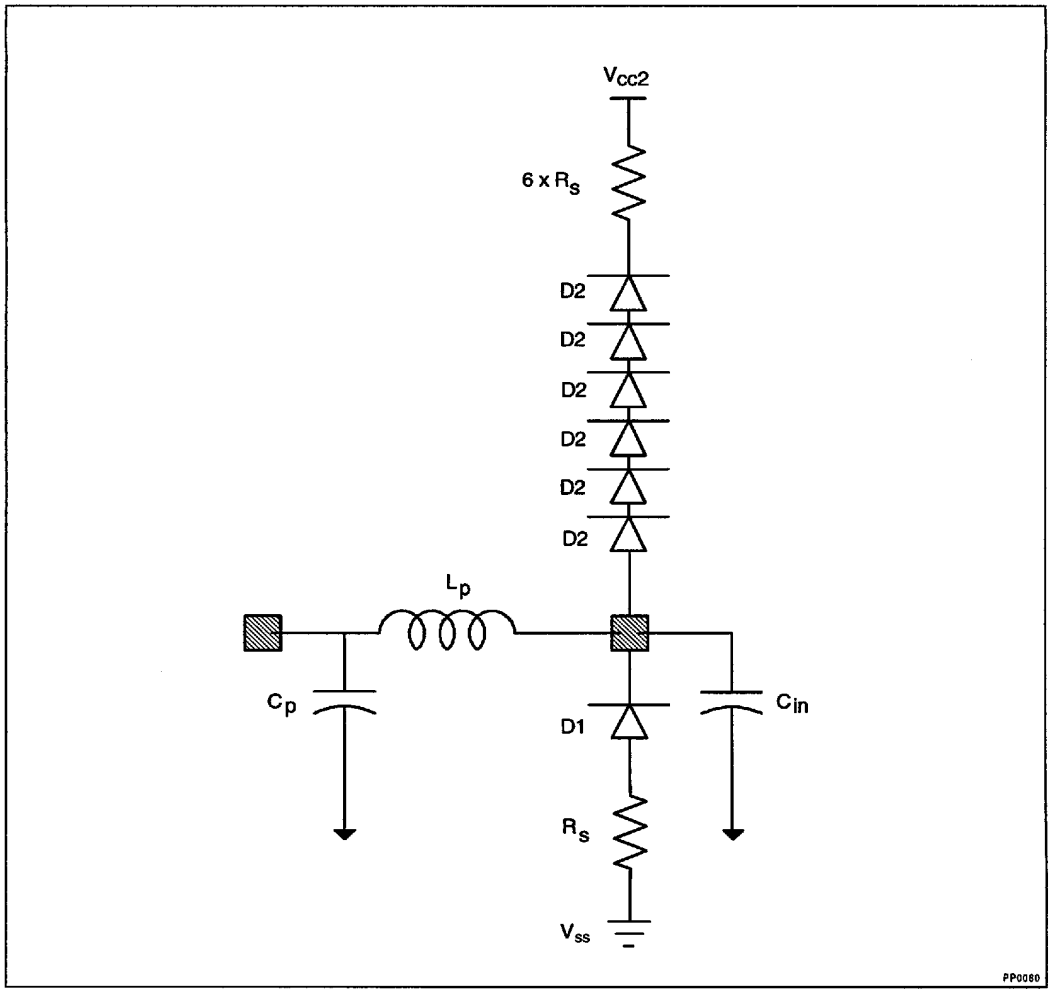

Figure 11. Input Buffer Model for Special Group

Table 16. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
Cin	Minimum and Maximum value of the capacitance of the input buffer model
Lp	Minimum and Maximum value of the package inductance
Cp	Minimum and Maximum value of the package capacitance
Rs	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 12 shows the structure of the output buffer model. This model is used for all of the output buffers of the Pentium processor with voltage reduction technology.

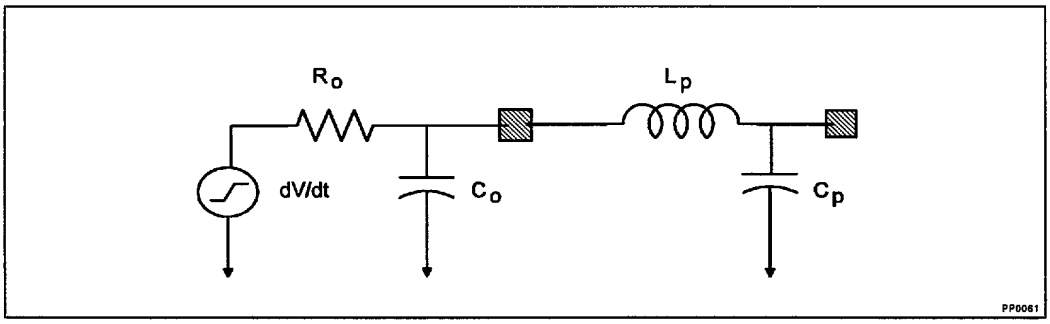

Figure 12. First Order Output Buffer Model

Table 17. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
Ro	Minimum and maximum value of the output impedance of the output buffer model
Co	Minimum and Maximum value of the capacitance of the output buffer model
Lp	Minimum and Maximum value of the package inductance
Cp	Minimum and Maximum value of the package capacitance

4.4.1. BUFFER MODEL PARAMETERS

This section gives the parameters for each TCP Pentium processor with voltage reduction technology input, output and bidirectional signal, as well as the settings for the configurable buffers.

Some pins on the TCP Pentium processor with voltage reduction technology have selectable buffer sizes. These pins use the configurable output buffer EB2. Table 18 shows the drive level for BRDY# required at the falling edge of RESET to select the buffer strength. The buffer sizes selected should be the appropriate size required; otherwise AC timings might not be met, or too much overshoot and ringback may occur. There are no other selection choices; all of the configurable buffers get set to the same size at the same time.

The input, output and bidirectional buffer values of the TCP Pentium processor with voltage reduction technology are listed in Table 20. This table contains listings for all three types, do not get them confused during simulation. When a bidirectional pin is operating as an input, use the Cin, Cp and Lp values; if it is operating as a driver, use all of the data parameters.

Please refer to Table 19 for the groupings of the buffers.

Table 18. Buffer Selection Chart

Environment	BRDY#	Buffer Selection
Typical Stand Alone Component	1	EB2
Loaded Component	0	EB2A

NOTES:
For correct buffer selection, the BUSCHK# signal must be held inactive (high) at the falling edge of RESET.

Table 19. TCP Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	I		ER0
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE[7:5]#, BP[3:2], BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO, U/O#	O	ED1	
A[31:21], AP, BE[4:0]#, CACHE#, D/C#, D[63:0], DP[8:0], HLDA, LOCK#, M/IO#, SCYC	I/O	EB1	EB1
A[20:3], ADS#, HITM#, W/R#	I/O	EB2/EB2A	EB2/EB2A
HIT#	I/O	EB3	EB3

Table 20. TCP Pentium® Processorlnput, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/nsec)		Ro (Ohms)		Cp (pF)		Lp (nH)		Co/Cin (pF)	
		min	max	min	max	min	max	min	max	min	max
ER0	Rising					0.3	0.4	3.9	5.0	0.8	1.2
(input)	Falling					0.3	0.4	3.9	5.0	0.8	1.2
ER1	Rising					0.2	0.5	3.1	6.0	0.8	1.2
(input)	Falling					0.2	0.5	3.1	6.0	0.8	1.2
ED1	Rising	3/3.0	3.7/0.9	21.6	53.1	0.3	0.6	3.7	6.6	2.0	2.6
(output)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.3	0.6	3.7	6.6	2.0	2.6
EB1	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.5	2.9	6.1	2.0	2.6
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.5	2.9	6.1	2.0	2.6
EB2	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.5	3.1	6.4	9.1	9.7
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.5	3.1	6.4	9.1	9.7
EB2A	Rising	3/2.4	3.7/0.9	10.1	22.4	0.2	0.5	3.1	6.4	9.1	9.7
(bidir)	Falling	3/2.4	3.7/0.9	9.0	21.2	0.2	0.5	3.1	6.4	9.1	9.7
EB3	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.4	3.2	4.1	3.3	3.9
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.4	3.2	4.1	3.3	3.9
EB4 (1)	Rising	3/3.0	3.7/0.9	21.6	53.1	0.3	0.4	4.0	4.1	5.0	7.0
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.3	0.4	4.0	4.1	5.0	7.0

Table 21. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4e-14A	2.78e-16A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 ohms	6.5 ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983V	0.967V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

4.4.2. SIGNAL QUALITY SPECIFICATIONS

Signals driven by the system into the Pentium processor with voltage reduction technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters: Ringback and Settling Time.

4.4.2.1. Ringback

Excessive ringback can contribute to long-term reliability degradation of the Pentium processor with voltage reduction technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below $V_{CC}3$ (or above V_{SS}) relative to $V_{CC}3$ (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

Maximum Ringback on Inputs = 0.8V (with diodes)

If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (Undershoot) is the absolute value of the maximum voltage above $V_{CC}3$ (below V_{SS}). The guideline assumes the absence of diodes on the input.

- Maximum Overshoot/Undershoot on 5V 82497 Cache Controller, and 82492 Cache SRAM Inputs (CLK and PICCLK only) = 1.6V above $V_{CC}5$ (without diodes)
- Maximum Overshoot/Undershoot on 3.3V Pentium processor with voltage reduction technology Inputs (not CLK) = 1.4V above $V_{CC}3$ (without diodes)

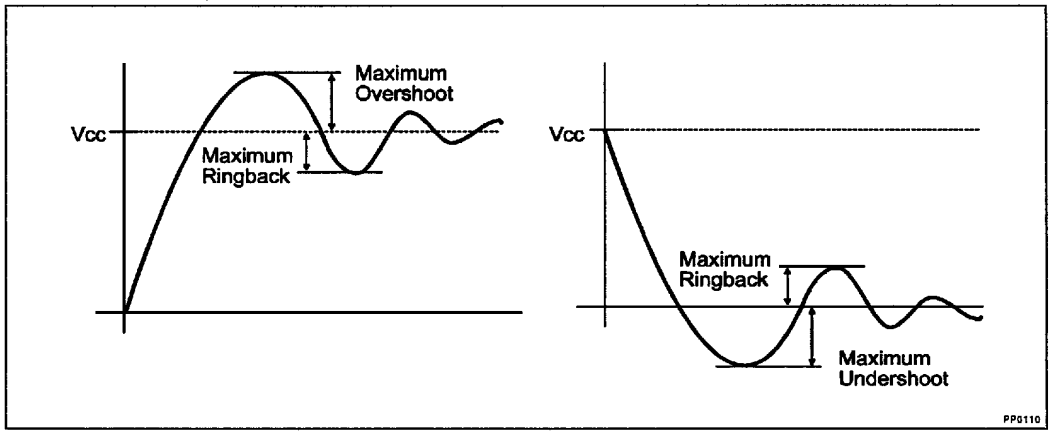

Figure 13. Overshoot/Undershoot and Ringback Guidelines

4.4.2.2. Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10 percent of $V_{CC}3$ or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second-order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur, simulate signal trace with D.C. diodes in place at the receiver pin. The D.C. diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, tuning of the layout is required.
5. Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled.

A typical design method would include a settling time that ensures a signal is within 10 percent of $V_{CC}3$ or V_{SS} for at least 2.5 ns prior to the end of the CLK period.

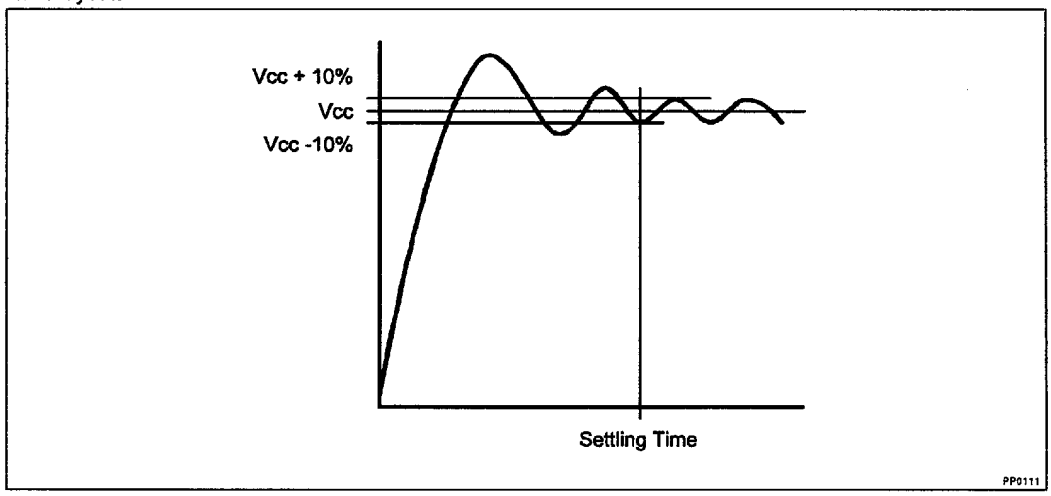

Figure 14. Settling Time

5.0. TCP PENTIUM® PROCESSOR MECHANICAL SPECIFICATIONS

Today's portable computers face the challenge of meeting desktop performance in an environment that is constrained by thermal, mechanical and electrical design considerations. These considerations have driven the development and implementation of Intel's Tape Carrier Package (TCP). The Intel TCP has been designed to offer a high pin count, low profile, reduced footprint package with uncompromised thermal and electrical performance. Intel continues to provide packaging solutions that meet our rigorous criteria for quality and performance, and this new entry into the Intel package portfolio is no exception.

Key features of the TCP include: surface mount technology design, lead pitch of 0.25 mm, polyimide body size of 24 mm and polyimide up for pick-and-place handling. TCP components are shipped with the leads flat in slide carriers, and are designed to be excised and lead formed at the customer manufacturing site. Recommendations for the manufacture of this package are included in Chapter 12 of the *1996 Packaging Data Book*.

Figure 15 shows a cross-sectional view of the TCP as mounted on the Printed Circuit Board. Figures 16 and 17 show the TCP as shipped in its slide carrier, and key dimensions of the carrier and package. Figure 18 shows a cross-section detail of the package. Figure 19 shows an enlarged view of the outer lead bond area of the package.

Tables 22 and 23 provide the Pentium processor with voltage reduction technology TCP dimensions.

5.1. TCP Mechanical Diagrams

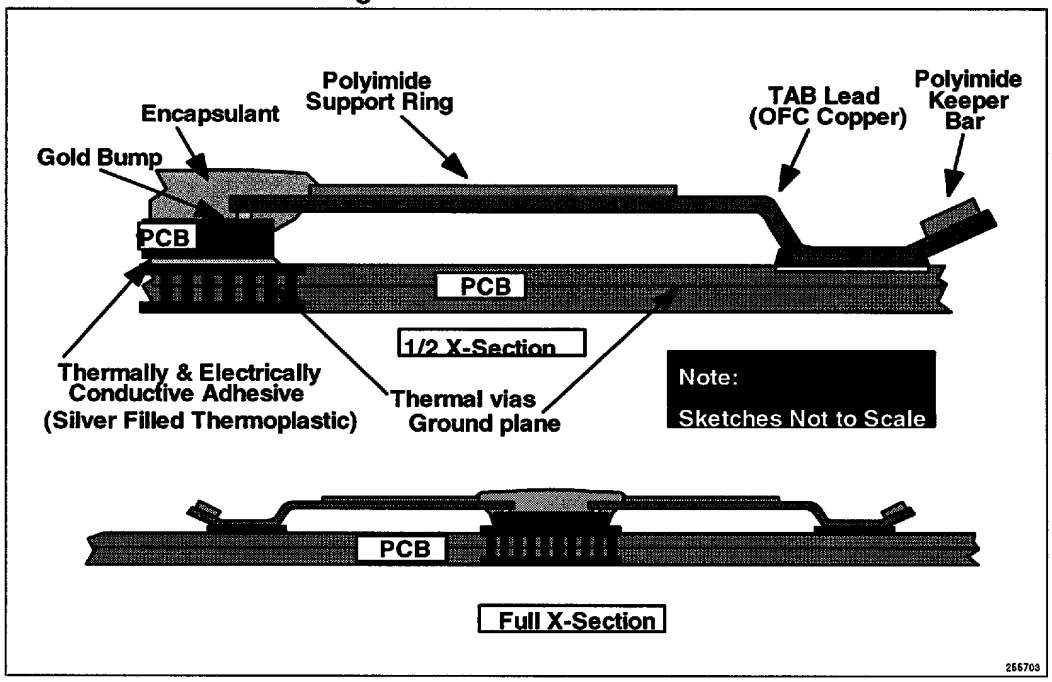

Figure 15. Cross-Sectional View of the Mounted TCP

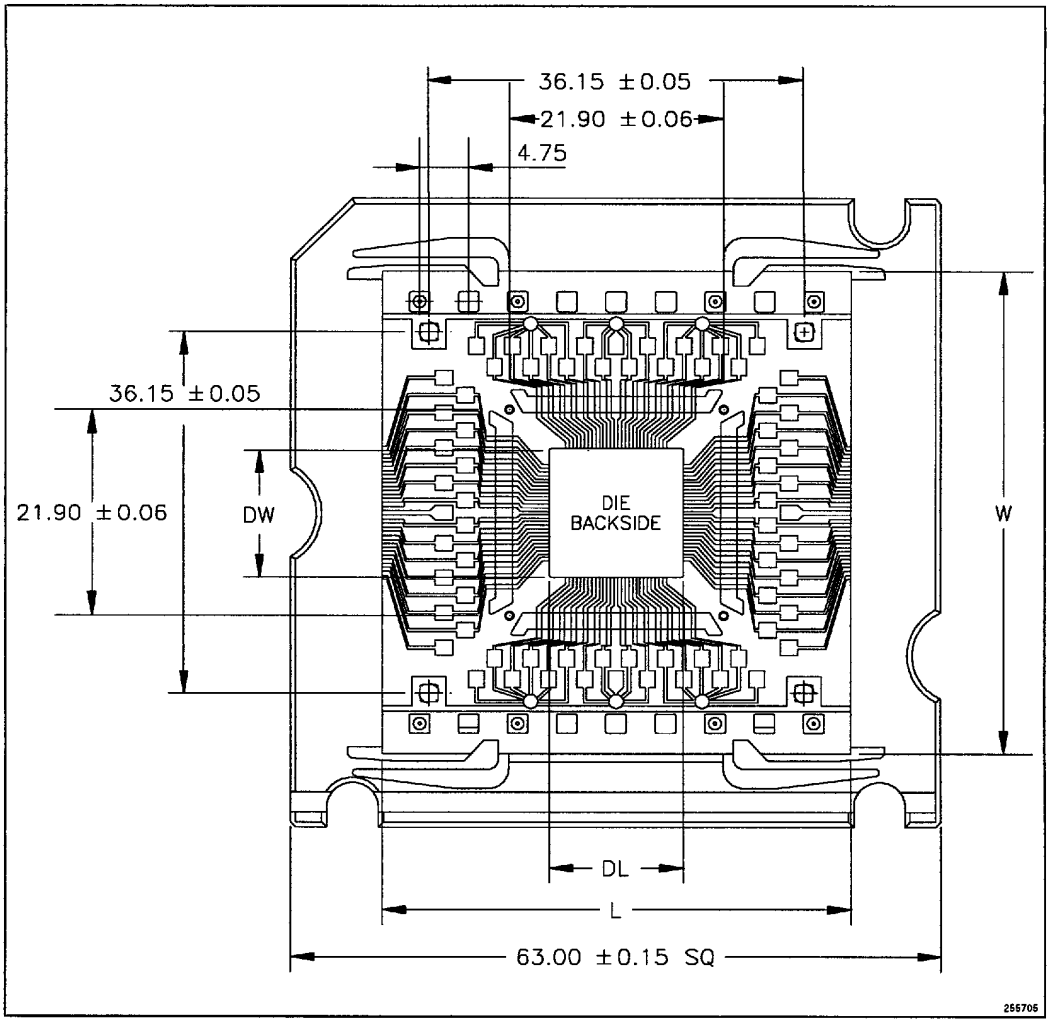

Figure 16. One TCP Site in Carrier (Bottom View of Die)

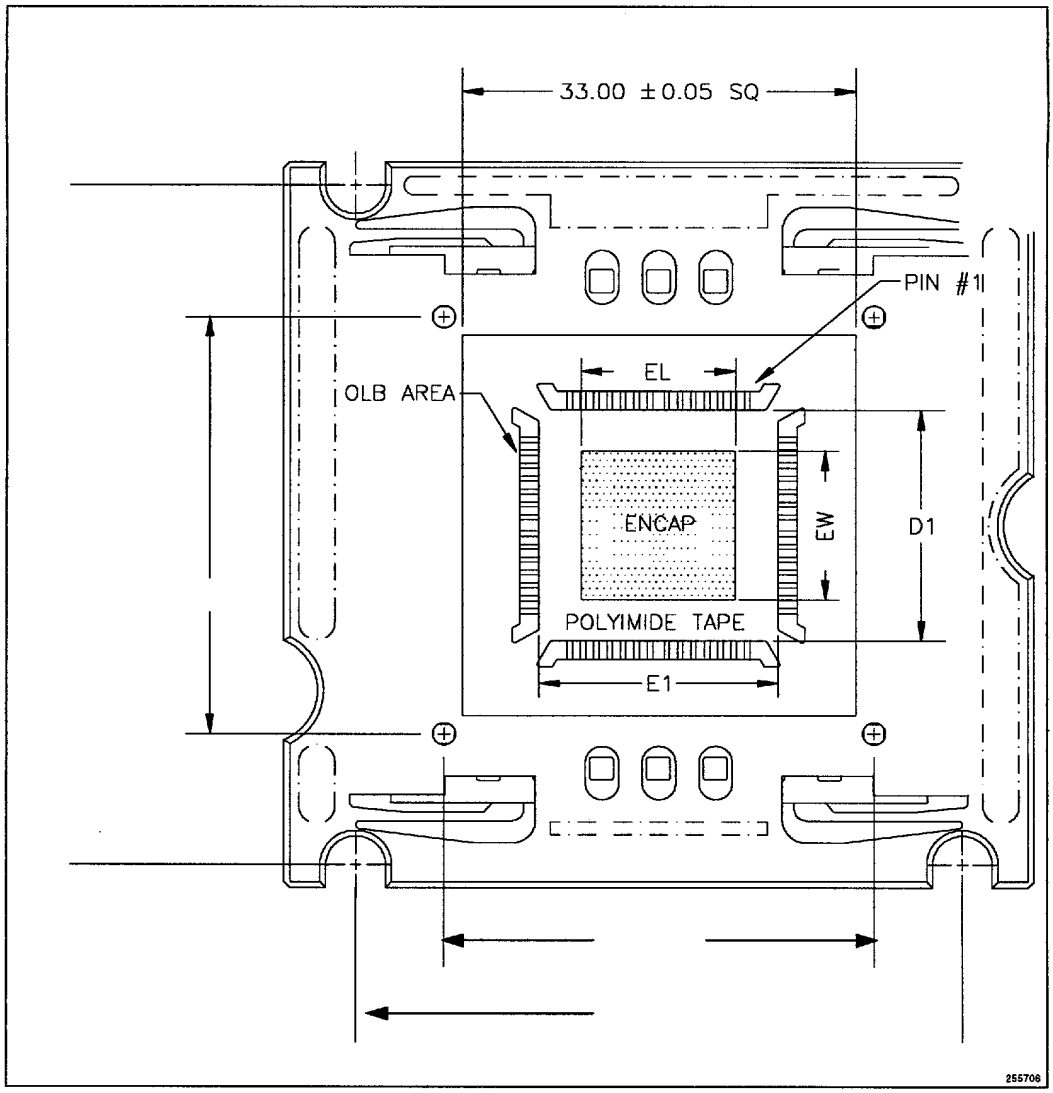

Figure 17. One TCP Site in Carrier (Top View of Die)

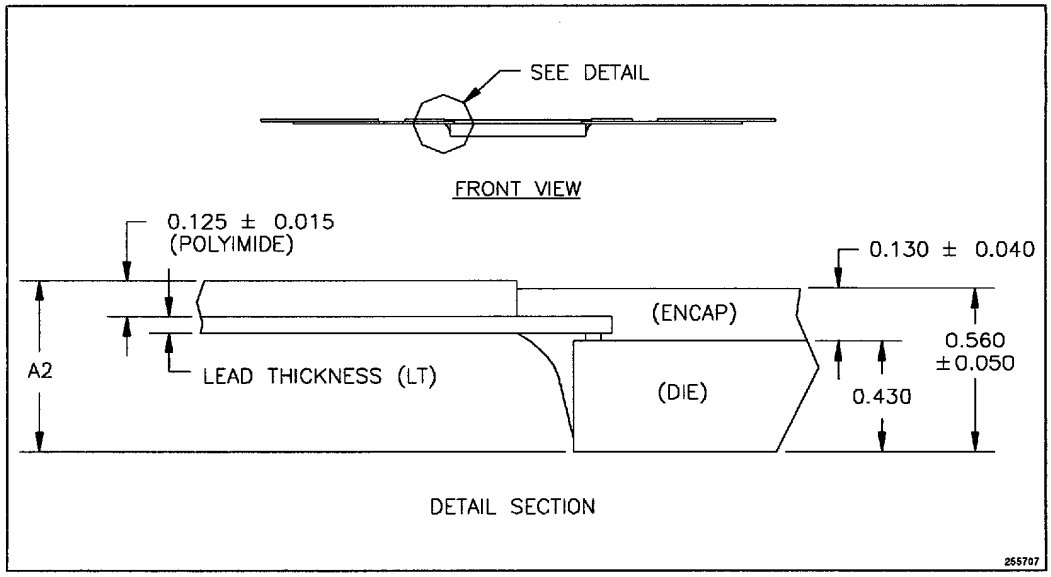

Figure 18. One TCP Site (Cross-Sectional Detail)

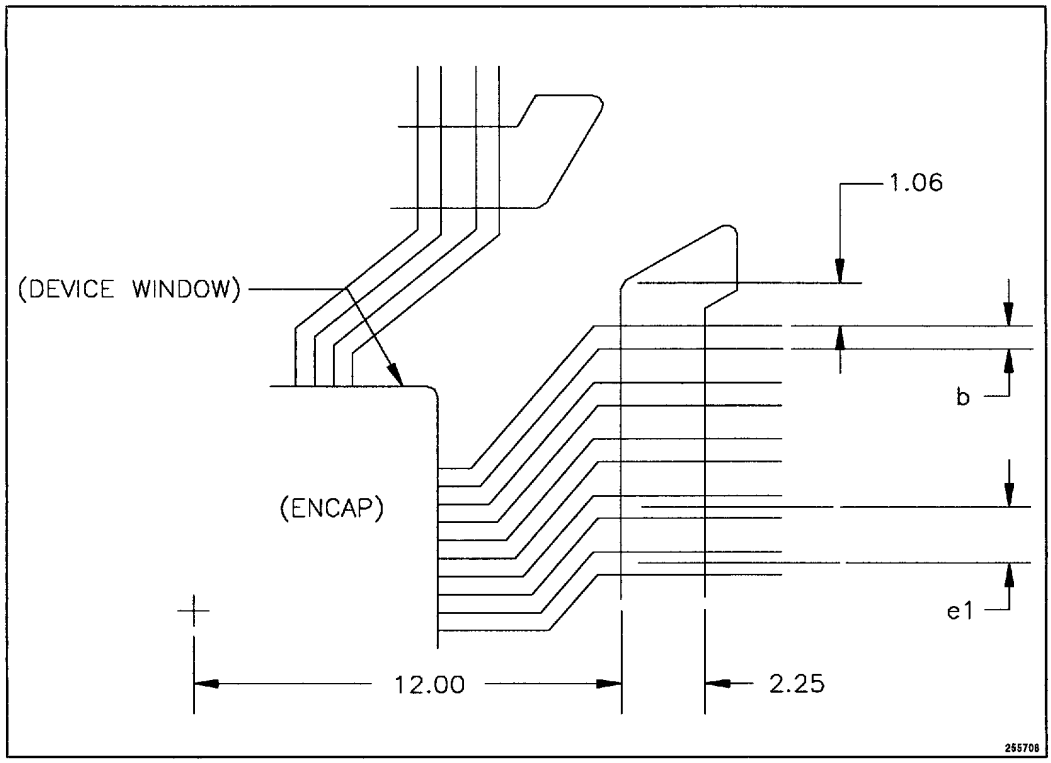

Figure 19. Outer Lead Bond (OLB) Window Detail

Table 22. TCP Key Dimensions

Symbol	Description	Dimension
N	Leadcount	320 leads
W	Tape Width	48.18 ±0.12
L	Site Length	(43.94) reference only
e1	Outer Lead Pitch	0.25 nominal
b	Outer Lead Width	0.10 ±0.01
D1,E1	Package Body Size	24.0 ±0.1
A2	Package Height	min--0.605 ±0.030 max--0.615 ±0.030
DL	Die Length	min--9.929 ±0.015 max--13.302 ±0.015
DW	Die Width	min--9.152 ±0.015 max--12.235 ±0.015
LT	Lead Thickness	min--0.025 max--0.035
EL	Encap Length	min--(10.56) reference only max--(13.94) reference onlly
EW	Encap Width	min--(9.78) reference only max--(12.87) reference only

NOTES:
Dimensions are in millimeters unless otherwise noted.
Dimensions in parentheses are for reference only.

Table 23. Mounted TCP Dimensions

Description	Dimension
Package Height	0.75 maximum
Terminal Dimension	29.5 nominal
Package Weight	0.5 g maximum

NOTE:
Dimensions are in millimeters unless otherwise noted.
Package terminal dimension (lead tip-to-lead tip) assumes the use of a keeper bar.

6.0. TCP PENTIUM® PROCESSOR THERMAL SPECIFICATIONS

The TCP Pentium processor with voltage reduction technology is specified for proper operation when the case temperature, T_{CASE}, (T_C) is within the specified range of 0 °C to 95 °C.

6.1. Measuring Thermal Values

To verify that the proper T_C (case temperature) is maintained for the Pentium processor, it should be measured at the center of the package top surface (encapsulant). To minimize any measurement errors, the following techniques are recommended:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using highly thermally conductive cements. Intel's laboratory testing was done by using Omega Bond (part number: OB-100).
- The thermocouple should be attached at a 90° angle as shown in Figure 20.

6.2. Thermal Equations

For the Pentium processor with voltage reduction technology, an ambient temperature (T_A) is not specified directly. The only requirement is that the case temperature (T_C) is met. The ambient temperature can be calculated from the following equations:

$$T_J = T_C + P \times \theta_{JC}$$
$$T_A = T_J - P \times \theta_{JA}$$
$$T_A = T_C - (P \times \theta_{CA})$$
$$T_C = T_A + P \times [\theta_{JA} - \theta_{JC}]$$
$$\theta_{CA} = \theta_{JA} - \theta_{JC}$$

where,

T_A and T_C are ambient and case temperatures (°C)

θ_{CA} = Case-to-Ambient thermal resistance (°C/W)

θ_{JA} = Junction-to-Ambient thermal resistance (°C/W)

θ_{JC} = Junction-to-Case thermal resistance (°C/W)

P = maximum power consumption (Watts)

P (maximum power consumption) is specified in section 4.2.

6.3. TCP Thermal Characteristics

The primary heat transfer path from the die of the TCP is through the back side of the die and into the PC board. There are two thermal paths traveling from the PC board to the ambient air. One is the spread of heat within the board and the dissipation of heat by the board to the ambient air. The other is the transfer of heat through the board and to the opposite side where thermal enhancements (e.g., heat sinks, pipes) are attached. Solder-side heat sinking, compared to TCP component-side heat sinking, is the preferred method due to reduced risk of die damage, easier mechanical implementation and larger surface area for attachment. However, component-side heat sinking is possible. The design requirements in a component-side thermal solution are: no direct loading of inner lead bonds on the TCP, a maximum force of 4.5 kgf on the center of a clean TCP, no direct loading of the TAB tape or outer lead bonds and controlled board deflection.

6.4. PC Board Enhancements

Copper planes, thermal pads, and vias are design options that can be used to improve heat transfer from the PC board to the ambient air. Tables 24 and 25 present thermal resistance data for copper plane thickness and via effects. It should be noted that although thicker copper planes will reduce the θ_{ca} of a system without any thermal enhancements, they have less effect on the θ_{ca} of a system with thermal enhancements. However, placing vias under the die will reduce the θ_{ca} of a system with and without thermal enhancements.

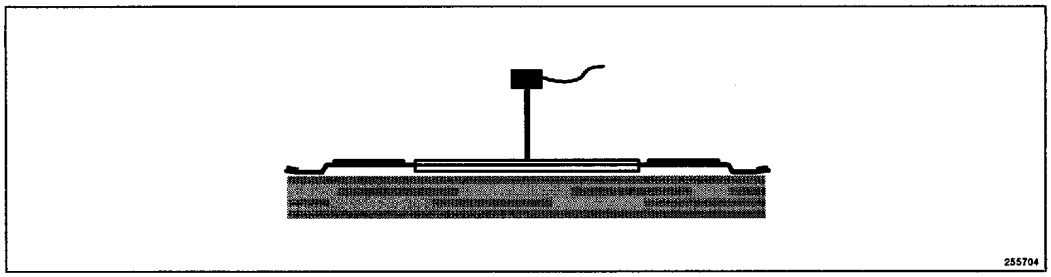

Figure 20. Technique for Measuring Case Temperature (T_C)

Table 24. Thermal Resistance vs. Copper Plane Thickness with and without Enhancements

Copper Plane Thickness*	θ_{CA} (°C/W) No Enhancements	θ_{CA} (°C/W) With Heat Pipe
1 oz. Cu	18	8
3 oz. Cu	14	8

NOTES:
*225 vias underneath the die
(1 oz = 1.3 mil)

Table 25. Thermal Resistance vs. Thermal Vias underneath the Die

Thermal Via Configuration	θ_{CA} (°C/W) No Enhancements
No thermal vias	15
20 mil drill on 40 mil pitch	13

Table 26. Pentium® Processor TCP Thermal Resistance without Enhancements

	θ_{JC} (°C/W)	θ_{CA} (°C/W)
Thermal Resistance without Enhancements	0.8	13.9

Table 27. Pentium® Processor TCP Thermal Resistance with Enhancements (without Airflow)

Thermal Enhancements	θ_{CA} (°C/W)	Notes
Heat sink	11.7	1.2"×1.2"×.35"
Al Plate	8.7	4"×4"×.030"
Al Plate with Heat Pipe	7.8	0.3"×1"×4"

Table 28. TCP Pentium® Processor Thermal Resistance with Enhancements (with Airflow)

Thermal Enhancements	θ_{CA} (°C/W)	Notes
Heat sink with Fan @ 1.7 CFM	5.0	1.2"×1.2"×.35" HS 1"×1"×.4" Fan
Heat sink with Airflow @ 400 LFM	5.1	1.2"x1.2"x.35" HS
Heat sink with Airflow @ 600 LFM	4.3	1.2"×1.2"×.35" HS

HS = heat sink
LFM = Linear Feet/Minute
CFM = Cubic Feet/Minute

6.4.1. STANDARD TEST BOARD CONFIGURATION

All TCP thermal measurements provided in the tables were taken with the component soldered to a 2" x 2" test board outline. This six-layer board contains 13.5 mil drill on 40 mil pitch vias (underneath the die) in the die attach pad which are connected to two 3 oz. copper planes located at layers two and five. For the TCP Pentium processor with voltage reduction technology, the vias in the die attach pad should be connected without thermal reliefs to the ground plane(s). The die is attached to the die attach pad using a thermally and electrically conductive adhesive. This test board was designed to optimize the heat spreading into the board and the heat transfer through to the opposite side of the board.

NOTE

Thermal resistance values should be used as guidelines only, and are highly system dependent. Final system verification should always refer to the case temperature specification.

7.0. SPGA PENTIUM® PROCESSOR WITH VOLTAGE REDUCTION TECHNOLOGY SPECIFICATIONS

7.1. SPGA Pentium® Processor with Voltage Reduction Technology Differences from 3.3V Pentium Processor

All SPGA Pentium processor with voltage reduction technology specifications, except the differences described in this section, are identical to those of the 3.3V Pentium processor.

7.1.1. Features Removed

The following features have been removed for the Pentium processor with voltage reduction technology: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 1 lists the corresponding pins which exist on the 3.3V Pentium processor but have been removed on the Pentium processor with voltage reduction technology.

7.1.2. Maximum Rating

The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the SPGA Pentium processor with voltage reduction technology contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Case temperature under bias.....–65°C to 110°C

Storage temperature.....–65°C to 150°C

3V Supply voltage
with respect to V_{SS}.....–0.5V to +4.6V

2.9V Supply voltage
with respect to V_{SS}.....–0.5V to +4.1V

3V Only Buffer DC Input Voltage..... ..–0.5V to $V_{CC}3$ .....+0.5; not to exceed 4.6V (2)

5V Safe Buffer
DC Input Voltage.....–0.5V to 6.5V (1,3)

NOTES:

1. Applies to CLK.
2. Applies to all SPGA Pentium processor with voltage reduction technology inputs except CLK.
3. See Table 29.

WARNING

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

7.1.3. DC Specifications

Tables 29, 30 and 31 list the DC specifications which apply to the SPGA Pentium processor with voltage reduction technology. The SPGA Pentium processor with voltage reduction technology core operates at 2.9V internally while the I/O interface operates at 3.3V. The CLK input may be at 3.3V or 5V. Since the 3.3V (5V safe) input levels defined in Table 31 are the same as the 5V TTL levels, the CLK input is compatible with existing 5V clock drivers. The power dissipation specification in Table 32 is provided for design of thermal solutions during operation in a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is used for design of a thermal solution for the device.

Table 29. SPGA 3.3V DC Specifications

T_{CASE} = 0 to 85°C; $V_{CC}2$ = 2.9V ±165mV; $V_{CC}3$ = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level (3)
V_{IH3}	Input High Voltage	2.0	$V_{CC}3$+0.3	V	TTL Level (3)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (1) (3)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (2) (3)
$I_{CC}2$	Power Supply Current from 2.9V core supply		2096 2515 2800	mA mA mA	@75 MHz (4) @90 MHz (4) @100 MHz (4)
$I_{CC}3$	Power Supply Current from 3.3V I/O buffer supply		265 318 350	mA mA mA	@75 MHz (4) @90 MHz (4) @100 MHz (4)

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3V TTL levels apply to all signals except CLK.
4. This value should be used for power supply design. It was estimated for a worst-case instruction mix and $V_{CC}2$ = 2.9V ± 165mV and $V_{CC}3$ = 3.3V± 165mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes.
5. The lower power number is due to a process improvement.

Table 30. SPGA 3.3V (5V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	–0.3	0.8	V	TTL Level (1)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTES:

1. Applies to CLK only.

Table 31. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{IH}	Input Leakage Current		200	µA	$V_{IN} = 2.4V$ (3)
I_{IL}	Input Leakage Current		–400	µA	$V_{IN} = 0.4V$ (2)

NOTES:
1. This parameter is for input without pull up or pull down.
2. This parameter is for input with pull up.
3. This parameter is for input with pull down.
4. Guaranteed by design.

Table 32. SPGA Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical(1)	Max(2)	Unit	Notes
Active Power Dissipation	2.0-3.0 2.5-3.5 2.8-3.9	6.0 7.3 8.0	Watts Watts Watts	@75 MHz @90 MHz @100 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		1.0 1.2 1.3	Watts Watts Watts	@75 MHz (3) @90 MHz (3) @100 MHz (3)
Stop Clock Power Dissipation	.02	0.05	Watts	(4)

NOTES:
1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at $V_{CC}2 = 2.9V$ and $V_{CC}3 = 3.3V$ running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using a worst-case instruction mix with $V_{CC}2 = 2.9V$ and $V_{CC}3 = 3.3V$. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. The lower power number is due to a process improvement.

7.1.3.1. Power Sequencing

There is no specific sequence required for powering up or powering down the $V_{CC}2$ and $V_{CC}3$ power supplies. However, for compatibility with future mobile processors, it is recommended that the $V_{CC}2$ and $V_{CC}3$ power supplies be either both on or both off within one second of each other.

7.1.4. AC Specifications

The AC specifications of the SPGA Pentium processor with voltage reduction technology consist of setup times, hold times, and valid delays at 0 pF. All SPGA Pentium processor with voltage reduction technology AC specifications are valid for $V_{CC}2$ = 2.9V ± 165mV, $V_{CC}3$ = 3.3V ± 165mV, and T_{CASE} = 0 to 85°C.

WARNING

Do not exceed the 75-MHz Pentium processor with voltage reduction technology internal maximum frequency of 75 MHz by either selecting the 1/2 bus fraction or providing a clock greater than 50 MHz.

Do not exceed the 90-MHz Pentium processor with voltage reduction technology internal maximum frequency of 90 MHz by either selecting the 1/2 bus fraction or providing a clock greater than 60 MHz.

7.1.4.1. Power and Ground

For clean on-chip power distribution, the SPGA Pentium processor with voltage reduction technology has 25 $V_{CC}2$ (2.9V power), 28 $V_{CC}3$ (3.3V power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external $V_{CC}2$, $V_{CC}3$ and V_{SS} pins of the SPGA Pentium processor with voltage reduction technology. On the circuit board all $V_{CC}2$ pins must be connected to a 2.9V $V_{CC}2$ plane (or island) and all $V_{CC}3$ pins must be connected to a 3.3V $V_{CC}3$ plane. All V_{SS} pins must be connected to a V_{SS} plane. Refer to Table 36 for a listing of $V_{CC}2$ and $V_{CC}3$.

7.1.4.2. Decoupling Recommendations

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3V plane and the 2.9V plane (or island). Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3V plane and the 2.9V plane (or island)) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed informations, please contact Intel or refer to the *Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems* application note (Order Number 242558).

7.1.4.3. Connection Specifications

All NC pins must remain unconnected. Refer to Table 36 for a listing of NC pins.

All RESERVED pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active high inputs should be connected to ground.

7.1.4.4. AC Timings

Table 33 contains the SPGA Pentium processor with voltage reduction technology AC timing changes for 50-MHz bus operation. Table 34 contains the SPGA Pentium processor with voltage reduction technology AC timing changes for 60-MHz bus operation. Table 35 contains the SPGA Pentium processor with voltage reduction technology AC timing changes for 66-MHz bus operation.

7.1.5. Thermal Specifications

The SPGA Pentium processor with voltage reduction technology is specified for proper operation when the case temperature, T_{CASE} (T_C) is within the specified range of 0 °C to 85 °C.

7.1.6. SPGA Package Differences

The SPGA Pentium processor with voltage reduction technology package has a pin array that is mechanically identical to the SPGA version of the 3.3V Pentium, but some pins need to be connected differently. Also, there are small differences in the package dimensions.

7.1.6.1. Pinout

Table 36 lists the SPGA Pentium processor with voltage reduction technology pins that are different from the SPGA 3.3V Pentium processor. Figure 21 depicts the pin side SPGA pinout diagram. The $V_{CC}2$ pins are 3.3V V_{CC} pins for the 3.3V Pentium processor, but will be 2.9V $V_{CC}2$ pins for the SPGA Pentium processor with voltage reduction technology. The NC pins correspond to the unused (for mobile) functions listed in Table 1. They should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings. For a brief functional description of the remaining pins, please refer to Tables 3 and 4. For Input and Output pins reference, please refer to Table 5, 6 and 7.

7.1.6.2. Package Dimensions

The Pentium processor with voltage reduction technology implements an SPGA package that removes the Heat spreader from the top of the package. The package is mechanically equivalent to the package used on the 3.3V Pentium processor C2 stepping except that the SPGA Pentium processor with voltage reduction technology will use the metal lid instead of a ceramic lid, and has the dimensions shown in Figure 22.

7.1.7. I/O Buffer Models

The I/O buffer models provided in section 4.4 of this document apply to both the TCP and SPGA Pentium processor with voltage reduction technology packages, although the capacitance (C_p) and inductance (L_p) parameter values differ between the two packages. For SPGA Pentium processor with voltage reduction technology values, refer to the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors.*

Table 33. SPGA Pentium® Processor AC Timing Changes for 50-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 85°C, C_L = 0pF

Symbol	Parameter	Min	Max	Unit
t_{6a}	W/R# Valid Delay	1.0	7.9	ns
t_{6a}	BE0-7# Valid Delay	1.0	8.1	ns
t_{6c}	LOCK# Valid Delay	1.1	7.9	ns
t_{6a}	PWT Valid Delay	1.0	7.5	ns
t_{6a}	CACHE# Valid Delay	1.0	7.3	ns
t_{6c}	A3-A31 Valid Delay	1.1	8.3	ns
t_{6d}	ADS# Valid Delay	1.0	7.4	ns
t_{10b}	HITM# Valid Delay	1.1	6.6	ns
t_{12}	DP, DBUS Valid Delay	1.3	9.2	ns

Table 34. SPGA Pentium® Processor AC Timing Changes for 60-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 85°C, C_L = 0pF

Symbol	Parameter	Min	Max	Unit
t_{6c}	A3-A31 Valid Delay	1.1	7.7	ns
t_{12}	DP, DBUS Valid Delay	1.3	7.8	ns

Table 35. SPGA Pentium® Processor AC Timing Changes for 66-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit
t_{6a}	BE0-7# Valid Delay	1.0	7.25	nS
t_{6e}	A3-A31 Valid Delay	1.1	7.5	nS
t_{6f}	M/IO# Valid Delay	1.0	7.0	nS
t_{9c}	HLDA Valid Delay	1.0	7.2	nS
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.8	nS

Table 36. SPGA Pentium® Processor with Voltage Reduction Technology $V_{CC}2$ and $V_{CC}3$ Pins

$V_{CC}2$*						
A17	A07	Q01	AA01	AN11		
A15	G01	S01	AC01	AN13		
A13	J01	U01	AE01	AN15		
A11	L01	W01	AG01	AN17		
A09	N01	Y01	AN09	AN19		
$V_{CC}3$						
A19	A27	AE37	AN25	G37	N37	U33
A21	A29	AG37	AN27	J37	Q37	U37
A23	AA37	AN21	AN29	L33	S37	W37
A25	AC37	AN23	E37	L37	T34	Y37
NC**						
A37	AE03	AN35	Q35	W33		
AA03	AE35	H34	R34	W35		
AC03	AL19	J33	S33	Y03		
AD04	AM02	L35	S35	Y35		

NOTE:

*These $V_{CC}2$ pins are 3.3V V_{CC} pins for the SPGA 3.3V Pentium® processor. For the SPGA Pentium processor with voltage reduction technology, these pins are 2.9V $V_{CC}2$ supplies for the SPGA core.

**These NC pins should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings.

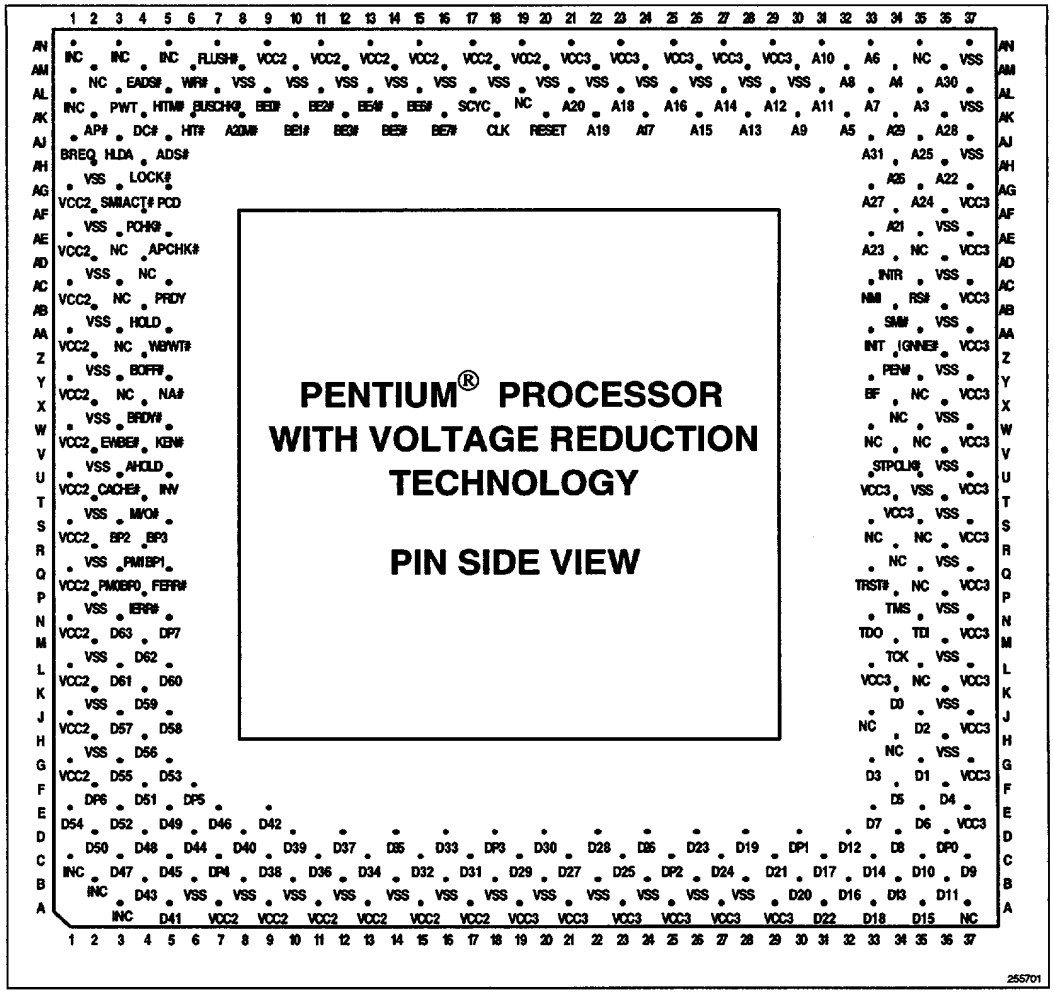

Figure 21. SPGA Pentium® Processor with Voltage Reduction Technology Pinout

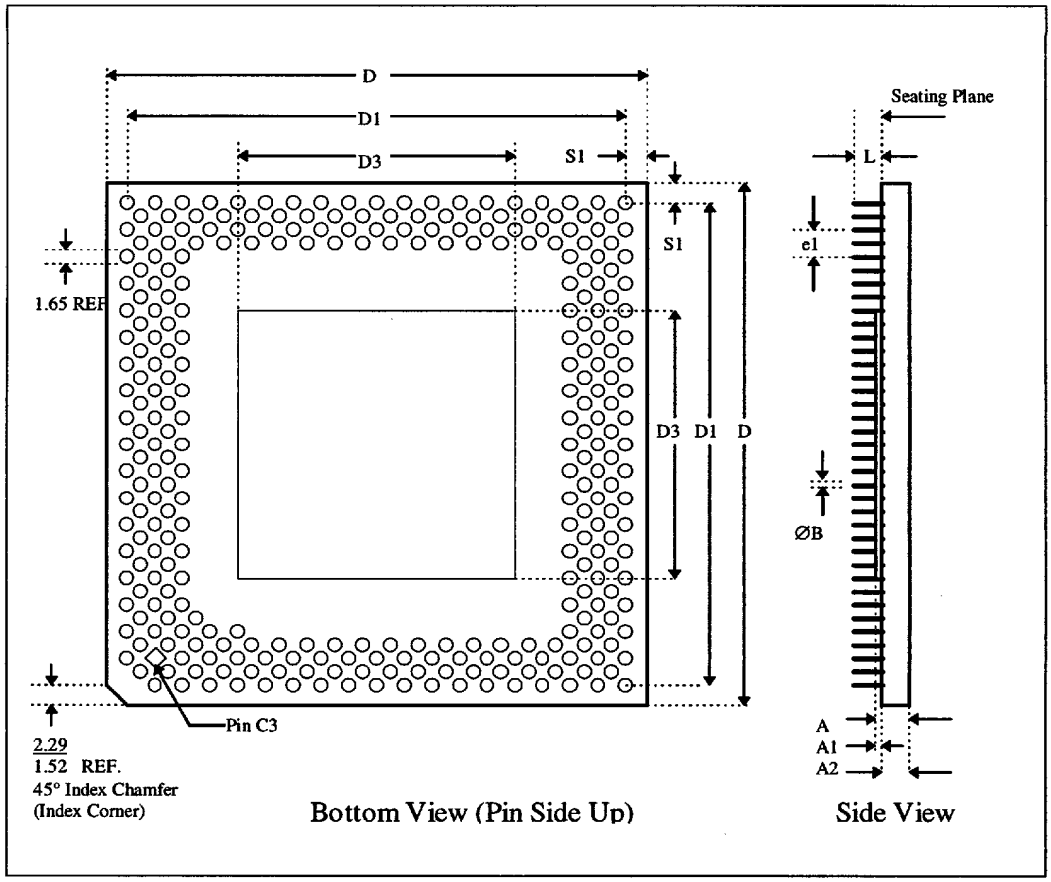

Figure 22. 296-Pin Ceramic Pin Grid Array Package

Table 37. 296-Pin Ceramic Pin Grid Array: The Package Dimensional Specification

	Millimeters			Inches		
Symbol	**Min**	**Max**	**Notes**	**Min**	**Max**	**Notes**
A	3.27	3.83	Ceramic Lid	0.129	0.151	Ceramic Lid
A1	0.66	0.86	Ceramic Lid	0.026	0.034	Ceramic Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D1	45.59	45.85		1.795	1.805	
D3	24.00	24.25	Includes Fillet	0.945	0.955	Includes Fillet
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	1.130	
N	296		Total Pins	296		Total Pins
S1	1.52	2.54		0.060	0.100	