3 Electrical Characteristics

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 7 V
Input voltage range, V_I ..... −0.5 V to V_{DD} + 0.5 V
Analog output short-circuit duration to any power supply or common ..... unlimited
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Junction temperature ..... 175°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltages, AV_{DD}, DV_{DD}	4.75	5	5.25	V
Reference voltage, V_{ref}	1.15	1.235	1.26	V
High-level input voltage, V_{IH}	2.4		V_{DD}+0.5	V
Low-level input voltage, V_{IL}			0.8	V
Output load resistance, R_L		37.5		Ω
FS ADJUST resistor, R_{SET}		523		Ω
Operating free-air temperature, T_A	0		70	°C

3.3 Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −800 µA	2.4			V
V_{OL}	Low-level output voltage	D(0−7), VCLK, RCLK, $\overline{SENSE}$	I_{OL} = 3.2 mA			0.4	V
		HSYNCOUT, VSYNCOUT	I_{OL} = 15 mA			0.4	
		SCLK	I_{OL} = 18 mA			0.4	
V_{ID}	Differential input voltage	ECL inputs		0.6		6	V
V_{IC}	Common-mode input voltage	ECL inputs		2.85	3.15	V_{DD}−0.5	V
I_{IH}	High-level input current	TTL inputs	V_I = 2.4 V			1	µA
		ECL inputs	V_I = 4 V			1	
I_{IL}	Low-level input current	TTL inputs	V_I = 0.8 V			−1	µA
		ECL inputs	V_I = 0.4 V			−1	
I_{DD}	Supply current, pseudo-color mode (see Note 2)	TVP3010-85	V_{DD} = 5		250	280	mA
		TVP3010-110			270	320	
		TVP3010-135			330	380	
		TVP3010-170			390	440	
I_{DD}	Supply current, true-color mode	TVP3010-85	V_{DD} = 5		270	320	mA
		TVP3010-110			320	370	
		TVP3010-135			370	420	
		TVP3010-170			420	475	
I_{OZ}	High-impedance-state output current					10	µA
C_i	Input capacitance	TTL inputs	f = 1 MHz, V_I = 2.4 V		4		pF
		ECL inputs	f = 1 MHz, V_I = 4 V		4		

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTE 2: I_{DD} is measured with dot clock running at the maximum specified frequency, SCLK frequency = dot clock frequency/8 (in pseudo-color modes), and the palette RAM loaded with repeating full-range toggling patterns (00h/00h/00h/00h/FFh/FFh/FFh/FFh). Pseudo-color mode is also known as color indexing mode.

3.4 Operating Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
	Gray scale error				5%	
	Output current (see Note 3)	White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black (7.5 IRE only)	16.74	17.62	18.5	mA
		Black level relative to blank (7.5 IRE only)	0.95	1.44	1.9	mA
		Blank level on IOR, IOB	0	5	50	µA
		Blank level on IOG (with SYNC enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with SYNC enabled)	0	5	50	µA
		One LSB (8/$\overline{6}$ high)		69.1		µA
		One LSB (8/$\overline{6}$ low)		276.4		µA
	DAC-to-DAC matching			2%	5%	
	DAC-to-DAC crosstalk			–20		dB
	Output compliance		–1		1.2	V
	Voltage reference output voltage		1.15	1.235	1.26	V
	Output impedance			50		kΩ
	Output capacitance	f = 1 MHz, I_{OUT} = 0		13		pF
	Sense voltage reference		300	350	400	mV
	Clock and data feedthrough			–20		dB
	Glitch impulse (see Note 4)			50		pV–s
	Pipeline delay, VGA port	Self-clocked timing		18 dot clock		periods
		Externally-clocked timing		15 dot clock		periods
	Pipeline delay, pixel port	Self-clocked timing		2 RCLK + 14 dot clock		periods
		Externally-clocked timing		1 RCLK +14 dot clock		periods

NOTES: 3. Test conditions for RS343-A video signals (unless otherwise specified) can be found in "Recommended Operating Conditions" using external voltage reference V_{ref} = 1.235 V, R_{SET} = 523 Ω. When using the internal voltage reference, R_{SET} may need to be adjusted in order to meet these limits.

4. Glitch impulse does not include clock and data feedthrough. The – 3-dB test bandwidth is twice the clock rate.

3.5 Timing Requirements (see Note 5)

			TVP3010 -85		TVP3010 -110		TVP3010 -135		TVP3010 -170		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Dot clock frequency			85		110		135		170	MHz
	CLK0 frequency for VGA pass-through mode (see Note 6)			85		85		85		85	MHz
t_c	Clock cycle time	TTL	11.8		9.1		7.4		7.1		ns
		ECL	11.8		9.1		7.4		5.8		
t_{su1}	Setup time, RS(0–3) valid before $\overline{RD}$ or $\overline{WR}$↓		10		10		10		10		ns
t_{h1}	Hold time, RS(0–3) valid after $\overline{RD}$ or $\overline{WR}$↓		10		10		10		10		ns
t_{su2}	Setup time, D(0–7) valid before $\overline{WR}$↑		35		35		35		35		ns
t_{h2}	Hold time, D(0–7) valid after $\overline{WR}$↑		0		0		0		0		ns
t_{su3}	Setup time, VGA(0–7) and $\overline{VGABL}$ valid before CLK0↑ (see Note 7)		2		2		2		2		ns
t_{h3}	Hold time, VGA(0–7) and $\overline{VGABL}$ valid after CLK0↑ (see Note 7)		2		2		2		2		ns
t_{su4}	Setup time, P(0–31) and PSEL valid before LCLK↑ (see Note 8)		2		2		2		2		ns
t_{h4}	Hold time, P(0–31) and PSEL valid after LCLK↑ (see Note 8)		5		5		5		5		ns
t_{su5}	Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{SYSBL}$ valid before VCLK↓		5		5		5		5		ns
t_{h5}	Hold time, $\overline{HSYNC}$, VSYNC and $\overline{SYSBL}$ valid after VCLK↓		1		1		1		1		ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low		50		50		50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high		30		30		30		30		ns
t_{w3}	Pulse duration, clock high	TTL	4		3.5		3		3		ns
		ECL	4		3		3		2.5		
t_{w4}	Pulse duration, clock low	TTL	4		3.5		3		3		ns
		ECL	4		3		3		2.5		
t_{w5}	Pulse duration, SFLAG high (see Note 9)		30		30		30		30		ns
t_{w6}	Pulse duration, SCLK high (see Note 9)		15	55	15	55	15	55	15	55	ns

NOTES: 5. TTL input signals are 0 to 3 V with less than 3-ns rise/fall time between the 10% and 90% levels unless otherwise specified. ECL input signals are $V_{DD}-1.8$ V to $V_{DD}-0.8$ V with less than 2-ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D(0–7) output loads are less than 50 pF. All other output loads are less than 50 pF unless otherwise specified.

6. In VGA mode, CLK0 minimum pulse duration for clock low should be greater than 4.8 ns. If VGA switching is to be performed using self-clocked timing, the maximum pixel rate cannot exceed 50 MHz.
7. Reference to CLK0 input only.
8. RCLK is delayed from SCLK in such a way that when RCLK is connected to LCLK, the timing is essentially the same as the TLC3407x family of parts.
9. This parameter applies when the split shift-register transfer (SSRT) function is enabled. See Section 2.15 for details.

3.6 Switching Characteristics

	PARAMETER	TVP3010-85			TVP3010-110			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK frequency ($C_L \leq 15$ pF) (see Note 10)			85			85	MHz
	SCLK frequency ($C_L \leq 60$ pF) (see Note 10)			85			85	MHz
	RCLK/VCLK frequency (see Note 10)			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(0–7) valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(0–7) disabled			17			17	ns
t_{v1}	Valid time, D(0–7) valid after $\overline{RD}$ high	5			5			ns
t_{PLH1}	Propagation delay, SFLAG↑ to SCLK high (see Note 10 and 11)	0		20	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D(0–7) starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to dot clock (internal signal) high/low		7			7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Note 12)	1	2	5	1	2	5	ns
t_{d4}	Delay time, VCLK high/low to RCLK high/low (see Note 12)	1	3	6	1	3	6	ns
t_{d5}	Delay time, RCLK high/low from dot clock high/low (internal signal)		7			7		ns
t_{d6}	Delay time, LCLK from RCLK			t_{RCLK-7}			t_{RCLK-7}	ns
t_{d7}	Delay time, dot clock high to IOR/IOG/IOB active (analog output delay time) (see Note 13)		4			4		ns
t_{d8}	Analog output settling time (see Note 14)		6			6		ns
t_{d9}	Delay time, dot clock high to HSYNCOUT and VSYNCOUT valid		9			9		ns
t_r	Analog output rise time (see Note 15)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 10. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typical 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst-case transition times between 10% and 90% levels less than 4 ns (typical 3 ns).

11. This parameter applies when the split shift-register transfer (SSRT) function is enabled. See Section 2.15 for details.
12. The SCLK and VCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with an RCLK to VCLK ratio of 1:1, a VCLK = RCLK load of 15 pF, and an SCLK load of 60 pF.
13. Measured from the 90% point of the rising edge of the internal dot clock signal to 50% of the full-scale transition
14. Measured from the 50% point of the full-scale transition to the point at which the output has settled within ± 1 LSB (settling time does not include clock and data feedthrough)
15. Measured between 10% and 90% of the full-scale transition

3.6 Switching Characteristics (Continued)

	PARAMETER	TVP3010-135			TVP3010-170			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK frequency ($C_L \leq 15$ pF) (see Note 10)			85			87.5	MHz
	SCLK frequency ($C_L \leq 60$ pF) (see Note 10)			85			85	MHz
	RCLK, VCLK frequency (see Note 10)			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(0–7) valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(0–7) disabled			17			17	ns
t_{v1}	Valid time, D(0–7) valid after $\overline{RD}$ high	5			5			ns
t_{PLH1}	Propagation delay, SFLAG↑ to SCLK high (see Note 10 and 11)	0		20	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D(0–7) starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to dot clock (internal signal) high/low		7			7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Note 12)	1	2	5	1	2	5	ns
t_{d4}	Delay time, VCLK high/low to RCLK high/low (see Note 12)	1	3	6	1	3	6	ns
t_{d5}	Delay time, RCLK high/low from dot clock high/low (internal signal)		7			7		ns
t_{d6}	Delay time, LCLK from RCLK			t_{RCLK-7}			t_{RCLK-7}	ns
t_{d7}	Delay time, dot clock high to IOR/IOG/IOB active (analog output delay time) (see Note 13)		4			4		ns
t_{d8}	Analog output settling time (see Note 14)		6			5		ns
t_{d9}	Delay time, dot clock high to HSYNCOUT and VSYNCOUT valid		9			9		ns
t_r	Analog output rise time (see Note 15)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 10. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typical 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst-case transition times between 10% and 90% levels less than 4 ns (typical 3 ns).

11. This parameter applies when the split shift-register transfer (SSRT) function is enabled. See Section 2.15 for details.
12. The SCLK and VCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with an RCLK to VCLK ratio of 1:1, a VCLK = RCLK load of 15 pF, and an SCLK load of 60 pF.
13. Measured from the 90% point of the rising edge of the internal dot clock signal to 50% of the full-scale transition
14. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough)
15. Measured between 10% and 90% of the full-scale transition

3.7 Timing Diagrams

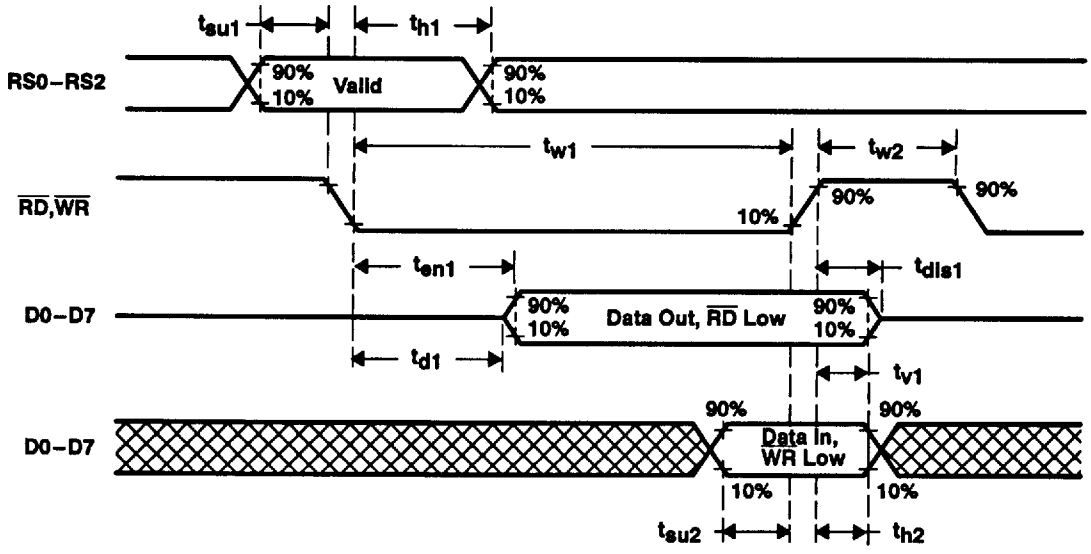

Figure 3–1. MPU Interface Timing

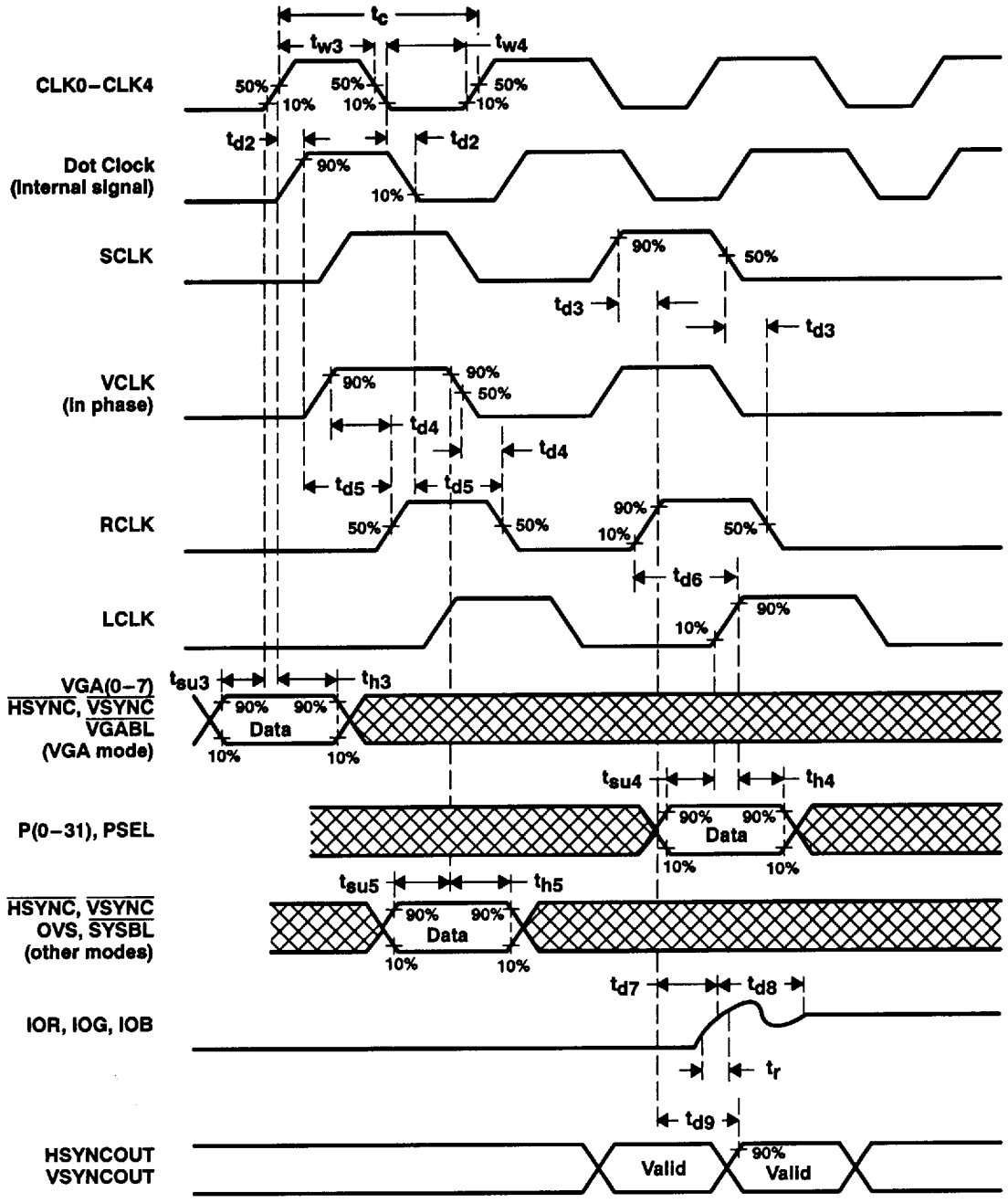

Figure 3–2. Video Input/Output Timing

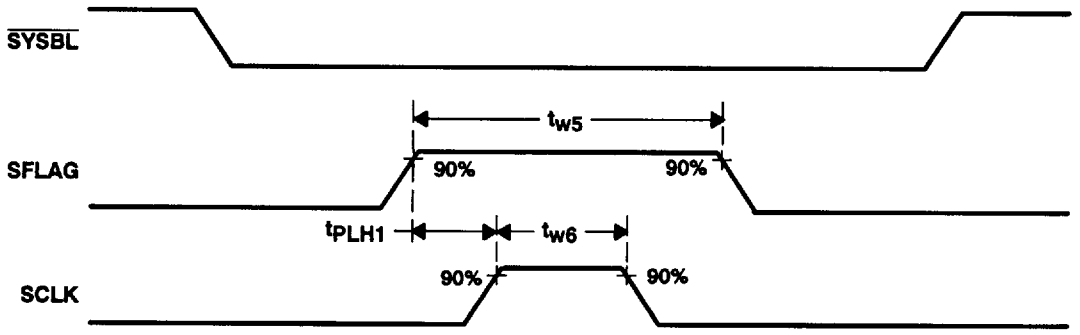

Figure 3–3. SFLAG Timing (When SSRT Function Is Enabled)