DS3RT Device
DS-3 Line Interface
TXC™-02001

PRELIMINARY DATA SHEET

FEATURES

- Provides all functionality required to terminate a DS-3 signal:
  - B3ZS/NRZ decoder
  - Clock recovery and filter
  - All line equalization
  - LOS/LOC detection and AIS generation
- Provides coding violation monitor and high error rate output signal
- Satisfies DS-3 jitter tolerance requirements
- Transmits and receives at the STS-1 rate (51.84 MHz) as well as the DS-3 rate (44.736 MHz)
- Duplicates NRZ outputs for secure operation
- Provides two DS-3 loopbacks:
  - Receive to transmit (digital, no B3ZS)
  - Transmit to receive (analog, no RX amplifiers)
- Meets all applicable ANSI/Bellcore standards:
  - T1.102, 107
  - TR-TSY-000009

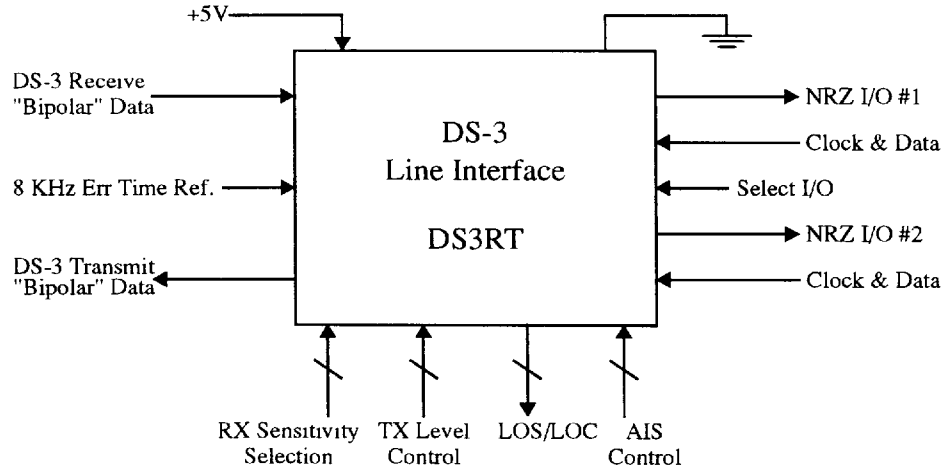
DESCRIPTION

This single CMOS device efficiently replaces traditional means of receiving and transmitting DS-3 signals. It also may be used to transmit and receive SONET STS-1 signals on cable. The DS3RT accepts a wide range of receive signals, and has a unique built-in transversal filter for output pulse shaping. Line compensation is reduced to a simple output level setting using a hardware strap. On-chip filter and clock recovery circuits eliminate the need for external components. A built-in framed AIS generator may be enabled in transmit and/or receive directions when there is a corresponding loss of signal or clock. Signal processing within the DS3RT includes B3ZS decoding/encoding, and the estimation of a bit error rate based on timing the occurrence of coding violations.

DS3RT devices may be operated in parallel for protected applications with appropriate external circuitry. Additionally, the NRZ I/O is duplicated on the DS3RT.

APPLICATIONS

- M13 multiplexers
- DS-3 or SONET transmission equipment
- Test equipment
- DCS and EDSX
- CSU/DSU



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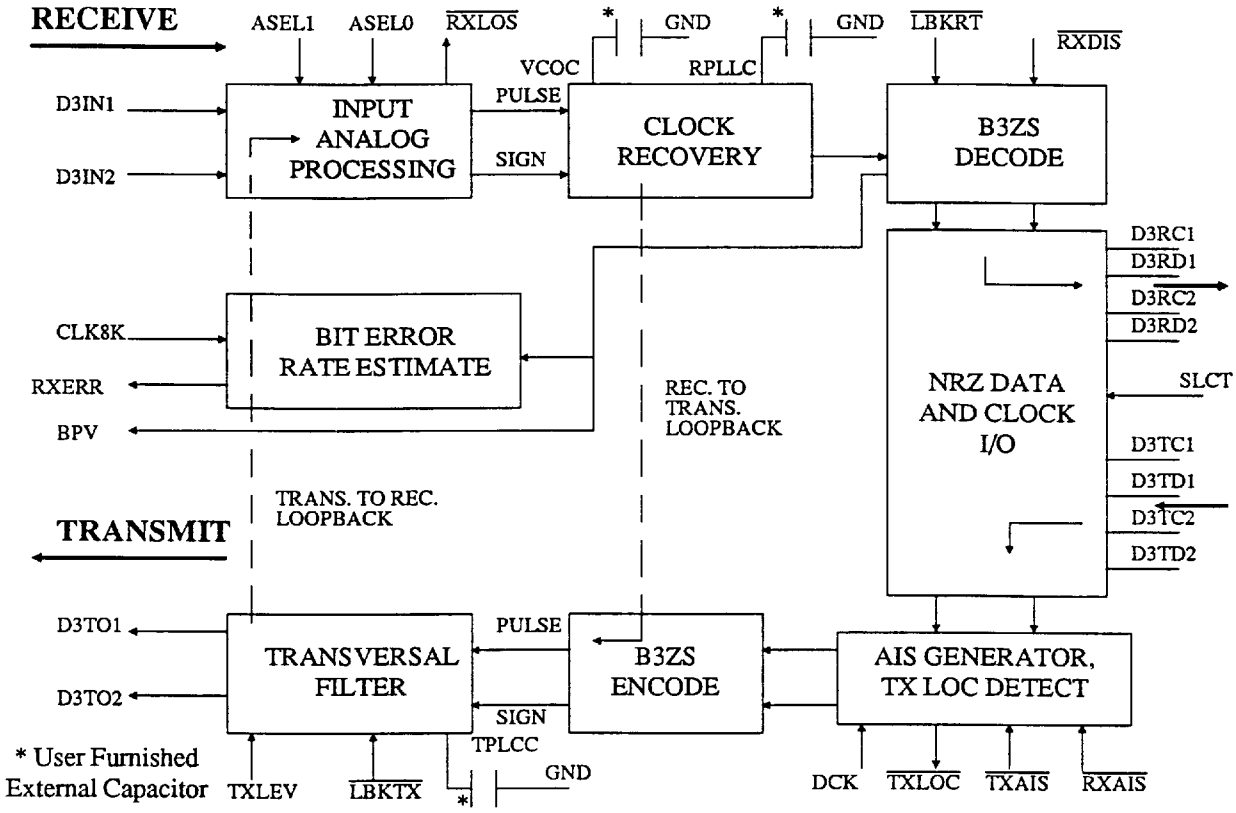
TranSwitch Corporation • 8 Progress Drive • Shelton, CT 06484 USA • Tel: 203-929-8810 • Fax: 203-926-9453

DS3RT BLOCK DIAGRAM



□ BLOCK DIAGRAM DESCRIPTION

The DS3RT accepts a wide range of receive signals, and has two control leads to adjust the input sensitivity: ASEL0 and ASEL1. The input analog processing block also has built-in thresholds for the detection of ones and zeros on the DS-3 line input. The clock recovery contains a phase-locked loop with digital logic for the clock recovery algorithm. The B3ZS decode block uses the logical inverse of the coding algorithm and sends coding violations to the bit error estimate block and to the BPV pin for a raw coding violation output. The NRZ output is directed to the selected pins via the SLCT lead.

The receive side of the DS3RT recovers clock from the B3ZS coded input signal. The average time to recover clock from the onset of received data is 1 ms, with the recommended components connected to RPLCC and VCOC. Correct recovery depends only on the amplitude of the received pulses and the proper setting of the ASEL1 and ASEL2 leads. There is ample overlap of cable lengths to ease the selection of ASEL1 and ASEL2 (see the Control Function Table on page 4).

If the DS3RT detects more than 128 zeros from the cable input, then $\overline{\text{RXLOS}}$ becomes valid. $\overline{\text{RXLOS}}$ may be connected to $\overline{\text{RXAIS}}$ to cause DS-3 AIS or "blue" signal to be sent

automatically on the outgoing D3RDn leads (n = 1 or 2), or $\overline{\text{RXAIS}}$ may be taken low independently to send AIS on the outgoing D3RDn leads.

Coding errors are accumulated in the DS3RT to give an estimate of the received DS-3 error performance. A time base is established with the 8 KHz clock input on CLK8K to cause the $\overline{\text{RXERR}}$ lead to go low when the estimated BER is 10^{-6}. Raw coding violations are available on the BPV lead.

On the transmit side, the NRZ clock and data from the selected input are encoded by the B3ZS encode block. The output of this block feeds a unique built-in transversal filter for output pulse shaping. Line compensation is reduced to a simple output-level setting using a hardware strap, TXLEV. When the $\overline{\text{TXAIS}}$ lead is at ground, the DS3RT generates a DS-3 AIS or "blue" signal internally and transmits it in place of the incoming NRZ signal from the D3TDn pins (n = 1 or 2). If there is loss of clock for about 500 clock cycles, the $\overline{\text{TSLOC}}$ lead goes to ground; and this lead may be connected to the $\overline{\text{TXAIS}}$ lead so that AIS is sent automatically when $\overline{\text{TXLOC}}$ goes low.

NRZ data and clock signals are selected from one of two possible inputs (D3TD1 and D3TC1 or D3TD2 and D3TC2). The DS3RT converts the data to bipolar form using the B3ZS standard to encode the signal. An internal transversal filter shapes the pulses that make up the bipolar signal using digital signal processing techniques and combines the shaped pulses to form the composite B3ZS line signal. The output stage provides a transmit level adjustment (TXLEV) to compensate the transmit output (D3TO1 and D3TO2) for various lengths of cable.

The resulting waveform is such that there is no need for external compensation networks to meet the requirements at the cross connect, regardless of the distance between it and the DS3RT. The plots on pages 8 and 9 show the pulse shape at the cross connect for three different cable lengths.

CONTROL FUNCTION TABLE

CONTROL	STATE	FUNCTION
$\overline{\text{LBKRT}}$	Open Gnd.	Loopback disabled, NRZ to NRZ Loopback enabled, NRZ to NRZ
$\overline{\text{LBKTR}}$	Open Gnd.	Loopback disabled, Bipolar to Bipolar Loopback enabled, Bipolar to Bipolar
ASEL1, ASLE0	Gnd., Open Open, Gnd. Open, Open Gnd., Gnd.	NOT USED 150 to 360 mv peak input 400 mv to 1 v. peak input 200 to 570 mv peak input
TXLEV	Open Gnd.	High Level Transmit Low Level Transmit
$\overline{\text{TXAIS}}$	Open Gnd.	Transmit AIS disabled Transmit AIS enabled
$\overline{\text{RXAIS}}$	Open Gnd.	Receive AIS disabled Receive AIS enabled
$\overline{\text{RXDIS}}$	Open Gnd.	Receiver enabled Receiver disabled
SLCT	Open Gnd.	NRZ I/O with "1" suffix active NRZ I/O with "2" suffix active

□ OPERATING CONDITIONS

Absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{DD} 7V
Input voltage, V_I ..... V_{DD}
Operating free-air temperature range , T_A ..... 0°C to 70°C
Storage temperature range, T_S ..... -65°C to 150°C

Functional Operating Range

V_{DD} = 5 +/- 5%; V_{SS} = 0 (ground) supply voltage
T_A = 0°C to 70°C operating free-air temperature range

INPUT PARAMETERS

PARAMETER	MIN	MAX	UNIT
V_{IH} High-level input voltage	2	V_{DD}+.5	V
V_{IL} Low-level input voltage	V_{SS}-.5	0.8	V
I_{IH} High-level input current		-50	µA
I_{IL} Low-level input current		50	µA
C_{IN} Input pin capacitance		10	pF

OUTPUT PARAMETERS

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	V_{DD}=4.75 TO 5.25 V	2.4	V_{DD}-.05	V
VOL	V_{DD}=5.25V	VSS	0.4	V
I_{OH}	V_{OH} = V_{DD} - .5 V	-1	4	mA
I_{OL}	V_{OL} = 0.4 V	-2		mA
C_{OUT}			25	pF

Power Dissipation

At V_{DD} = 5.25 V and with all ports active, I_{DD} Max is about 100 mA. The maximum power is 500 mW. The nominal power dissipation is 400 mW.

Analog B3ZS I/O

ANALOG INPUT AND OUTPUT PARAMETERS

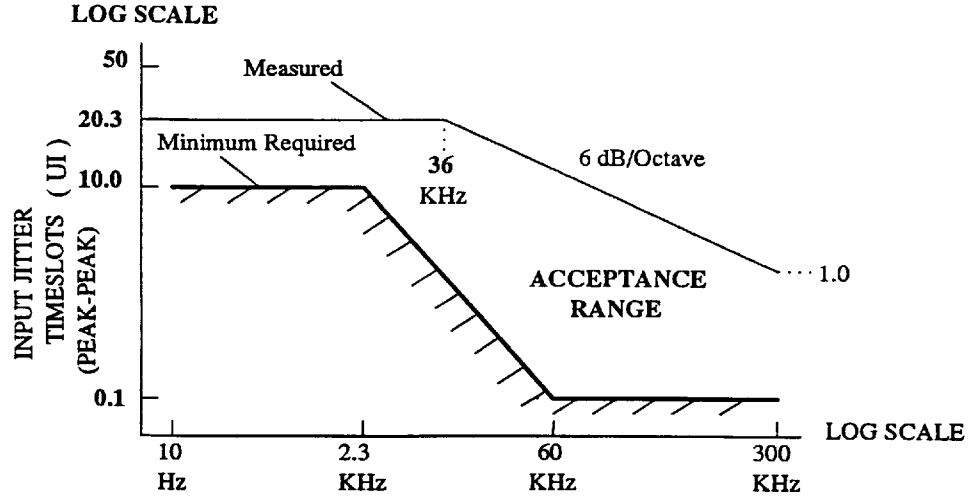
PARAMETER	MAX	MIN	UNIT
Peak input DS3	1.0	0.15	V
Peak output DS3 (TXLVL open)	1.3	1.1	V*
Peak output DS3 (TXLVL gnd.)	0.95	0.85	V*
Input impedance	7200	4800	Ohms
Output 2nd harmonic	-30		dB
Frequency range	52	40	MHz

* In order to meet these voltage output levels, the output of the DS3RT must be loaded with no more than 10K ohms in parallel with 2 pF. See the TXC-02001-AXXX-AN application note for details.

The DS3RT receive side operates error free with a 44.746 MHz interfering signal up to -20 dB below the level of the DS-3 input signal.

DS-3 B3ZS Jitter Tolerance

DS3RT JITTER ACCOMMODATION



JITTER ACCOMMODATION CHARACTERISTIC

This jitter tolerance curve applies at the line input of the DS3RT (pin 29, DS3IN1). The DS3RT properly recovers clock, decodes the B3ZS, and outputs error free NRZ data and clock in the presence of the input jitter characteristic shown in the illustration.

With the recommended values of components on pin 7, VCOC, the jitter transfer through the DS3RT is unity or 0 dB and is independent of the frequency of the jitter. Please see the Application Note for the DS3RT: TXC-02001-AXXX-AN for details.

□ TIMING CHARACTERISTICS

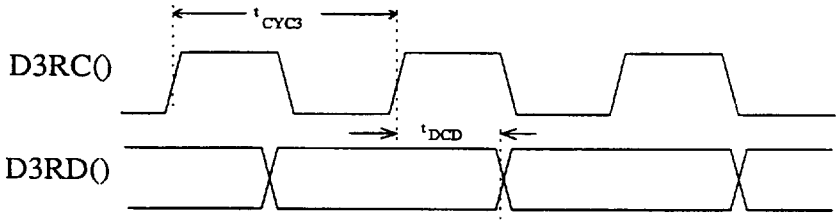
DS3RT TIMING PARAMETERS

PARAMETER	I/O, CONDITION	MIN	MAX	UNIT
t_{DCD}, Delay	Clock high to data change, out	5	15	ns
t_{SDC}, Setup	Data to clock high, in	3		ns
t_{HCD}, Hold	Data stable after clock high, in	2		ns
t_{CH}	DS3TC(1,2) transmit clock high	10		ns
t_{CL}	DS3TC(1,2) transmit clock low	10		ns
t_{CVH}	Coding violation pulse high	20		ns
t_{CYC3}	DS-3 clock cycle time		22.35	ns

A voltage waveform is defined as "high" when it last exceeds V_{OH} or V_{IH}, as appropriate. Likewise, a voltage waveform is defined as "low" when it last goes below V_{OL} or V_{IL}. Timing intervals are defined as the time difference between the crossing of the voltage values on the same or different waveforms. The maximum capacitive load on any digital output is 25 pF.

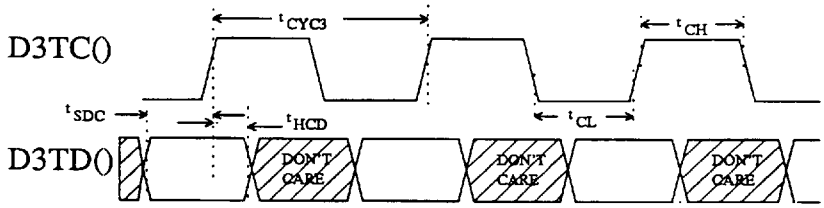
Timing Diagrams

DS-3 NRZ OUTPUT TIMING



This figure illustrates the propagation delay of the data on the NRZ output with respect to the clock.

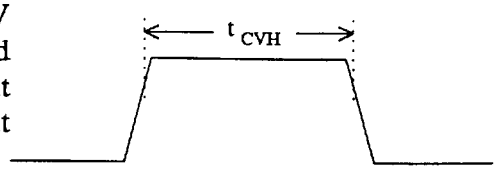
DS-3 NRZ INPUT TIMING



The DS3 transmit signal on the NRZ input to the DS3RT. The brackets stand for the two alternate inputs, 1 and 2. The clock cycle time is nominally 22.35 ns: both receive and transmit clocks have a duty cycle of 50 +/- 5 %.

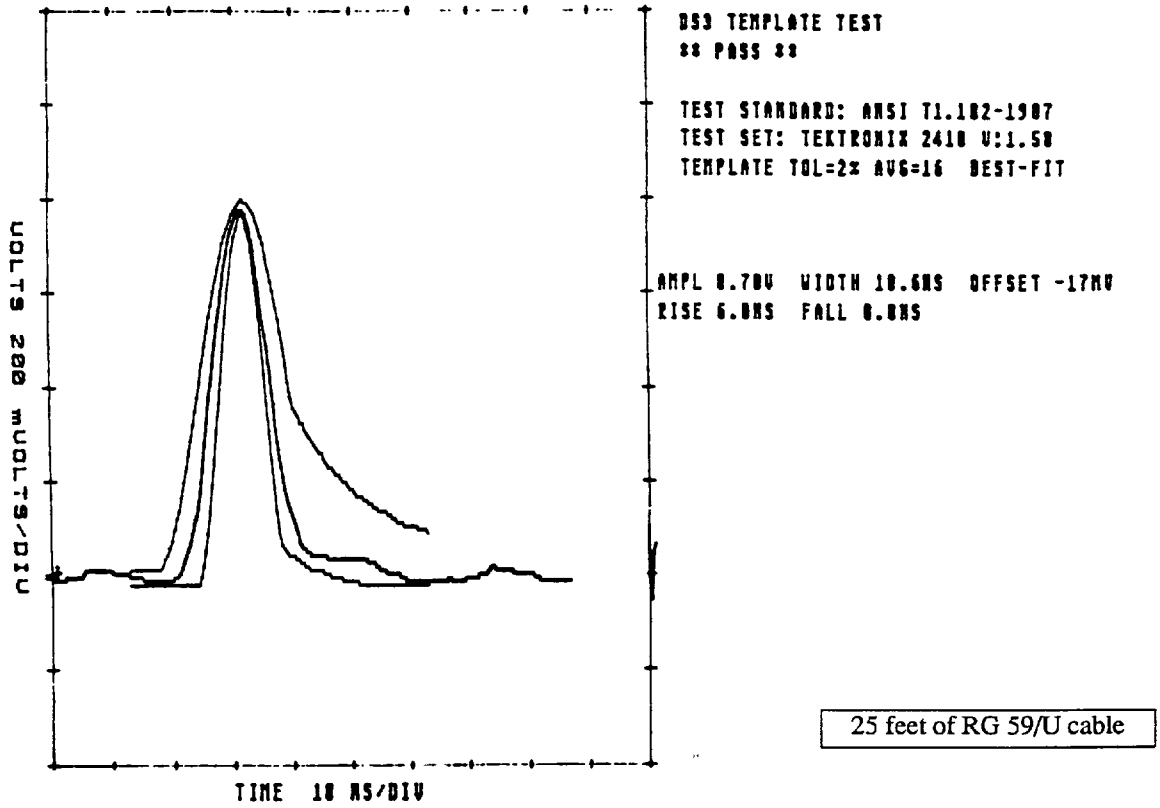
CODING VIOLATION (BPV) OUTPUT PULSE

Only the duration of the coding error signal on the BPV pin is specified. The rise and fall time are load-dependent and are nominally 3 ns maximum. The positive edge of this output is delayed about 15 ns from the positive edge of the output clock, D3RC().

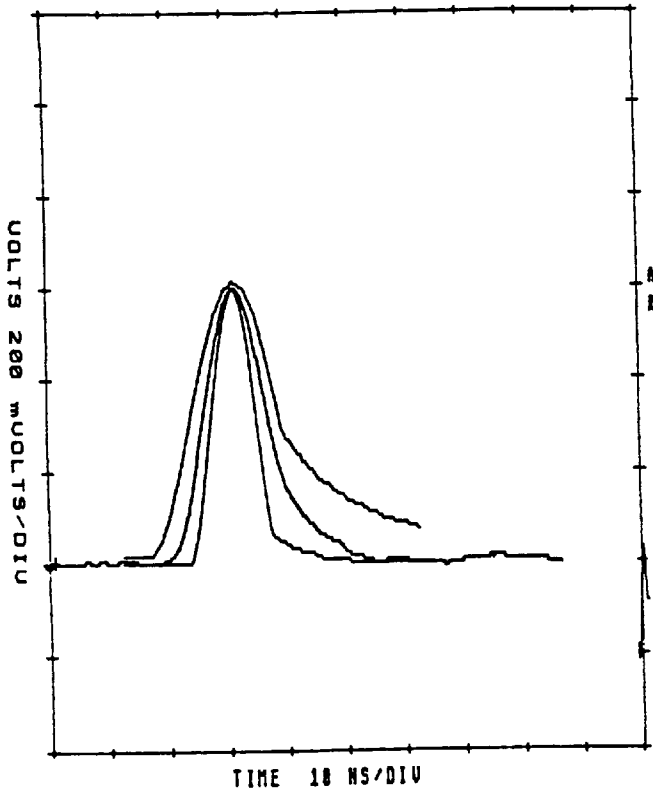


PLOTS OF THE TRANSMITTED WAVEFORM DS3RT WITH BUFFER AMPLIFIER AND TRANSFORMER

The plots on pages 8 and 9 were made from a Tektronics 2410 Digital Interface Test System using a 2% tolerance on the DS-3 mask given in ANSI T1.102-1987. ANSI is adopting % tolerance on the DS-3 waveform mask. The DS3RT requires no external build out, and its tra nit waveform meets the mask at all lengths up to 450 feet, as required.



The peak amplitude of the pulse at the output of the cable of 25 feet is 700 mv. The DS3RT was on TranSwitch's DS3RT test board, TXC-21004-AXXX, and the TXLEV lead (pin 35) was at ground for the low level output (about 770 mv). The ANSI requirement at the DSX ranges from 850 to 360 mv. The observed amplitudes are within the required range for all cable lengths.

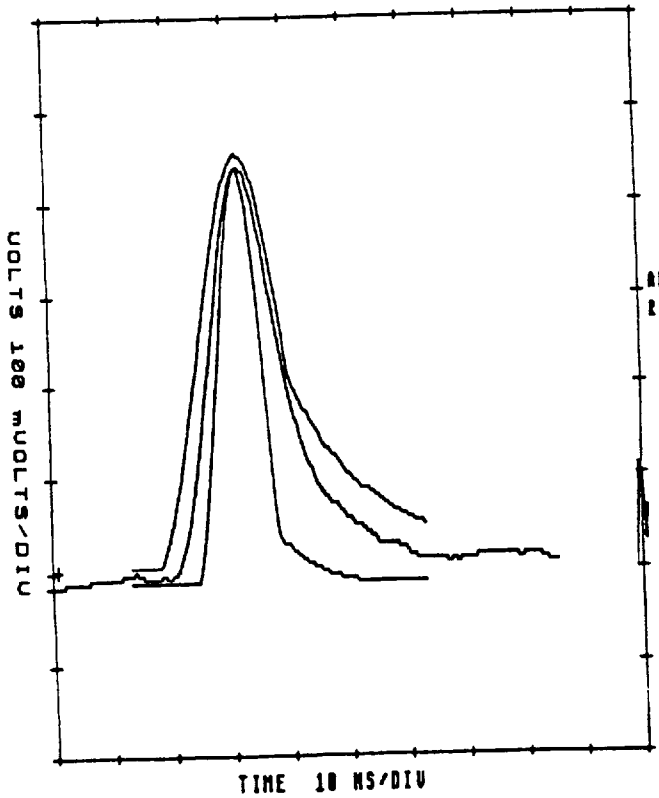


DS3 TEMPLATE TEST
** PASS **

TEST STANDARD: ANSI T1.102-1987
TEST SET: TEKTRONIX 2410 V:1.50
TEMPLATE TOL=2% AVG=8

AMPL 0.68V WIDTH 11.2NS OFFSET -3MV
RISE 6.9NS FALL 13.1NS

225 feet of RG 59/U cable



DS3 TEMPLATE TEST
** PASS **

TEST STANDARD: ANSI T1.102-1987
TEST SET: TEKTRONIX 2410 V:1.50
TEMPLATE TOL=2% AVG=8

AMPL 0.44V WIDTH 12.8NS OFFSET -9MV
RISE 7.1NS FALL 19.1NS

450 feet of RG 59/U cable

□ PIN DEFINITIONS

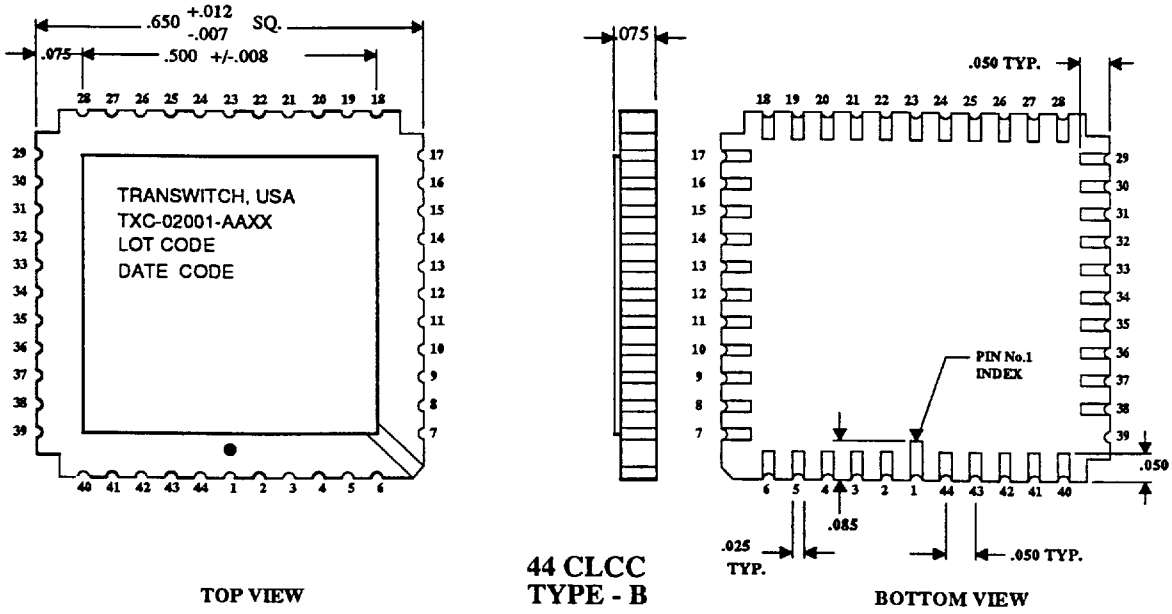
DS3RT PIN I/O AND FUNCTION

NAME	I/O	PIN NO.	FUNCTION
VDD	P	10,23,37,42	5-volt supply voltage, +/- 5%, analog transmit
GND	P	6,11,16,31,36,44	Vss or ground, 0 volts reference, analog receive
$\overline{\text{TXLOC}}$	O	2	Ground-true indication of TX loss of clock
$\overline{\text{RXAIS}}$	I	3	Strap to ground to enable receive AIS
CLK8	I	4	8 KHz clock input to estimate BER
$\overline{\text{RXERR}}$	O	5	Approximate indication of BER>10-6
VCOC		7	External capacitor connection
DCK	I	9	DS-3 external clock for AIS and loss of clock
D3RD2	O	12	NRZ DS-3 receive data no. 2
D3RD1	O	13	NRZ DS-3 receive data output no. 1
D3RC2	O	14	Clock out for receive DS-3 data output no. 2
DS3C1	O	15	Clock out for receive DS-3 data output no. 1
RPLLC		17	External capacitor connection
BPV	O	19	Coding violation pulse output
$\overline{\text{RXLOS}}$	O	20	Ground-true indication of receive loss of signal
$\overline{\text{RXDIS}}$	I	21	Strap to ground to disable the receive path
SLCT	I	22	Strap to ground to enable NRZ I/O no. 2
$\overline{\text{LBKRX}}$	I	24	Strap to ground to loop back RX to TX
$\overline{\text{LBKTX}}$	I	25	Strap to ground to loop back TX to RX
ASEL0	I	26	Receive gain control LSB
ASEL1	I	27	Receive gain control MSB
D3IN1	I	29	DS-3 line input (1 of 2)
D3IN2	I	30	DS-3 line input (2 of 2) - external C
TPLLC		32	External capacitor connection
D3TO2	O	33	DS-3 line output (2 of 2) - external C
D3TO1	O	34	DS-3 line output (1 of 2)
TXLEV	I	35	Line transmit level control
D3TC1	I	38	Clock input for transmit DS-3 data
D3TC2	I	39	Clock input for transmit alternate DS-3 data
D3TD1	I	40	Transmit DS-3 data input
D3TD2	I	41	Transmit DS-3 alternate data input
$\overline{\text{TXAIS}}$	I	43	Strap to ground to enable transmit AIS
N.C.		1,8,18,28	Connect to ground

□ PACKAGING

Both ceramic and plastic packages are available for the DS3RT. The upper drawing is for a 44-pin ceramic package (Type B) with pads for surface mounting. A similar plastic package (Type C) is illustrated below. These and other packaging options are available on request from TranSwitch. The TranSwitch family of DS-3 devices is characterized over the full commercial temperature range of 0°C to 70°C. Burn-in is a customer option.

CERAMIC 44-PIN LEADLESS CHIP CARRIER

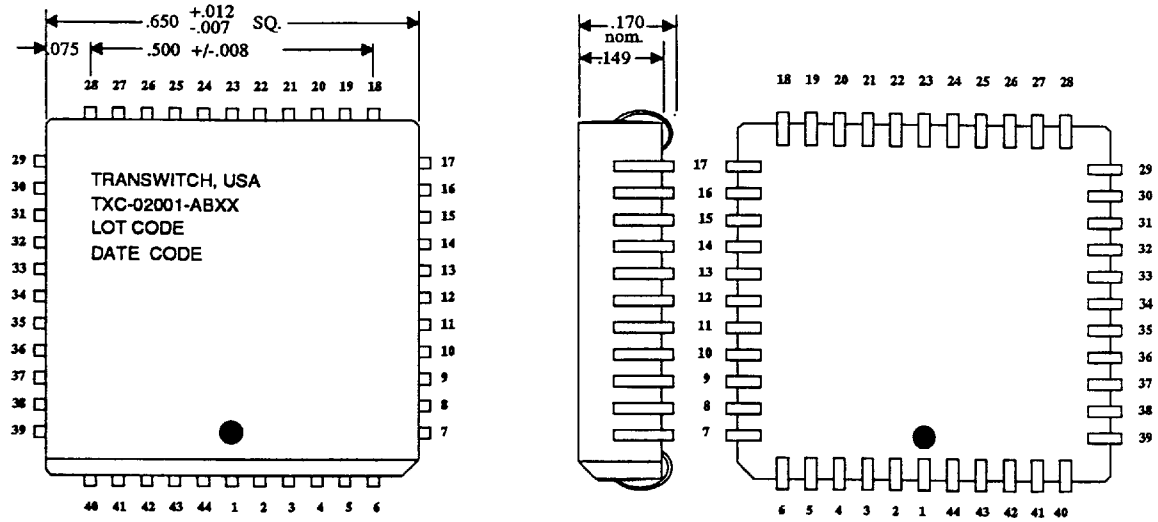


TOP VIEW

44 CLCC
TYPE - B

BOTTOM VIEW

PLASTIC 44-PIN LEADED CHIP CARRIER



TOP VIEW

44PLCC
TYPE - C

BOTTOM VIEW

□ ORDERING INFORMATION

TXC-02001-ACPL	Plastic 44-Pin Leaded Chip Carrier, 0^{o} C to 70^{o} C
TXC-02001-ACCN	Ceramic 44-Pin Leadless Chip Carrier, 0^{o} C to 70^{o} C

Future: -40^{o} C to $+85^{o}$ C version is planned.

□ RELATED PRODUCTS

- TXC-02002-AXXX DS3RTA

  This device is similar to the DS3RT, but does not have the B3ZS codec function and dual NRZ inputs/outputs. The DS3RTA supplies a P and N data rail with clock and clock inputs and outputs on the equipment side. Please see Data Sheet TXC-02002-AXXX-MB.

TXC-02003-AXXX DS3RX

This device has the complete receive (only) functionality of the DS3RT, including dual NRZ outputs. It is useful for DS3 monitoring and similar applications. Please see Data Sheet Summary TXC-02003-AXXX-MA.